Using a Pulsed Supply Voltage for Delay Faults Testing of Digital Circuits in a Digital Oscillation Environment

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Abstract

High-performance digital circuits with aggressive timing constraints are usually very susceptible to delay faults. Much research done on delay fault detection needs a rather complicated test setup together with precise test clock requirements. In this paper, we propose a test technique based on the digital oscillation test method. The technique, which was simulated in software, consists of sensitizing a critical path in the digital circuit under test and incorporating the path into an oscillation ring. The supply voltage to the oscillation ring is then varied to detect delay and stuck-at faults in the path.

1. Introduction

Electro Magnetic Compatibility (EMC) coupled with process variations in deep submicron (DSM) technologies leads to timing related defects modeled as delay faults. The delay faults cause digital integrated circuits to malfunction at the desired clock rates and violate timing specifications. Testing these delay faults is becoming therefore critical in DSM CMOS digital circuits. Testing these high performance digital logic circuits is a difficult and expensive task. As the minimum feature size is decreasing, the gap in speed between the automatic test equipment (ATE) and the device is increasing [1]. Thus devices cannot be tested at their operational speed, unless proper Design-for-Testability (DFT) is provided. Another approach to test these high-performance digital circuits is by using Design-for-Delay-Testability structures [2, 3]. This is the motivation for this investigation wherein we study the fundamental issues pertaining to the digital oscillation test method. Over the past decade, many delay fault models have been proposed, both in functional and structural domains (transition, gate, path, segment, etc.). The fault models vary one from another by trading off the test coverage and computational requirements.

In new DSM technologies, the interconnect delay exceeds the gate delay. The interconnect delay varies as a function of placing and routing efficiency and process variations and is not predictable at gate-level chip simulations.

Much research has already been carried out in delay fault testing. This research includes the development of fault models like: the gate-delay fault model, path-delay faults, robust delay faults, non-robust delay faults and hazard-free delay faults [4, 5]. For all these approaches, the testing setup is rather complicated, for example it needs two sets of latches with precisely controllable test clocks and test-pattern pairs. These approaches are therefore time consuming and occupy a lot of silicon area.

One way to overcome this critical test setup is to make use of the digital oscillation test method. In this paper it will be shown that by introducing a varying supply voltage in combination with the oscillation test method it is possible to detect delay faults as well as stuck-at faults in the particular sensitized critical path in the digital circuit under test (CUT) [6, 7].

The paper is organized as follows. Section 2 gives a brief review on delay faults and section 3 covers the oscillation test method. In section 4, 5 and 6 the proposed technique will be discussed. In section 7 some conclusions are provided.

2. Low Voltage Testing

Hao and McCluskey first showed in [8] that very-low-voltage (VLV) testing can detect flaws in CMOS integrated circuits (IC's). A delay flaw is a defect that causes a local timing failure, but the failure is not severe enough to cause malfunctioning of the IC.

A delay fault is a timing failure that makes the circuit fail to work at the designed speed and to function at a slower speed. Most studies on testing timing failures concentrate on the detection of delay faults. However, some timing failures that are embedded in short paths may not cause delay faults at normal operating conditions. The supply voltage for low voltages testing for detection of delay faults should be set in the region where the changing rate of the propagation delay of a CMOS gate starts increasing significantly. Earlier studies [8, 9] show that VLV testing is effective for fault detection. Furthermore, it is non-destructive to a CUT.

3. The Oscillation Test Method

The oscillation test method is concerned with sensitizing a critical path and then test for delay faults. Critical paths are those paths that have the longest propagation delay from primary input to primary output. Therefore, the critical path is the most likely path for a

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delay fault to cause the circuit to malfunction. To sensitize a path, all off-path logic value inputs must be set to non-controlling values [10]. In the oscillation test method for digital circuits one considers the well-known digital ring oscillator in which an oscillation occurs when there is an odd number of inverting elements in the ring. If an even amount is present an inverter is added in the feedback path. The earlier mentioned sensitized path in the CUT is then incorporated into a ring oscillator to test for delay faults. The oscillation frequency is determined by the propagation delay through the sensitized path. Any delay-fault or stuck-at-fault that may alter or stop the oscillations, can be detected by observing the oscillating frequency. A simple combinational circuit, with critical path going from Input B through gates 1, 2 and 4 to output Q, is shown in figure 1. In figure 2, the same critical path is sensitized with the output Q connected to the input B to be used in the oscillation test method. This is shown as the feedback path in figure 2 and will need a multiplexer to enable it for test purposes only. The 0 and 1's indicated in figure 2 represent logic levels needed for sensitization of the particular critical path. The X represents a changing state due to the oscillation in the critical path. Therefore, a given delay increase in a critical path may result in a malfunction in the circuit but, the same delay increase in another path may not effect the circuit functionality and performance.

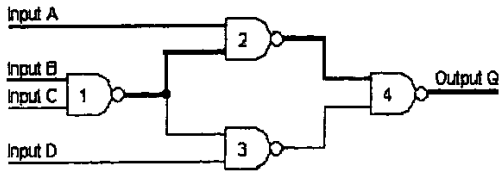

Figure 1. Critical Path in Circuit Under Test

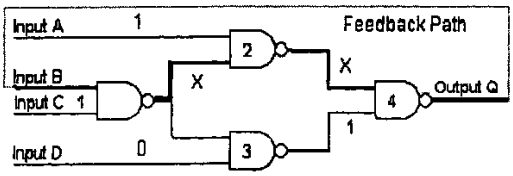

Figure 2. Sensitized Critical Path in Circuit Under Test

The oscillating frequency (fosc), is a function of the propagation delay through the critical path. Therefore, the loss or the deviation of the oscillating frequency from its nominal value can be employed to detect delay faults in the circuit.

4. A New Test Technique

4.1 Test Principles

The principle of the oscillation test method is based on the fact that when there is loop with an odd number of inverting elements in a combinational circuit, it will oscillate at a unique frequency. This oscillating frequency will be stable as long as the sensitized path is preserved and no defects occur. As soon as a change in the particular path in the circuit occurs, or a fault is present, that will change the propagation-delay time of the specific path in the circuit, then the unique oscillating frequency will change.

Several different approaches have been proposed for the detection of delay faults by using the digital oscillating method. One method was used to precisely measure the maximum operating frequency by measuring the delay through the critical paths. Hence, the method was able to detect gate delays, path delays, and stuck-at faults [6]. Another method uses the counting of the output pulse within a time period when oscillating, and detects if the circuit was operating correctly or if faults are present [7].

Our proposed method is concerned with varying the supply voltage of the CUT and observing the output, which is also connected to the input of the specific critical path that is being dealt with. This test must be done with every critical path that was identified in the CUT. In figure 3 one can see the flow diagram of the steps of our proposed method. First, the critical paths in the combinational circuit have to be identified. Next, the critical path has to be sensitized and one has to make sure that there are an uneven number of inverting elements to ensure oscillation. Next we will look in detail at the characteristics of the varying supply voltage and how it was established.

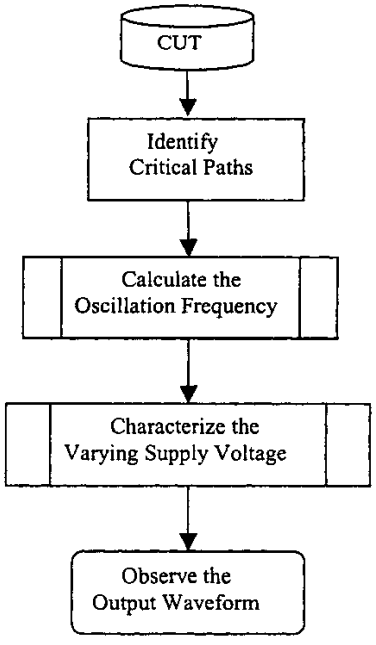

Figure 3. Different Steps in Proposed Test

4.2 Test Strategy

The first step in the test strategy, as shown in figure 3, is the identification of the critical paths. Since a lot of work has been published on this matter [10], it is not part of this investigation. It is therefore assumed that all critical paths have been identified. As from now, one particular critical path will be chosen and used in the remainder of this paper. The second step is to measure the typical oscillating frequency of the circuit with the critical path being sensitized. This can be easily done, for example using a digital counter to capture the characteristics.

Next, a varying supply voltage will be applied to the CUT. The next section will be focused on establishing the characteristics of the circuit due to the varying supply voltage. The last part of the test will be to observe the output waveform of the CUT whilst varying the supply voltage. The characteristics of the output waveform will show if any delay or stuck-at faults are present. One has to remember that a stuck-at fault can be detected as a delay fault with infinite delay. Later it will be shown how to interpret the output waveform to be able to prove if delay faults are present in our CUT. Figure 4 shows the nominal oscillating frequency of the CUT with a constant supply voltage of 5 volts for the configuration that was shown in figure 2.

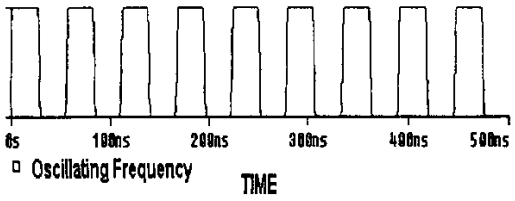

Figure 4. Simulated Oscillating Output of Sensitized Path in Circuit Under Test (see fig. 2) with a Constant Supply Voltage of 5 volts.

5. Varying the Supply Voltage

In our proposed method it has been investigated to change the shape of the supply-voltage of the CUT. In our proposed technique it is required to apply a supply voltage with the same pulse width as the normal oscillating frequency of the circuit. The varying supply voltage will therefore be a square wave with 50% duty cycle and period equal to that of the normal oscillating frequency of the CUT. One therefore has to ensure that the circuit is still able to operate correctly when the supply voltage is changed to a low value [11]. The supply voltage is critical, which is also a parameter that influences many other characteristics of a particular circuit.

The operating speed of any circuit can be increased by raising the supply voltage (V_{CC}) and lowering the temperature. Changing the supply voltage varies the overall performance of the chip or circuit. Voltage drops on the power distribution system can result in variations in delay across the chip. The variation of power on an active circuit changes the tolerance of delay and noise margin on the circuits as well as the threshold voltage (V_T) specifications.

When looking at varying the supply voltage one first has to consider the implications of such variations on the circuit performance. Transistor drive current and therefore circuit speed performance is proportional to the gate overdrive (V_{CC}-V_T) raised to the power n where n is between 1 and 2 $((V_{CC}-V_T)^{n})$. When lowering the supply voltage, the gate overdrive is rapidly decreasing for DSM devices, thereby strongly degrading device performance if the normal operating temperature is assumed. This decreasing gate overdrive is enhancing sub-threshold leakage, which is fundamental to silicon MOSFET operation and is set by the device threshold voltage. It is therefore clear that one cannot lower the circuit supply voltage without carefully considering the above mentioned.

It has been investigated to which extent one can decrease the supply voltage without causing the circuit to malfunction. In our tests, use was made of SPICE and using the 0.35 μm TSMC CMOS technology from MOSIS [12]. A combinational circuit was used as test vehicle and the supply voltage was lowered and operation of the circuit verified. This test shows that the optimal minimum value for this specific test circuit is 1.75 volts. The normal supply voltage of the circuit was 3.3 volts. This test was also repeated on the same combinational circuit making use of 0.8μm technology with normal supply voltage of 5 volts. The results show that 1.75 volts was again the optimal minimum value for the supply voltage that constantly ensures correct operation of the circuit. It was therefore decided that 1.75 volts would be used as the minimum value for our varying supply voltage. This relates closely to the result from previous work on VLV [8, 9] in which it was stated that the supply voltage ideal range for VLV testing is between 2 and 2.5 times the threshold voltage of the specific technology that is used. Our technology has a minimum threshold voltage of 0.69 volt and it convert therefore to a supply voltage of 1.73 volts if the above-mentioned results are considered. This varying supply voltage will only be applied during the testing phase.

In figure 5, the shape of the varying supply voltage signal is shown together with the output waveform of the combinational circuit as was shown in figure 1. This result shows the normal unique oscillating frequency while a varying supply voltage is applied to the CUT. This simulation was done on a number of simple combinational circuits. The simulations were carried out using SPICE and the 74HC High-Speed CMOS series was used to form the combinational circuits. The only synchronization that is needed is that the varying supply voltage must have a logic high initial start condition.

Figure 5 shows the result when a varying supply voltage is applied. The oscillation occurs as with normal supply voltage as shown in figure 4.

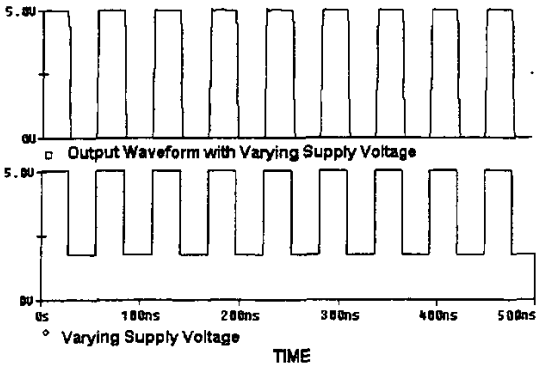

Figure 5. Output Waveform under a Varying Supply Voltage

6. The Fault Detection Process

6.1 Test Setup

A simple possible implementation for our proposed test techniques is shown in figure 6. The control logic block controls the input logic and output logic as well as the signal comparison. The good circuit response is compacted into a good machine signature and compared to the output response of CUT. The stored response will be with respect to either the number of transitions or the duty cycle of the output waveform of the circuit. The purpose of the input logic is to apply the test patterns to the CUT. The output logic is to generate the signal that the comparator will compare with the stored signature. Finally, the control logic directs the whole operation. It controls the input and output logic, generates the required input pattern and evaluate the oscillating frequency.

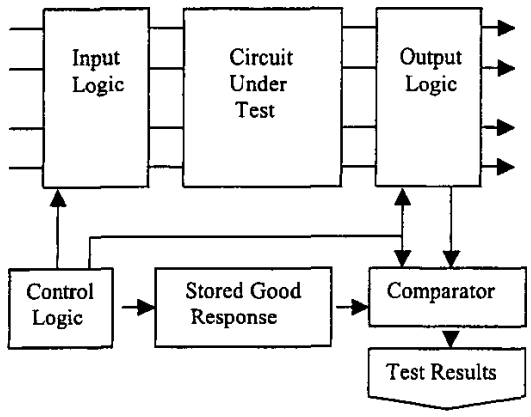

Figure 6. Block Diagram Representation of Typical Test Organization for the Proposed Technique

It must be noted that this test organization assume that there is only one path sensitized and converted to oscillation at a given time. There is an option to include the above-mentioned evaluation and input pattern generation on-chip as Built-in-Self-Test (BIST).

Care must be taken for introducing faults into the test setup due to the extra circuitry needed. The extra circuitry must be self-checking or be included in the test process as an initial test.

6.2 Experimental Results

First, stuck-at faults were introduced into our combinational circuit. A stuck-at 0 and then a stuck-at 1 fault were introduced into the sensitized critical path. The simulations were carried out using PSpice and the 74HC High-Speed CMOS series was used to form the combinational circuits. The results show clearly no oscillation occurred and it was therefore easily detected. The overall propagation delays of the combinational circuit was 73ns. The next part of the test simulations was concerned with inserting extra delay into the critical path and observing the output waveform. The same combinational circuit as before was used. The first graph of figure 7 shows the output in the case of an extra delay of 10ns in the critical path and the second if the delay is 4ns. The results are shown in figure 7.

The waveforms show that the normal oscillation characteristics are now not present. If one look at the signal above 1.75 volts the presence of the extra delay is noticeable because the oscillation is clearly abnormal. Further simulations show that one important parameter of the varying supply voltage is that the period of it must be equal to the period of the normal fosc.

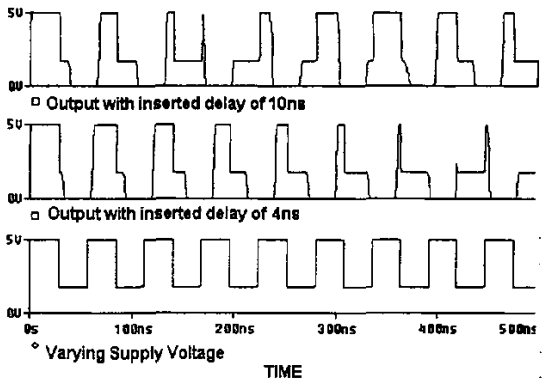

Figure 7. Output Waveform with Extra Inserted Delays

The next parameter that was changed was the duty cycle. This was in an effort to make the detection of even smaller delay faults possible. Simulations show that the best results were obtained with a 10% duty cycle of the supply voltage. Results of simulations done in PSpice with the same circuit as above are shown in figure 8. The

waveforms show that if the signal above the 1.75 volt margin is considered the inserted delay of 1 ns result in an output that is not oscillating any more.

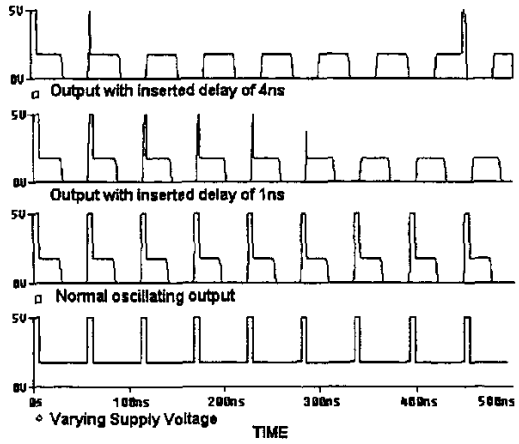

Figure 8. Output Waveform with Extra Inserted Delays and Duty Cycle of 10%

7. Conclusions

Digital oscillation test methods have already been used for measuring precisely the maximum operating frequency of a circuit. It has also been used for detection of faults by observing the output or by counting the output frequency. In this paper we have explained and shown results of a proposed technique by applying a varying supply voltage to the CUT while it is oscillating and observe the output.

The scheme connects outputs of the CUT to its input with odd inversion parity and applies appropriate input patterns to the unconnected inputs to sensitize paths of the circuit, converting them to oscillation rings. The effect of a change in duty cycle was also shown. By observing whether the output oscillates normally or not, at the target frequency, one can tell whether the circuit is working properly or not. This testing method requires simple added hardware, which can be applied externally or built internally in the circuit to be part of a Built-in-Self-test architecture. The area overhead for this test method will depend on the complexity of the circuitry to change the duty cycle. This testing of the circuit can be done at-speed with this technique. The influence of process- and application-induced variations can have a major effect of the testing results [13]. Additional simulations must be done to establish the influence of these variations on this test method.

The test resolution depends on the technique employed to measure and evaluate the oscillating frequency. This test technique will have a very small impact on the chip performance because it is only active during the test sequence.

Acknowledgements

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