THE BLACK SILICON METHOD V: A STUDY OF THE FABRICATING OF MOVABLE STRUCTURES FOR MICRO ELECTROMECHANICAL SYSTEMS

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ABSTRACT

This paper presents a study of various well-known release techniques (bulk- and surface-micromachining) for the fabrication of movable silicon micromechanical structures. Their pro's and con's will be discussed. Further, a detailed study of a new self-aligned plasma technique is presented which uses *silicon on insulator wafers (SOI)*. It has the ability to etch, release, and passivate MEMS *in one RIE run*. Therefore, MEMS can be fabricated quickly, accurate, and at low costs.

INTRODUCTION

Starting the process, usually a sandwich of poly-Si on top of SiO_2 is used. However, for SCS structures BESOI (Back etched SOI) or SIMOX (Separation by ion implantation of oxygen) wafers have to be used [1-3]. SCS is characterised by a low intrinsic damping, -fatigue, -hysteresis, and -built-in stress making it an ideal material for vibrating structures. Additionally, there are no constraints in structure height and the wafers are commercially available.

After etching micromechanical Si structures, they have to be released. This isn't straightforward and many techniques have been proposed. Frequently -in surface micromachining- the SiO_2 layer is used as a sacrificial layer which is etched using wet- or vapour etchants [4-6]. They are cheap but suffer from the so-called sticking problem - due to surface tension of liquids- and many solutions have been proposed to solve this [5-12]. In bulk micromachining some very useful -dry- plasma release techniques have been proposed [13,14]. Sticking isn't found in dry etching making this technique more reliable. Nevertheless, all the proposed techniques -wet, vapour, and dry- have always specific constraints, therefore the BSM multi-step one-run process is proposed as a more sophisticated dry release technique able to extend the limits.

VAPOUR ETCHING

In vapour HF etching the removal of the sacrificial SiO_2 layer is -almost- directly transformed into the gas phase. Nevertheless, condensation of water vapour is needed to uniformly initiate etching which may cause sticking [5]. Another problem with this technique is that some reaction products may precipitate on the surface reducing the yield. J. Ruzyllo showed that these problems can be suppressed by etching at low pressure in an anhydrous HF/CH_3OH gas mixture at elevated temperature [6].

WET ETCHING

Generally, HF is used for sacrificial layer etching SiO_2. However, for long thin beams the yield is low due to: 1) Structure damage caused by bubble formation during etching and rinsing steps during cleaning and 2) structural deformation resulting in stiction during drying. The first problem is difficult to control but for the last problem several techniques have been developed such as: freeze drying [7,8], photoresist-assisted releasing [9-11], and surface modifications [12].

Freeze drying: This technique uses e.g. cyclohexane as the final rinsing agent. After freezing -at 7 °C- it is sublimated thus avoiding sticking. This is accomplished by placing the substrate under a forced nitrogen flow on a regulated Peltier element with a temperature just below the freezing point. Nevertheless, for long thin structures we observed a low yield, caused by bubble- and rinse-damage and -in spite of careful "sublimation"- we still observed stiction.

Photoresist-assisted releasing: This technique uses a resist layer temporally to avoid stiction. There are at least three different approaches found in literature: A resist pattern used as "rubber feet" under the microstructures to carry them [9], a resist pattern side ways or on top of the structures to hold them [10] and a photoresist refill to replace the final rinsing liquid [11]. After sacrificial layer etching and drying, the photoresist layer is removed by an O_2 plasma. A disadvantage of the first two techniques is that an extra mask has to be aligned, the second approach is only possible for special mask designs, and the last technique requires a uniform coating of photoresist beneath the structures for successful releasing. All techniques are less successful for long thin MEM structures with high aspect ratios (>5) and small gap spaces (<2μm).

Surface modification: Important parameters to consider for the sticking effect during drying a micro structure in a wet etchant are the surface free energy and wetting angle. If the wetting angle is lower than 90 degrees, beams will be attracted to the nearest surfaces. In contrast -at higher angles- beams are "pushed away", thus preventing sticking. The magnitude of the force is a function of both the surface free energy and wetting angle. Shortly to prevent sticking, the etchant or structure surface should be modified to create a wetting angle exceeding 90 degrees. Although this technique is very promising little activity is found in this area [12].

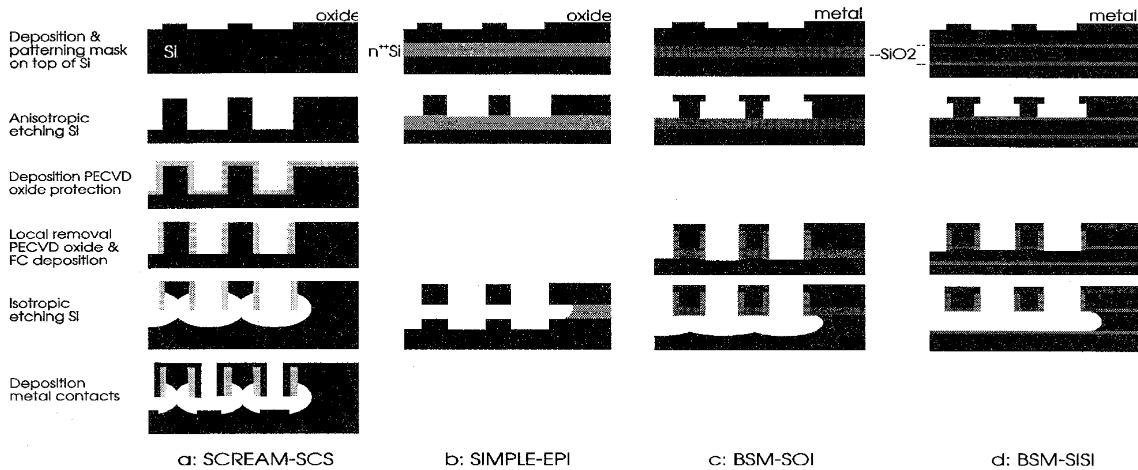

Figure 1: Various dry plasma techniques: SCREAM, SIMPLE, and BSM.

PLASMA ETCHING

To avoid sticking dry etching technologies have been presented recently such as the SCREAM and SIMPLE processes [13,14]. Both techniques are self-aligned and suitable for batch fabrication. Now, the releasing of the structures takes place in the gas phase so there is no liquid phase, responsible for stiction.

SIMPLE: The acronym SIMPLE stands for silicon micromachining by single step plasma etching [13]. This technique uses a CL_2-based plasma chemistry which etches p- or lightly doped Si anisotropically but heavily n-doped Si isotropically. In such a way movable MEMS can be patterned and released from the substrate in a single-step RIE plasma as shown schematically in fig.1b. However, disadvantages of SIMPLE are: 1) A thick PECVD oxide mask is needed as a mask material because the Si/SiO_2 selectivity is rather low in a CL_2 plasma. 2) The under etch rate is low (50 nm/min) and is a function of the doses of the buried layer and the spacing between the micro beams. 3) After etching, the bottom beneath the structures shows deep trenches, which may affect the moving of free-hanging structures.

SCREAM: The acronym SCREAM stands for single-crystal reactive etching and metalisation [14]. In fig.1a the process scheme of this technique is shown: After directional chlorine-based etching of Si using SiO_2 as a mask-material, the trenches are passivated with a PECVD oxide. This oxide is removed at the bottom of the trench (CHF_3 plasma) and after that an isotropic fluorine-based etch (SF_6) will release the structures. For electrical contacting, a deposited metal layer is needed. Notwithstanding its potential, there are some disadvantages such as: 1) The released structures are hollowed out during the isotropic etch (Fig.2a), 2) RIE lag while etching the Si directional may cause problems during the isotropic etch because the etch depth might be different at both sides of a beam (Fig.2a), 3) the deposited PECVD layer should be stress-arm or tensile to avoid buckling (Fig.2b), and 4) the mask layer should be stress-arm to avoid bending after the releasing (Fig.2c). The first two problems make mask design rules necessary. Additionally, many process steps are needed to fabricate the MEMS (e.g. RIE, PECVD, MIE, and sputter equipment) which is time-consuming and might limit the yield.

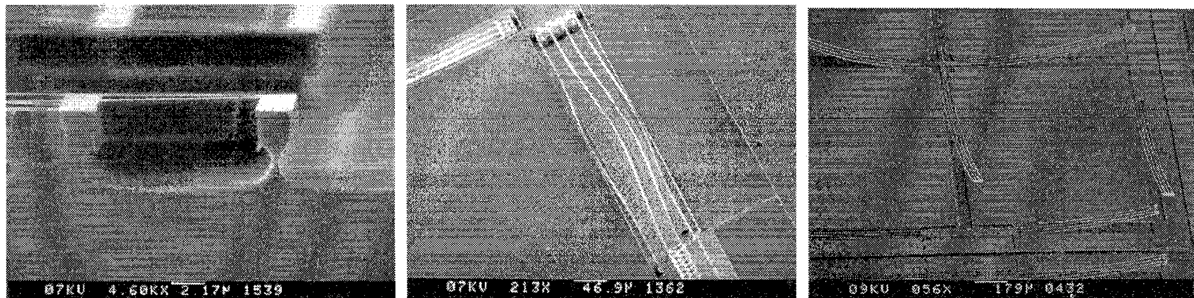

Fig. 2: a) Hollowing out of beams and asymmetrical releasing due to RIE lag. b) Buckling due to compressive stress. c) Bending due to stress in the mask.

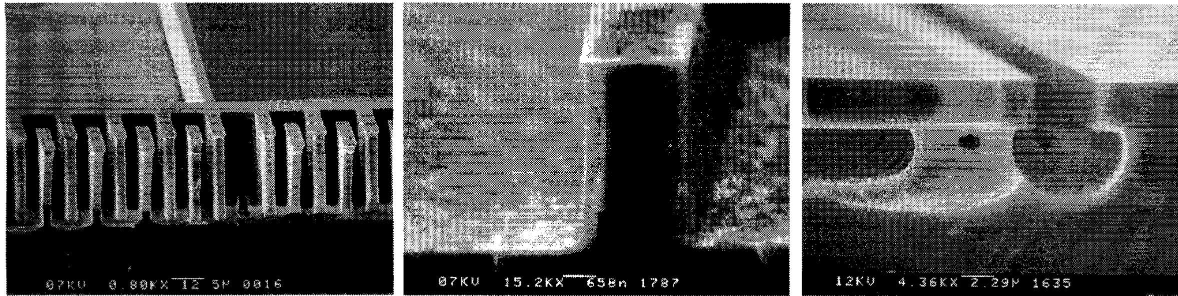

Figure 3: a) Anisotropic etching with $SF_6/O_2/CHF_3$ plasma. b) Sidewall passivation with CHF_3 plasma. c) Isotropic etch with SF_6 plasma.

BSM multi-step one-run: To solve the problems mentioned in the previous sections a new technique has been developed which has the ability to etch, passivate, and release MEMS in one run. This technique, the so-called *BSM multi-step one-run process* is developed on an Electrotech, Plasmafab 310-340 twin deposition/etch parallel-plate system operating at 13.56 MHz. The technique starts with commercially available BESOI wafers (Fig.1c). After the deposition of a 30 nm (lift-off) mask for the pattern definition, the movable structures can be fabricated in only one RIE run with four individual steps (fig.3): 1) The (an)isotropic $SF_6/O_2/CHF_3$ RIE of the top Si, 2) the CHF_3 RIE of the insulator together with the passivation (C_xF_y film) of the sidewalls of the structures, 3) the $SF_6/O_2/CHF_3$ RIE of the floor, and 4) the SF_6 RIE of the bulk Si. Eventually, the process can be finished with a conformal step coverage of a C_xF_y film to protect the released structures from the environment [15]. For instance, these fluorocarbon (FC) films do have an extremely low surface tension and therefore they repel water and others. With this technique it is possible to release long thin Si beams successfully as indicated in fig.4.

RESULTS & DISCUSSION

We fabricated xy-stages, micro grippers, springs etc. with typical dimensions listed in figure 5 in comparison with the SCREAM and SIMPLE processes. As can be seen, the only limiting steps are aspect ratio of trenches and beams.

BSM SOI: There are some important remarks to consider in the BSM technique i.e.: 1) Anisotropic etching: The profile has to be vertical with a little under etch making it possible to deposit a FC layer where no ion bombardment occurs i.e. under the "roof" of the mask. The profile can be adjusted by using the BSM method [16-18]. Also RIE-lag can be suppressed by applying this method [17]. When the intermediate insulator of the SOI wafer is reached, the etch process has to be stopped, to avoid unwanted under etching. This is a crucial step because when the SiO_2 is reached, the loading is decreasing causing a strong enhancement in lateral etching. The etching process is stopped by e.g. visual inspection. Typical parameters during etching are $SF_6/O_2/CHF_3$ gasflow=30/10/7 sccm, power flux=0.3 W/cm^2, self-bias=40 V, pressure=75 mTorr, 3 inch Si loading, and target temperature=10 ^oC. 2) Sidewall passivation: The deposition of FC is a function of e.g. pressure and self-bias [15]. This layer is necessary to protect the sidewalls during isotropic etching. We observed a satisfying coverage of the sidewalls directly under the mask roofs at pressure=20 mTorr, power flux=0.3 W/cm^2, self-bias=600 V, and CHF3 gasflow=10 sccm. A typical deposition rate for this process is 20 nm/min. Simultaneously, during this step the insulator is etched at a speed of ca. 50 nm/min. 3) Isotropic etching: Before starting the isotropic etching with an SF_6 plasma it is necessary to "clear" the floor of the trenches first with an oxygen-based plasma such as $SF_6/O_2/CHF_3$.

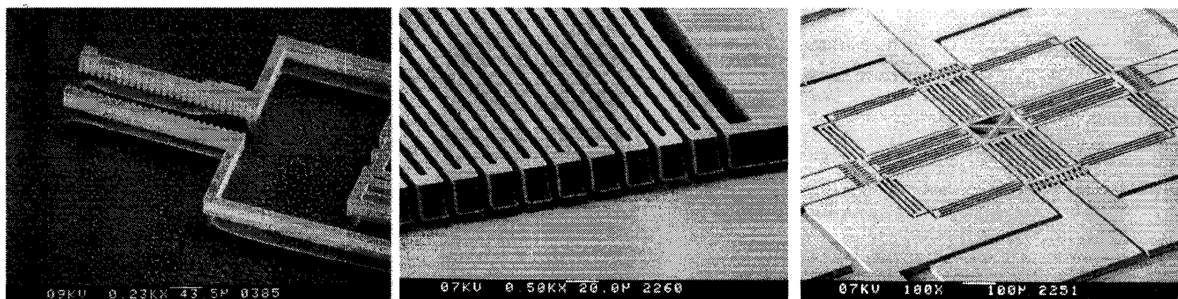

Figure 4: A few typical examples of the BSM SOI process scheme: A gripper (left), part of a spring (mid), and xy-stage (right).

Process Step	Description	Etch/deposit rate
1. Photolithography	Transfer pattern	Shipley 1805
2. Metal deposition	E-beam: Cr 25 nm	6 nm/min
3. Lift-off	Acetone	xxx
4. Trench etching	$SF_6/O_2/CHF_3$	0.5 -1 μm/min
5. Wall passivation	CHF_3	20 nm/min
Oxide etching	CHF_3	50 nm/min
6. Floor etching	$SF_6/O_2/CHF_3$	1 min
7. Releasing	SF_6	0.5-1.0 μm/min
8. FC Deposition	CHF_3	20 nm/min

Beam structure	SCREAM	SIMPLE	BSM
Height (μm)	<20	<4	<400
Width (μm)	<5	<4	<50
Length (μm)	<2000	<2000	<2001
Lateral Gap (μm)	>1	>3	>1
Aspect ratio beam	<10	<10	<50
Aspect ratio trench	<7	<7	<10

Figure 5 : Outline of BSM one-run process with typical dimensions.

Some remarks about BESOI: When a relative thick intermediate layer (>0.1μm SiO_2) is used, bending of the beam structure may occur due to compressive stress in the oxide layer. Another problem might be differences in stress between the two bonded silicon wafers, which introduces bending and/or buckling of beams.

BSM SISI: A disadvantage of the BSM SOI technique is that -after releasing the free hanging structures- deep trenches are found and the under etch rate is limited due to the relatively high Si loading. To eliminate this problem we constructed a Silicon on Insulator on Silicon on Insulator (SISI) wafer. Now, a Si layer of (1-2 μm) is used as a sacrificial layer surrounded by two insulators (fig.1d and 6a). The deepest lying insulator protects the Si during releasing resulting in a smooth/flat bottom and a small loading thus high lateral etch rate (>1μm/min).

CONCLUSIONS

It can be stated that the BSM multi-step one-run process is favourable for the releasing of MEMS with long thin beams. It includes the Black Silicon Method as an excellent tool for profile control and to suppress RIE-lag.

Instead of SiO2, a thin metal (30 nm Cr) layer is used as a mask, which has an almost infinite selectivity with respect to Si and creates less additional stress problems (bending). The Fluorocarbon layer has a low Young's modulus which prevents stress problems in long thin beams (buckling). The intermediate layer of SOI prevents the beam for hollowing out during the isotropic etch making an exact definition of the structure height possible. After the mask is deposited it is now possible to fabricate very quickly, accurate, and at low cost free-hanging MEMS (e.g. an accelerometer, tuneable spring/filter, AM/FM modulator, or micromechanical transistor) in one process run with a RIE plasma without turning the plasma of.

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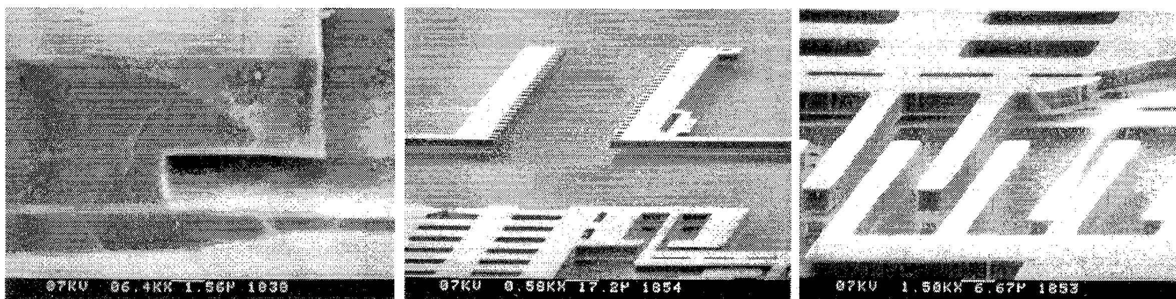

Figure 6: The BSM SISI process: Profile view (left) and some examples (mid, right).