

# HIGH RESOLUTION SHADOW MASK PATTERNING IN DEEP HOLES AND ITS APPLICATION TO AN ELECTRICAL WAFER FEED-THROUGH

G.J. Burger, E.J.T. Smulders, J.W. Berenschot, T.S.J. Lammerink, J.H.J. Fluitman and S. Imai\*

MESA Research Institute, University of Twente, P.O.Box 217, 7500 AE Enschede, the Netherlands  
Tel: XX-31-53 892 805, Fax: XX-31-53 309 547

\*Mechanical Engineering Research Laboratory, Hitachi Ltd., 502, Kandatsu, Tsuchiura, Ibaraki 300, Japan

## SUMMARY

This paper presents a technique to pattern materials in deep holes and/or on non-planar substrate surfaces. A rather old technique, E-beam evaporation of metals through a shadow mask, is used [1]. The realisation of high resolution shadow masks using micromachining techniques is described. Further, a low ohmic electrical wafer feed through with a small parasitic capacitance to the substrate and a high placing density is presented.

## INTRODUCTION

High resolution patterning in deep holes and/or on non-planar ( $> 10 \mu\text{m}$ ) substrate surfaces is an often encountered problem in micromechanics. The main cause for this problem is that normal resist spinning can not be used on such a substrate. But even if spray-on resist or spin-on photosensitive polyimide is used, the pattern resolution is limited by the lithographic resolution in a deep hole which additionally may be interfered by optical reflections in the hole. The high pattern resolutions presented in this paper are realised by E-beam evaporation of metals through a shadow mask. The use of micromachining techniques for the realisation of the shadow mask, together with recently developed aligning and bonding tools, significantly improve the pattern resolution and alignment accuracy.

## METHOD

Evaporation is done by heating a source of desired material under high vacuum conditions ( $< 10^{-3}$  Pa) to its melting temperature. In this pressure range the mean free path of the vapour atoms is much larger ( $> 10$  m) than the distance of the source to the substrates. Therefore the vapour atoms stream in straight lines radial from the source to the substrate. If a "shadow mask" is brought between the source and the substrate the "shadow" pattern is transferred to the deposited layer, see figure 1a. It is obvious that the deposited pattern is always larger than the pattern in the shadow mask. The enlargement ( $E$ ) can easily be calculated from the geometry of the evaporation equipment. In most equipment this enlargement shall be in the order of one tenth percent (e.g.  $c = 0.5\text{m}$ ,  $d = 0.5\text{mm} \Rightarrow E = 1.001$ ). On wafer scale this means a deviation in the order of several tens of microns.

An other deviation in the deposited pattern is illustrated in figure 1b. When the substrate and shadow mask are not placed exactly perpendicular to the vapour stream than the pattern will be shifted. An angle of  $1^\circ$  gives a pattern shift of  $10\mu\text{m}$  ( $d = 0.5$  mm). Therefore the positioning of the substrate should be arranged carefully for accurate pattern definition.

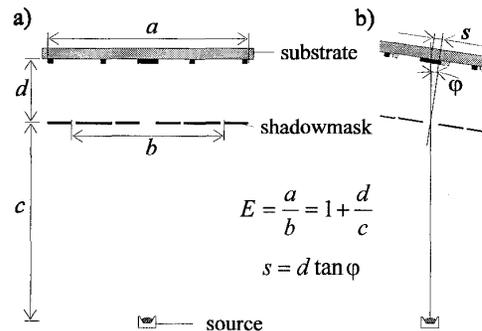


Figure 1. E-beam evaporation through a shadow mask; a) enlargement of the pattern; b) shift due to rotation.

If we focus on the edge of a deposited pattern we find a smooth decay (spreading) in layer thickness, see figure 2. This is mainly because the vapour source is not a point source, which results in a penumbra region near the edge of the patterns.

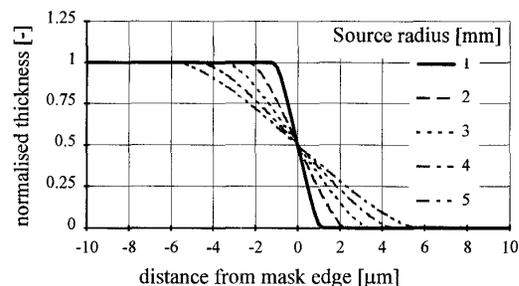


Figure 2. Calculated thickness profile near the edge of a pattern deposited from a circular source. A uniform emission over the source area is assumed. The source-mask distance ( $c$ ) is 350 mm and the mask-substrate spacing ( $d$ ) is 0.38 mm.

Another reason for spreading is that if the sticking coefficient of the vapour atoms is lower than unity they will scatter at the mask edge and/or the substrate [2]. These scattered atoms may be deposited under the shadow mask. Both effects result in an undesired thin film of evaporation material in the shadow regions. However, since this spreading is much thinner than the desired pattern it can easily be removed by dipping the substrate in an appropriate etch solution.

To determine the resolution which can be achieved, tracks of aluminium were deposited through a shadow mask with slits of different width. Figure 3 gives the normalised track thickness as a function of the slit width at different deposition rates ( $r$ ) and mask substrate spacings ( $d$ ). At small slit widths the thickness drops drastically, which indicates the non-point source effect. The achievable resolution is determined by the slit width at which the layer thickness is comparable with the maximum value. It is clear that the resolution depends strongly on the mask substrate spacing, however a resolution of 5  $\mu\text{m}$  can easily be achieved.

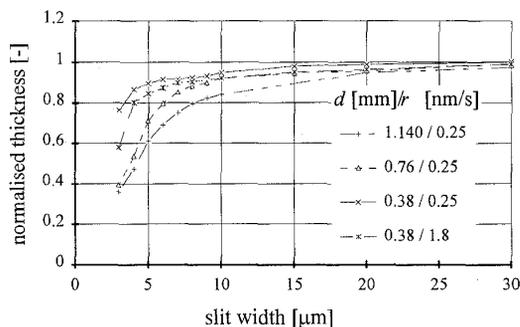


Figure 3. Relative track thickness of aluminium tracks deposited through a slit. Process parameters:  $c = 350 \text{ mm}$ ,  $d = 0.38 \text{ mm}$ , a: deposition rate =  $0.25 \text{ nm/s}$ , background pressure =  $6 \cdot 10^{-4} \text{ Pa}$ , source radius  $\approx 2 \text{ mm}$ . b: deposition rate =  $1.8 \text{ nm/s}$ , background pressure =  $6 \cdot 10^{-4} \text{ Pa}$ , source radius  $\approx 2 \text{ mm}$ .

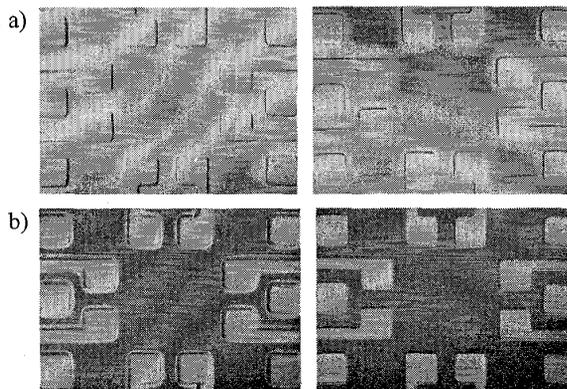


Figure 4. Spreading around deposited aluminium patterns; a) as deposited; b) after 60 s etch in a NaOH solution. deposition rate; left:  $1.8 \text{ nm/s}$ , right:  $0.25 \text{ nm/s}$ .

At higher slit width the thickness gradually reaches the maximum, this indicates the scattering effect. Figure 4a gives an illustration of the spreading due to scattering. It can be seen that the spreading depends on the deposition rate. Lower deposition rates give a better pattern definition, however, the surface roughness of the deposited layer is much larger. Figure 4b shows the structures after a short dip in an appropriate etchant. The resulting structures are well defined without spreading caused by scattered atoms.

## SHADOW MASKS

Shadow mask patterning was (is) a very important tool in thin film processing of components, such as resistors, resistor arrays, capacitance's end electric circuitry on a large variety of substrates. Usually the masks are realised in metal or graphite sheets by e.g. milling, arc erosion or laser cutting. The smallest aperture can be around 50  $\mu\text{m}$  with a tolerance of 5  $\mu\text{m}$  [1]. The limitations in resolution and the topical constraints on shadow masks (circular connected patterns cannot be used because the inside should be supported) are responsible for the inapplicability in normal micromachining processes, however shadow mask can be useful in cases where normal patterning (lithography) is difficult.

The shadow masks presented in this paper are realised by using bulk micromachining techniques. With this, a smallest aperture of 2  $\mu\text{m}$  with a tolerance of 0.5  $\mu\text{m}$  can be obtained. The deposited pattern resolution in a typical evaporation set up can be around 5  $\mu\text{m}$  ( $d < 0.5 \text{ mm}$ ). The spreading near the pattern edges can also be of advantage because the area under a small beam (e.g. 2  $\mu\text{m}$  width) of the shadow mask will be covered completely if the spreading is larger than the width of the beam. In this way a circular connected pattern can be realised by suspending the inside mask part of the mask by beams of 2  $\mu\text{m}$  width.

Here, two shadow mask are evaluated, namely; a silicon shadow mask, and an integrated shadow mask.

### Silicon shadow mask

The shadow mask is made of a  $\langle 100 \rangle$  oriented silicon wafer (see figure 6a-c, left). The shadow pattern is anisotropic dry etched (RIE)  $\pm 25 \mu\text{m}$  deep [3] and covered with LPCVD silicon nitride (0.5  $\mu\text{m}$ ) (a). Then membranes are etched (25% aqueous KOH solution at  $75^\circ\text{C}$ ) from the backside till the shadow pattern is clearly visible (b). Finally the silicon nitride membranes are removed by dry etching (RIE) (c). The etch time in the KOH is not very critical because the shadow pattern is etched anisotropically, therefore the shadow image will not change due to over etch. Figure 5 gives an illustration of a realised shadow mask.

To bond the shadow mask onto the substrate a few droplets of photoresist are deposited near the edge of the shadow mask and the mask is spun at 1000 rpm. After a short prebake (5 min,  $90^\circ\text{C}$ ) the two wafers are aligned and

fixed, using a mask aligner with aligned bonding facilities[4]. The actual bonding is done by heating the package to 150 °C for 20 minutes in nitrogen ambient. After evaporation of the desired material the mask can be removed by exposing the package to an oxygen plasma at 120°C for about 30 minutes.

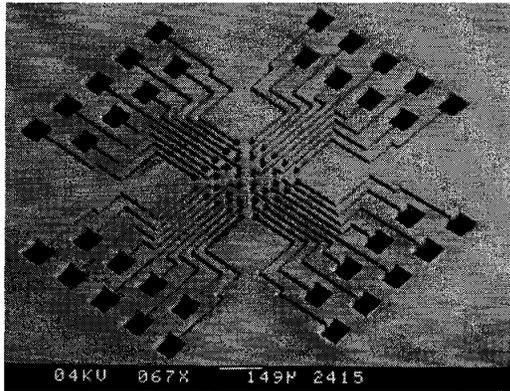


Figure 5. Micromachined shadow mask; this mask is used for the pattern shown in Figure 7.

#### Integrated shadow mask

Here the realisation of the shadow mask is integrated in the same substrate on which it is needed. For example an KOH under etched beam may act as a shadow mask for the underlying hole or channel (e.g. see figure 9). This is a very elegant usage of the shadow mask principle because of its simplicity and no need of alignment with the etched structures. However the available patterns and applicability to electrical contacting is limited.

#### APPLICATIONS

In the literature several electrical wafer feed-through's are found [5,6]. Most of these are rather large because generally each connection needs a hole through the wafer. Therefore the contact density is low ( $\approx 1/\text{mm}^2$ ) and the connections have a high parasitic capacitance to the substrate. Realisation of multiple connection tracks through one hole can easily be realised with the shadow mask method. Figure 6 shows the basic process steps of the realisation of the feed through contacts.

First the feed through holes are etched (25% aqueous KOH solution at 75°C) down to a silicon nitride membrane (a). The silicon nitride membrane is removed and a short etch dip (KOH) provides for smooth hole edges (b). A LPCVD silicon nitride layer is grown for electrical insulation (c). A silicon shadow mask is bonded onto the substrate, as described before, and the aluminium tracks are deposited (d). After removing the shadow mask, small connection holes are etched in the silicon nitride membranes from the other side of the wafer and the connection layer is deposited (e). Prior to this deposition the spreading may be removed. The electric connection may be disturbed due to a

thin native oxide layer between the two metal layers. The connection can be improved by an anneal step at 450°C for 15 min. For this application the deviation (shift) of the pattern deposited on the membrane due to a misalignment of the substrate with respect to the vapour stream, is not harmful because the succeeding pattern steps can easily be aligned to the pattern on the membranes.

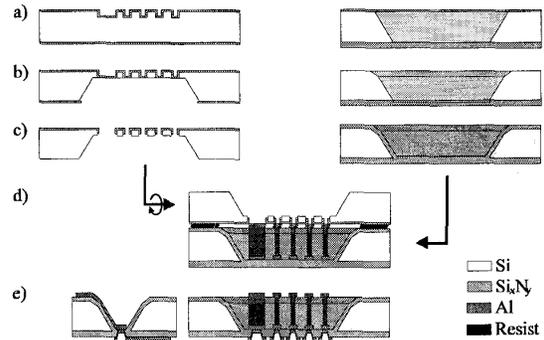


Figure 6. Process scheme of the electric wafer feed through using a silicon shadow mask.

Figure 7 gives a SEM photograph of the realised feed-through's. Table 1 gives the typical specifications of an electric connection with tracks of 10  $\mu\text{m}$  width through a 380  $\mu\text{m}$  thick wafer.

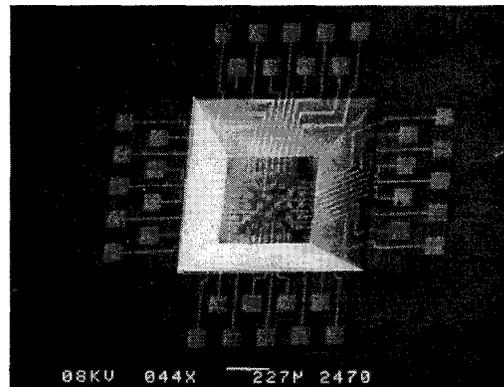


Figure 7. Realised feed-through's; the hole is 380  $\mu\text{m}$  deep and covers an area of approximately  $1 \times 1 \text{ mm}^2$ , the 36 signal tracks are 10  $\mu\text{m}$  wide, the silicon nitride insulation layer is 0.5  $\mu\text{m}$  thick.

Resistance [ $\Omega$ ]	Capacitance [pF]	Contact density [number/ $\text{mm}^2$ ]
< 5	< 1	36

Table 1. Specifications of the realised feed-through's.

Using this process the resolution in the hole is at least 5  $\mu\text{m}$  and a large variety of patterns can be deposited. Figure 8 shows an example of a coil which is deposited in a hole.

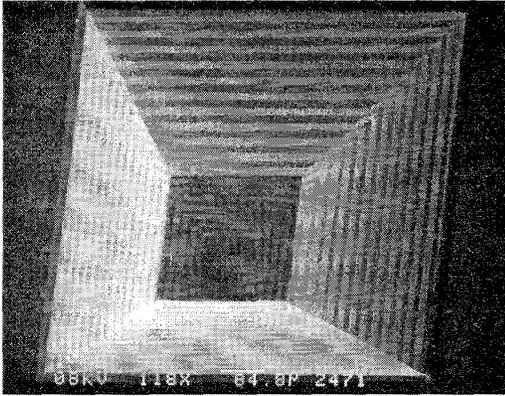


Figure 8. A coil in a hole, the track is  $10\mu\text{m}$  wide (seen from above).

A wafer feed-through can also be realised with an integrated shadow mask, see figure 9. The actual silicon nitride shadow mask is deposited prior to the silicon nitride KOH etch mask. After KOH etching of the hole, and removal of the etch mask the silicon nitride shadow mask is left above the hole. Now a short isotropic silicon etch provides for a deepened trail under the shadow mask. After deposition of the desired metal the tracks deposited in the trail will be disconnected from the top surface.

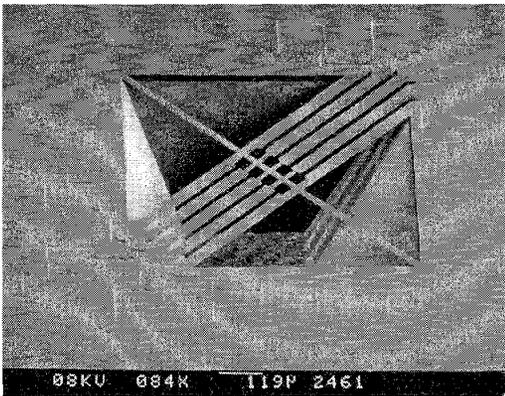


Figure 9. A feed-through realised with an integrated shadow mask.

The integrated shadow mask technique has also been applied successfully in the realisation of carrier beam structure of a vibro-actuated micro-mover [7], see figure 10. Here, a silicon nitride mask was subsequently used as an KOH-etch mask, as a diffusion mask during oxidation and as a shadow mask during aluminium deposition. HF etching was used to pattern the silicon oxide. After etching of aluminium, nitride and silicon the structure as shown is obtained.

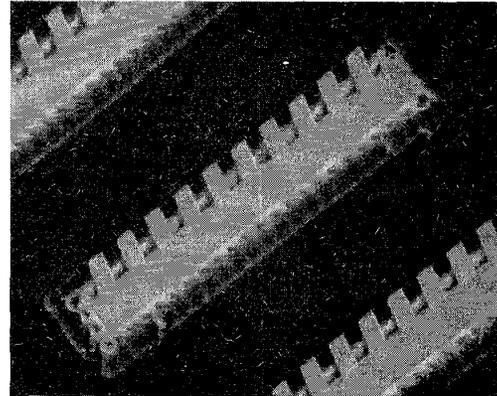


Figure 10. Inclined silicon oxide beams for a vibro-actuated micro-mover.

## CONCLUSIONS

Evaporation of metals through a shadow mask is used for high resolution patterning in deep holes. The presented micromachined masks and aligning processes significantly improve the practical resolution of shadow mask patterning. A resolution of at least  $5\mu\text{m}$  in a hole of  $380\mu\text{m}$  deep is demonstrated. The technique successfully applied to a high density, low-ohmic electrical wafer feed-through.

## REFERENCES

- [1] Glang, R; and Gregor, L V. Generation of patterns in thin films, Handbook of thin film technology, McGraw-Hill (1970) pp. 7-1 - 7-10.
- [2] Gray, S; and Weimer, P K. Production of fine patterns by evaporation, RCA Review, 20 (1959) 413-425.
- [3] Jansen, H; et. al. The black silicon method: A universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control, Proc. MME'94 (Pisa, Italy, Sep. 1994) pp. 60-64.
- [4] Electronic vision, AL-6.
- [5] Esashi, M. Micromachining for packaged sensors. Proc. 7th Int. Conf. on Solid-State Sensors and Actuators, Transducers '95, (Yokohama, Japan June 7-10, 1993), pp. 260-265.
- [6] Linder, S; Baltus, H; Gnaedinger, F; and Doering, E. Fabrication technology for wafer through-hole interconnections and three-dimensional stacks of chips and wafers, Proc. 7th IEEE Workshop on Micro Electro Mechanical Systems, MEMS'94, (Oiso, Japan, January 25-28, 1994), pp. 349-354.
- [7] Smulders, E J T. To be published.