Reduction of Intrinsic 1/f Device Noise in a CMOS Ring Oscillator

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Abstract

The implications of intrinsic 1/f device noise reduction in MOS transistors due to periodic on-off switching in a CMOS ring oscillator are explored. It is shown that maximising the amplitude of oscillation helps to reduce the close-in phase noise. Measurement results, corrected for amplitude-dependent upconversion and effective bias show an improvement of 8 dB in phase noise at 1KHz frequency offset from the carrier at 4.5 dB increase in carrier power.

1. Introduction

Ring oscillators are widely applied in areas such as digital data processors and wireless communication circuits. In these applications oscillator phase noise critically affects system performance. Recently, especially the close-in phase noise (which is largely determined by 1/f device noise in CMOS oscillators) has received increasing attention [1].

This paper's primary objective is to bring to the footlight a mechanism for reducing the intrinsic 1/f device noise by periodic on-off switching of MOS devices. The effect was reported in 1991 [2] but we seem to be the first to explore its implications. The amount of 1/f noise reduction strongly depends on the gate-source voltage in the OFF state. In a CMOS ring oscillator this reduction mechanism can result in a decrease of the 1/f frequency noise (which is equivalent to $1/f^3$ phase noise) when the amplitude of oscillation is increased.

In [3] we presented results of spectral sideband measurements performed on a 3-stage CMOS ring oscillator. A 10 dB decrease of the 1/f frequency noise related sideband strength, relative to the carrier power, was observed for a 2dB increase of the carrier power. The dominant mechanism by which device noise is upconverted to the oscillation sidebands is FM-modulation. As a drastic change in the efficiency of the FM-upconversion seemed unlikely, these results qualitatively suggested that periodic on/off switching of the MOS transistors in the ring caused a reduction of their intrinsic 1/f device noise. A recent paper [1] shows that the efficiency of (FM-) upconversion is strongly dependent on the symmetry properties of the oscillation waveform. The present paper therefore gives new experimental results, in which the upconversion efficiency is actually measured for each of the oscillation amplitudes used. By correcting the phase noise measurement results for (1) measured changes in the upconversion efficiency, and for (2) changes in the effective biasing of the MOS devices, the final results are convincingly shown to be in good agreement with baseband 1/f device noise measurements.

The results presented here are relevant for the optimisation of the $1/f^3$ phase noise in CMOS oscillators: designers should maximise the oscillation amplitude so as to reduce intrinsic 1/f device noise.

2. Baseband 1/f device noise under switched bias conditions

In this section, the influence of gate-source voltage switching on the baseband 1/f noise current PSD of an NMOST is investigated. For this purpose, the experimental setup depicted in figure 1 is used.

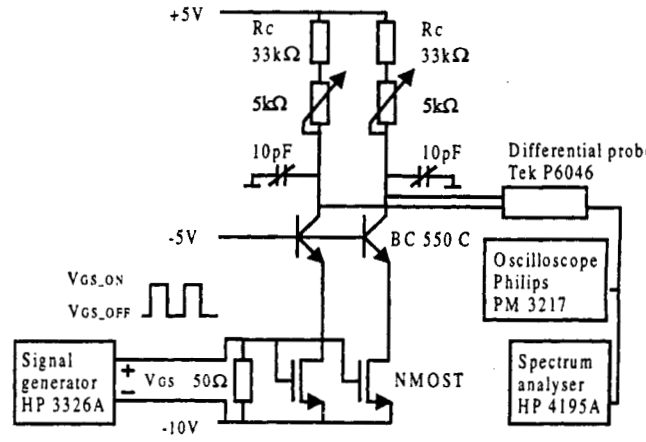

Figure 1. Baseband 1/f noise measurement setup.

The gates of two NMOS transistors are driven by a square wave signal which is characterised by a 50% duty cycle, a maximum voltage level V_{GS_ON} and an adjustable minimum voltage level V_{GS_OFF} (see table 1) which remains below the threshold voltage. To suppress the influence of the large common mode switching signal, the output noise voltage is measured using a differential

probe. The resistors and capacitors are adjusted to compensate for the effects of MOS transistor mismatch. More details on the measurement setup can be found in [3]. Figure 2 presents the measurement results; curve A corresponds to the case of steady-state bias, while curves B-D correspond to the cases of switched bias with different V_{GS_OFF} (see table 1).

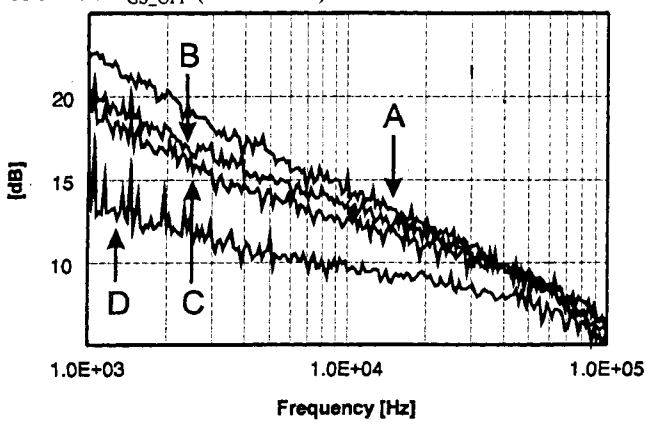

Figure 2. Measured baseband 1/f noise in the cases of steady-state (A) and switched bias (B-D, table 1).

The applied square wave bias signal has repetition frequency 2 MHz, duty cycle 50 % and V_{GS_ON}=2.5 V. Curves B-D have been shifted up by 6 dB to correct for the effect of duty cycle. At frequencies beyond about 100 kHz, the influence is observed of the pole associated with the output nodes in the experimental setup. Figure 2 leads to the remarkable conclusion that the V_{GS_OFF} voltage supplied to the MOS devices affects their 1/f noise in the ON state. This conclusion was reported earlier by Bloom and Nemirovsky, who used a rather complicated measurement setup [2].

Table 1. V_{GS_OFF} values corresponding with the curves in figure 2 (V_{GS_ON}=2.5 V in all cases).

Curve nr. (Fig. 2)	V_{GS_OFF} [V]
A	non switched
B	0.7
C	0.4
D	0

3. Phase noise measurement

Figure 3 shows the experimental setup for the phase noise measurements on a 3-stage ring oscillator. The oscillation amplitude can be adjusted by means of the resistors Rn. For experimental freedom, the inverter stages were based on standard HEF4007 chips. NMOS and PMOS transistors in these chips have roughly equal β-factors, so that good oscillator waveform symmetry may be expected. In order to facilitate the measurement of upconversion efficiency and to compare the phase noise measurements with the baseband device noise measurements of section 2, the channel width of the NMOS transistor in stage 3 is taken half that of the other NMOS transistors. In this way the oscillation waveform exhibits maximum asymmetry at node c (see figure 5), leaving stage 3 the dominant contributor to upconversion efficiency [1], irrespective of the oscillation amplitude (verified by measurement). Although upconversion efficiency has been increased deliberately in this experiment, in practice the unavoidable mismatch of NMOS and PMOS transistors in each stage will cause significant upconversion even in a well-designed oscillator.

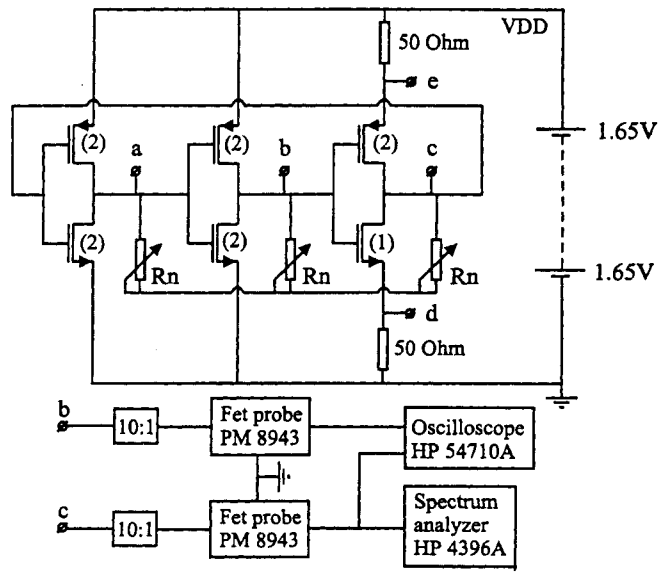

Figure 3. Phase noise measurement setup.

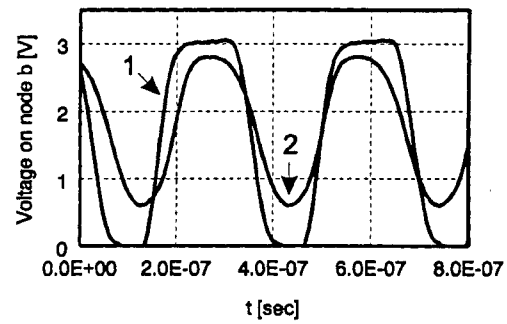

Figure 4. Voltage measured at node b (fig. 3) at two different Rn settings (table 2); VDD = 3V.

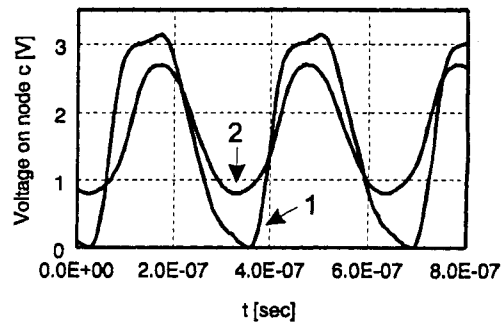

Figure 5. Voltage measured at node c (fig. 3) at two different Rn settings (table 2); VDD = 3V.

As NMOS devices are known to produce much stronger 1/f noise than PMOS devices, the NMOST in stage 3 is expected to be the dominant source of 1/f frequency noise. According to section 2, the OFF voltage of the waveform at node b is thus expected to be important for device noise reduction.

Now we conduct two experiments at different VDD values to realise different current bias conditions: one at VDD=3V (figs. 4,5,6 and table 2) and the other at VDD=4.5V (fig. 7 and table 3). In both experiments we choose multiple settings for Rn to achieve multiple distinct amplitudes. For each of these settings we measure the phase noise spectrum as well as the maximum and minimum voltage levels of the waveform at node b (the minimum level is expected to determine the 1/f noise reduction [2,3]). After each measurement of sideband noise the upconversion efficiency from node c is measured (see section 4).

Using the sideband measurement results obtained with the experimental setup of figure 3, the PSD of phase fluctuations can be calculated from the ratio $L(F_m)$, defined as the noise power $P_{sideband,1Hz}(F_m)$, measured in a bandwidth of 1 Hz at a frequency distance F_m from the carrier, to the carrier power $P_{carrier}$:

$$L(F_m) = \frac{P_{sideband,1Hz}(F_m)}{P_{carrier}}$$

In the sideband frequency region where $L(F_m)<<1$, assuming that amplitude modulation can be neglected, the phase noise PSD $S_{\Delta\phi}$ can be approximated as:

$$S_{\Delta\varphi}(F_m) = 2 \cdot L(F_m)$$

The phase noise PSD is commonly specified as a logarithmic function of $L(F_m)$:

$$10 \cdot \log(L(F_m)) \qquad [dBc / Hz]$$

Figure 6 shows the measured $10\cdot\log(L(F_m))$ behaviour at different oscillation amplitudes for VDD=3V. Table 2 lists the corresponding values of Rn, the oscillation frequency, the maximum and minimum voltage of the waveform at node b, and the carrier power. A smaller Rn leads to a smaller oscillation amplitude and is accompanied by an increase of $1/f^3$ phase noise. As a smaller oscillation amplitude corresponds to a higher V_{GS_OFF}, this trend is apparently consistent with the 1/f noise reduction hypothesis and the results of section 2.

Figure 7 shows the measured $10\cdot\log(L(F_m))$ for biasing at VDD=4.5V, while table 3 lists the corresponding relevant information. Here, at first sight, the trend does not seem to be consistent with the 1/f noise reduction hypothesis: curve 5 with the lowest peak-peak voltage ($2.9V_{pp}$ voltage swing at node b, 1 dBV carrier power) lies in between curves 3 ($4.6V_{pp}$, 5.5 dBV) and 4 ($4.0V_{pp}$, 4.1 dBV). Furthermore, the curves lie much closer together. However, in the next section we will show that after correction for upconversion and effective biasing, the result agrees well with the 1/f noise reduction hypothesis.

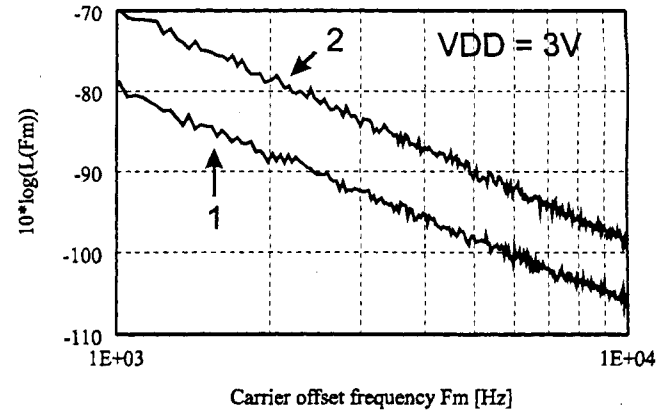

Figure 6. Measured $10\cdot\log(L(Fm))$ at different Rn settings (table 2); VDD = 3V.

Table 2. Parameters for VDD = 3V (figure 4-6).

Curve nr. (Fig. 4-6)	Rn [kΩ]	F_{OSC} [MHz]	$V_{MAX,b}$ [V] (Fig. 4)	$V_{MIN,b}$ [V] (Fig. 4)	$P_{CARRIER}$ (node b) [dBV]
1	15	3.016	3.1	-0.04	2.7
2	2.5	3.274	2.8	0.62	-0.9

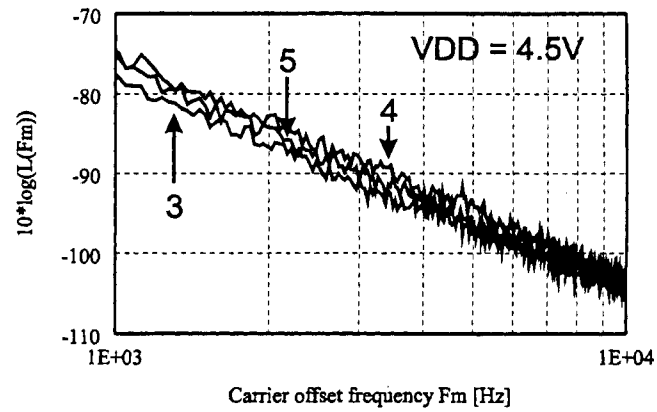

Figure 7. Measured $10\cdot\log(L(Fm))$ as a function of carrier offset frequency at different Rn settings (table 3); VDD = 4.5V.

Table 3. Parameters for VDD = 4.5V (figure 7).

Curve nr. (Fig. 7)	Rn [kΩ]	F_{OSC} [MHz]	$V_{MAX,b}$ [V]	$V_{MIN,b}$ [V]	$P_{CARRIER}$ (node b) [dBV]
3	15	6.169	4.5	-0.10	5.5
4	1.5	7.031	4.2	0.22	4.1
5	0.8	7.938	3.9	0.98	1.0

4. Correction for upconversion efficiency and effective bias level

Changes of the oscillation amplitude may be accompanied by changes of the waveform asymmetry

and may thus affect the upconversion efficiency. Also the effective levels of gate-source bias voltage are affected by the oscillation amplitude. In this section the required corrections for both effects will be examined quantitatively.

Measurement of the upconversion efficiency is carried out by injecting a 10kHz sinusoidal current at node c in the running oscillator and measuring the relative strength of the resulting sideband component at 10 kHz offset from the carrier. More elaborate measurements have shown that the upconversion efficiency from the NMOST in stage 3 in the ring oscillator dominates by more than 10 dB over that of the PMOST in the same stage. As PMOS devices generally produce less 1/f noise than NMOS devices, the measured phase noise can safely be attributed solely to the NMOST. This allows a fair comparison between the baseband noise measurements of section 2 and the 1/f device noise as it will be inferred from the oscillator phase noise measurement results.

The upconversion measurements are performed immediately after each phase noise measurement. Results obtained at VDD = 3V and VDD = 4.5V are listed in the second column of table 4.

Table 4. Correction figures from measured upconversion efficiency and effective V_{GT} ($V_{GT,REF}$=1.0 V).

Curve nr.	Upconversion [dB]	$20\log\left(\frac{V_{GT,EFF}}{V_{GT,REF}}\right)$ [dB]	correction used in fig. 8 [dB]
1	-33.5	1.5	-33.5 + 1.5 = -32.0
2	-28.0	-0.6	-28.0 - 0.6 = -28.6
3	-39.4	8.4	-39.4 + 8.4 = -31.0
4	-39.7	7.3	-39.7 + 7.3 = -32.4
5	-43.9	6.0	-43.9 + 6.0 = -37.9

Next we will establish the corrections on the noise measurements that are required because of changes in the effective gate-source voltage bias at different amplitudes. As argued before, it is allowed to focus on the dominant noise contributor: the NMOST in stage 3. This NMOST produces its maximum noise current during the time interval in which it discharges node c. As the discharging process determines oscillator timing, the noise current of the NMOST in stage 3 is translated into timing jitter (phase noise) just when it is maximal. In the calculation of the device noise it is therefore reasonable to assume an effective steady-state bias voltage at node b which is equal to the flat maximum of the actual oscillation waveform at node b (see fig. 4). Since the PSD of the 1/f noise current in steady-state MOS transistors is roughly proportional to V_{GT}^2 ($V_{GT}=V_{GS}-V_T$), the ratio of the effective bias $V_{GT,EFF}$, to an arbitrarily chosen reference value $V_{GT,REF}$=1.0V has been used to correct for amplitude-dependent biasing. Correction figures in dB are listed in the third column of table 4.

The resulting total correction in dB is shown in the fourth column of table 4. Fig. 8 shows the curves of figs. 6 and 7 after correction. Remarkably, now an *amplitude increase corresponds to a decrease of phase noise*, supporting the hypothesis of intrinsic 1/f device noise reduction. The improvement in phase noise is maximally about 8 dB at a frequency offset Fm of 1KHz and corresponds well with the baseband measurements. It is concluded that a strong agreement has been shown between 1/f device noise as obtained by (1) baseband measurements of switched devices and (2) inference from oscillator phase noise measurements. The remaining differences could be caused by the assumptions about the effective bias level and the use of a first order 1/f noise model.

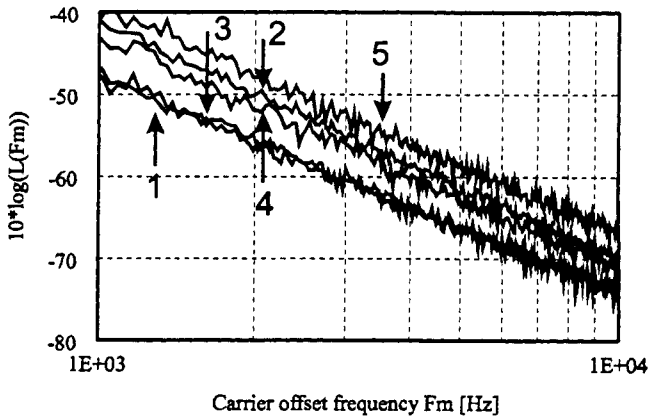

Figure 8. The curves of figures 6 and 7, after correction with figures from table 4.

5. Conclusions

For the first time the implications of 1/f noise reduction in periodically switched MOS transistors on phase noise in CMOS ring oscillators have been explored quantitatively. Measurement results, corrected for the actual upconversion and effective bias show an improvement of the close-in phase noise of about 8 dB at 1KHz frequency offset from the carrier at 4.5 dB increase in carrier power. It is concluded that maximising the oscillation amplitude can help to reduce the close-in phase noise of CMOS oscillators.

6. References

[1] A. Hajimiri and T.H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 2, February 1998, pp. 179-194.

[2] I. Bloom and Y. Nemirovsky, "1/f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation", *Applied Physics Letters*, Vol. 58 No. 15, April 1991, pp. 1664-1666.

[3] S.L.J. Gierkink *et al.*, "Reduction of the 1/f noise induced phase noise in a CMOS ring oscillator by increasing the amplitude of oscillation", accepted for publication at the *ISCAS '98*, Monterey, June 1998.