A Wide-Band Injection-Locked Frequency Divider in 0.18um CMOS

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Abstract— **In this paper we propose a novel inductor-less Injection-Locked Frequency Divider (ILFD) that can make divisions with ratios 2,4,6 and 8 with wide locking ranges. Fabricated in a digital 0.18µm CMOS process the divider can operate up to 15 GHz. The measured locking ranges of the divider for division ratios 4 and 6 are 1.6 GHz and 1.1 GHz wide respectively. The current consumption of the divider is 3.8 mA operating at 1.8V supply. The active area of the chip is 100x67µm^2.**

Keywords— Frequency; frequency conversion

I. INTRODUCTION

Low Power and high frequency integrated wireless transceivers in CMOS technology can enable important applications. In wireless transceivers, RF synthesizers are in general of phase-locked loop (PLL)-based architectures, and consume a significant portion of the total power budget. In a RF PLL crucial components are the voltage controlled oscillator (VCO) and the prescaler. Main concerns in VCO-design are low phase noise and low power consumption. Important design criteria for the frequency divider are low power consumption and high frequency-capability. In this context, the need for high performance RF prescalers in deep sub micron CMOS technology is the motivation of this work.

High-speed CMOS frequency dividers can be categorized into two groups; static divider and injection-locked frequency divider (ILFD) [1]. Static dividers are capable of operating with wide-bandwidth; however the power consumption increases drastically along with the increments of operating frequency. On the contrary, ILFDs can operate at relatively higher frequencies at the expense of a narrow locking range [1]. The division capability of the ILFD with ratios higher than two brings an important power consumption and speed advantage to ILFD over static dividers.

In this paper, we propose an inductor-less ILFD that can operate at high frequencies with low power consumption. The most important property of the proposed ILFD is the wide-band locking range, even for division ratios higher than two. The proposed ILFD is based on *injection locking* of a *static frequency divider*. Simulation and experimental results have verified that an ILFD based on injection locking of a static divider can have relatively wide-locking range.

In the next section injection-locked and static dividers will briefly be discussed. In section 3 the proposed ILFD is presented and measurement results are given in section 4. Finally, in section 5 the performance of the proposed ILFD is compared with the recently reported ILFDs.

II. INJECTION-LOCKED AND STATIC FREQUENCY DIVIDER

A. Injection-Locked Frequency Divider

In 1939 Miller proposed a regenerative frequency divider based on injection-locking phenomenon [4]. The main idea of his concept of frequency division was to create an oscillation at the sub-harmonic of the input signal. A simplified architecture for injection-locked frequency divider (ILFD) is given in Fig. 1 [3]. It consists of an injector (e.g. mixer), and a low-pass filter. Miller's divider can achieve division ratios greater than two by using a frequency multiplicative element in the feedback loop as indicated by the block $X(N-1)$ in Fig. 1. This frequency multiplicative element does not have to be explicit and can represent non-linearities present in the circuit (e.g. the non-linearity of the mixer). The

mixer multiplies the input signal (ω_{in}) with the output signal (ω_{out}) and generates $\omega_{in} \pm (N-1)\omega_{out}$, assuming linear operation of the mixer. The high frequency component, $\omega_{in} + (N-1)\omega_{out}$ is filtered out by the LPF. If the total gain and the phase shift in the loop are respectively 1 and multiples of 2π , the following equality will be satisfied:

$$\omega_{in} - (N-1)\omega_{out} = \omega_{out} \quad \Rightarrow \quad \omega_{out} = \omega_{in} / N \tag{1}$$

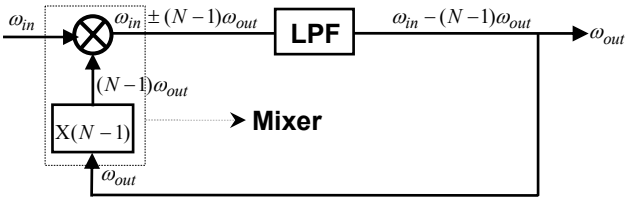

Fig. 1 Injection-locked frequency divider architecture

When the loop is locked the output frequency (ω_{out}) will be synchronized with sub-harmonics of the input signal (ω_{in} / N) [1]. The output (ω_{out}) follows (ω_{in} / N) within the locking range of the divider when there is an input signal with sufficient amplitude. In the case of a lack of any input signal the divider oscillates at its self-oscillation frequency that is mainly determined by the circuit parameters. In [1] the locking range ($\Delta\omega_R$) of an ILFD is expressed as:

$$\Delta\omega_R = \gamma \bullet \alpha_N (\omega_c / 2Q) V_{in} \tag{2}$$

where α_N is the N[th] order harmonic coefficient of the injector, γ is injection efficiency, ω_c is the oscillation frequency, and Q is the quality factor of the frequency selective network. Injection efficiency (γ) is an important parameter limiting the highest division ratio of an ILFD. As the division ratio increases the input frequency also increases and the injection efficiency decreases, hence the locking range degrades.

B. Static Divider

In Fig. 2 a static frequency divider circuit is given. The divider employs two D-latches in a master-slave configuration with negative feedback. Each latch has two transistors for sensing (M3 and M4 in the master and M3* and M4* in the slave), two cross-coupled transistor pairs for latching (M5 and M6 in master and M5* and M6* in slave) and two clock transistors (M1 and M2 in the master and M1* and M2* in the slave). When the CLK is in high state the master D-latch is in the sense mode whereas the slave D-latch is in the latch mode. When the CLK is in low state the roles are exchanged.

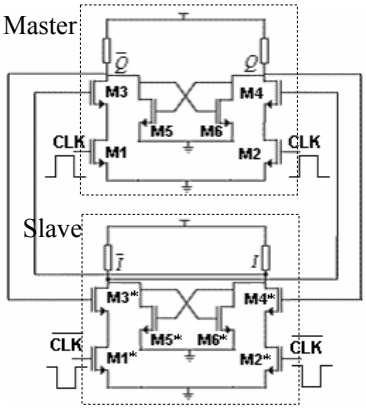

Fig. 2 A Static frequency divider circuit diagram

In Fig. 2 the clock transistors beneath the cross-coupled transistor pairs are removed, which is different than in conventional latch topologies, such as given in [6]. This leads to an increase in the gate-source voltage and thus in the gm of M5, M6, M5* and M6*. Increase in gm allows decreasing the width of the cross-coupled transistors, thereby decreasing the parasitic capacitance at the output nodes, and thus enabling the divider to reach higher frequencies.

Static dividers have very wide bandwidth. They can operate down to arbitrarily low frequencies. The maximum frequency of operation is generally limited by the delay of the D-latches. Cascading more static dividers' stages in order to increase the division ratio increases the total power consumption of the prescaler. In ILFDs the division ratio is related to the non-linear behavior and therefore not necessarily demands extra power consumption. This property gives an important advantage to ILFD in terms of speed and power consumption over static dividers. However, this advantage of ILFDs has practical value only when it can be combined with a reasonable locking range.

III. THE PROPOSED ILFD

Static dividers can also have a self-oscillation frequency as in ILFDs. The chosen size of the cross-

coupled transistor has an important effect on this. As the latch transistor size is reduced, the self-oscillation frequency increases, but the locking range is reduced [6]. By increasing the latch size the locking range of a static divider can be increased. Therefore, when a static divider is used as a starting point to realize an ILFD the presence of the latches in the circuit topology can give an important advantage in obtaining wide-locking range even for frequency divisions higher than two.

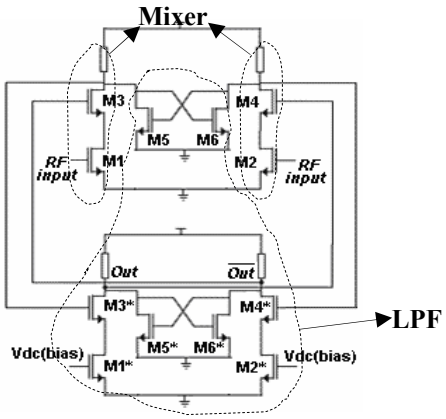

Fig. 3 Proposed ILFD circuit diagram

With a simple modification the static divider given in Fig. 2 can be converted into an ILFD, as illustrated in Fig. 3. Only a biasing dc voltage is applied to the gates of M1* and M2* in Fig. 3. The RF input signal is being applied to the gate of M1 and M2 (biasing of M1 and M2 is not shown for the sake of simplicity). The transistor pairs M1&M3 and M2&M4 form the mixer and the rest of the circuit acts as a low-pass filter.

As the latch size increases the locking range of the proposed ILFD increases too. In obtaining wide bandwidth, the dimensioning of M1 and M2 as well as the cross-coupled transistors is important. For synchronization of the output signal even at small amplitude of the input signal the transconductance of M1 and M2 transistor pair was kept large. This required large transistor sizes for M1 and M2 and thus increased power consumption and sensitivity to the DC input level.

It is possible to use one silicon realization of the proposed divider as ILFD or static divider. This feature of the proposed divider will be useful in programmable architectures such as software defined radio.

IV. Measurement Results

The proposed divider was fabricated in a digital 0.18μm CMOS process with five layers Al-metal. The chip microphotograph is seen in Fig. 4 and measures 1600x600 μm^2. The size is mainly determined by the pad frame and not by the active area (shown with dotted square, 100x67μm^2). All measurements were performed on wafer. The represented measurement data has been corrected for losses caused by cables. The proposed ILFD has a differential amplifier to drive the external 50 Ω loads. 50 Ω on chip resistors were placed between the substrate and gate of M1 and gate of M2 for input matching. Excluding the current consumption due to input matching resistors and the differential pair at the output, the proposed ILFD consumes only 3.8mA current at 1.8V supply. In Fig. 5 the input (4 GHz) and output (2 GHz) waveforms of the proposed ILFD are shown for a divide by 2 mode (using an Agilent 86100A oscilloscope).

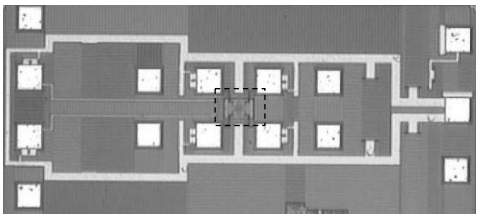

Fig. 4. Chip micrograph of the proposed ILFD

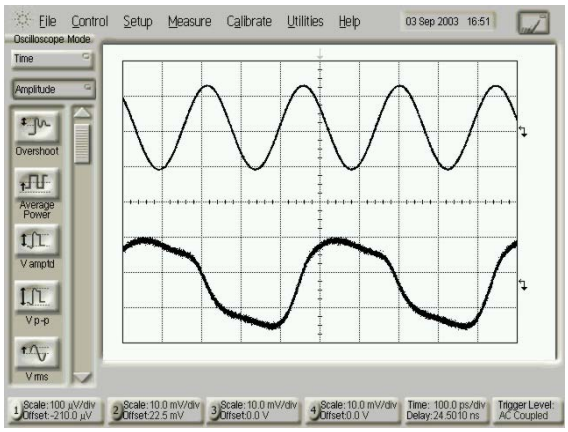

Fig. 5. Input (4 GHz) /Output (2 GHz) signals of the proposed ILFD.

Fig. 6 shows the measured sensitivity curves for division by 2 and 4 with a locking range of 2GHz and 1.6GHz respectively. In Fig. 7 the same data is provided for division by 6 and 8, revealing a locking range of 1.1GHz and 0.25GHz, respectively. Therefore, while changing the input frequency, the circuit switches from a divide by 2 mode to a divide by 8 mode, as expected from theory. The divider has a self-oscillation frequency of 1.8GHz and operates up to 14.65 GHz as shown by

Fig. 7. By increasing the Vdc biasing voltage the current consumption is increased from 3.8mA to 4mA and the proposed ILFD operates up to 15.1 GHz. Note that the high frequency performance of the proposed ILFD comes without use of inductors.

The measurements indicate an input power around 0 dBm for division ratios higher than 2, which is in the same range as in [1, 5]. This means that the VCO has to deliver an output swing of 220 mVrms in order to drive the divider. Although this is a high value, state-of-the-art VCOs can handle this. As explained in section 2, when the input frequency increases the injection efficiency degrades and hence locking range decreases, a behavior clearly visible from the measurement results in Fig. 6 and 7.

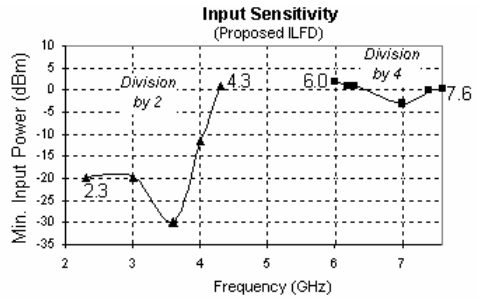

Fig. 6. Measured ILFD locking range for division by 2 and 4

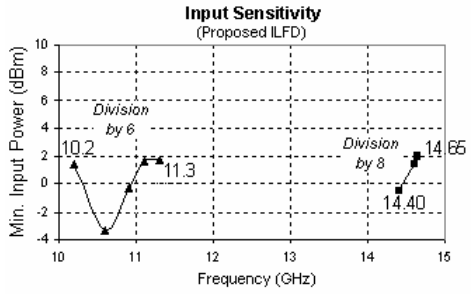

Fig. 7. Measured ILFD locking range for division by 6 and 8

To measure the phase noise performance of the proposed circuit, a HP83731B signal source has been used together with an Agilent E4448A phase noise spectrum analyzer. As shown in Fig. 8 the phase noise of the 3 GHz input signal is measured as -91 dBc/Hz at 10 kHz offset. Driven by this signal the proposed ILFD has decreased the phase noise to -97 dBc/Hz at 10 kHz offset (Fig. 8).

In order to better demonstrate the benefit of the proposed ILFD over static dividers, a static divider with the topology given in Fig. 2 has also been implemented in the same technology as the ILFD. The static divider consumes 12mA and can operate up to 12 GHz as can be seen by the measured input sensitivity (Fig. 9). The lack of sensitivity below 2GHz is caused by the limited slew rate of the sinusoidal input signal and increased loss in the hybrid coupler.

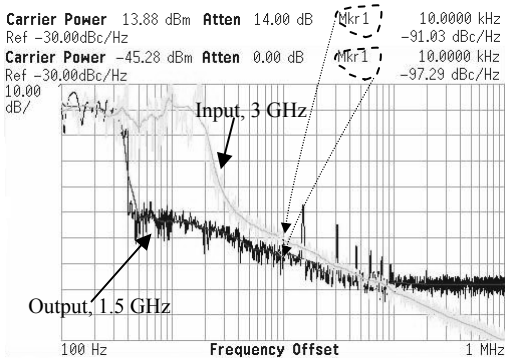

Fig. 8. Measured phase noise vs. carrier offset frequency of the signal generator driving the proposed ILFD and the output of the proposed ILFD

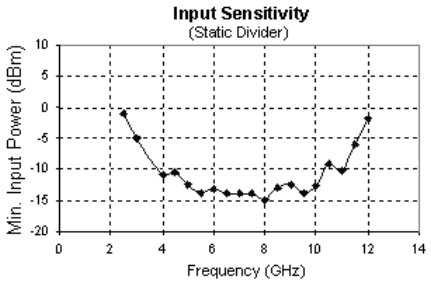

Fig. 9. Measured input sensitivity curve of the static frequency divider

V. CONCLUDING REMARKS

We proposed an inductor-less injection-locked RF frequency divider that can operate at high frequency with low power consumption. The most striking property of the proposed ILFD is the wide-bandwidth (1.6GHz for division by 4 and 1.1GHz for division by 6).

In Table 1 the main features of some of the recently published ILFDs and the proposed ILFD are given. As evident from Table I the proposed ILFD has wider bandwidth than other four ILFDs. If (Locking Range/ Max. Input Freq.) is taken as figure of merit, this figure of the proposed ILFD (for division by 4) is at least 2 times higher than the rest of the ILFDs in Table I.

The locking range obtained in [2] is close to locking range of the proposed ILFD (for division by 6) however the power consumption of [2] is almost two times higher.

The min. required input powers for the proposed ILFD are in reasonable magnitude compared with the other ILFDs given in Table I.

TABLE I
Comparison of the summary of the proposed ILFD and some of the recent published priori art ILFDs

	[1]	[3]	[5]	[2]	Proposed ILFD	
Locking Range (GHz)	**0.01**	**0.06**	**0.2**	**1**	**1.1**	**1.6**
Max. input freq. (GHz)	18.2	2.8	1.8	10.0	11.3	7.6
Power diss. (mW)	1.75	0.99	1.75	12.60	6.84	6.84
Min. input power (dBm)	5	-5	7	?	2	0
Division ratio	5	4	2	8	6	4
CMOS (μm)	0.25	0.24	0.5	0.18	0.18	0.18

Although the 6.8mW power consumption of the proposed ILFD is less than one third of the 21.6mW power consumption of the static divider, the proposed ILFD can reach to higher frequencies. Operating at high frequencies with reasonable bandwidth, the proposed ILFD can easily be used instead of static dividers in many applications.

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