Transmission Line Model Testing of Top-Gate Amorphous Silicon Thin Film Transistors

N. Tosic[1], F. G. Kuper[1,2], T. Mouthaan[1]
[1]MESA+ Research Institute, University of Twente, The Netherlands,
[2]Philips Semiconductors, Nijmegen, The Netherlands.
Email: N.Tosic@el.utwente.nl

ABSTRACT

In this paper, for the first time Transmission Line Model (TLM) characterization is used to analyze ESD events in amorphous silicon thin film transistors (α-Si:H TFT). It will be shown that, above an ESD degradation threshold voltage, deterioration of electrical characteristics sets in, and that above another ESD failure threshold voltage, dielectric breakdown occurs. Electrical simulations of an α-Si:H TFT confirm creation of positive interface charges as being the most likely cause of the deterioration process. Two failure modes have been identified by failure analysis.

1. INTRODUCTION

Due to the presence of a glass insulating layer, electrostatic discharge (ESD) is a hot topic in display manufacturing. To date, only a few papers that treat ESD in hydrogenated amorphous silicon thin film transistors (α-Si:H TFTs) have been published concerning ESD protection circuit design [1,2] or machine model testing [3]. Instabilities of the threshold voltage (V_T) induced by DC gate bias stress have been more extensively investigated. Two mechanisms have been found to contribute to V_T shift after applying prolonged gate bias stress to α-Si:H TFTs: trapping of charge in the gate dielectric and creation/removal of metastable silicon dangling bond states [4]. The mechanisms depend on material differences [5]. In the case of high electric field across the gate insulator (>2 *MV/cm*), instabilities were attributed to a secondary instability such as field induced interface state creation [6]. Concerning voltage stress on drain, Kaneko et al. [7] showed that prolonged drain voltage up to 30 *V* does not influence V_T. The problem of the instabilities induced by ESD stress on drain/source is still open. This paper will provide new insights concerning this issue.

2. EXPERIMENTAL

The devices used in this work were top gate (staggered) symmetrical α-Si:H TFTs (Fig. 11). To test ESD robustness of the TFTs a high voltage pulse (zap) is applied on drain of a grounded gate TFT by means of Transmission line model (TLM) [8]. In crystalline MOS transistors this voltage pulse is transformed into a current pulse. In TFTs however, due to low conductivity of α-Si:H, the voltage pulse is not converted into a current pulse. During TLM stress on drain, an α-Si:H TFT is staying off. The only current under TLM stress is sub-threshold current. This level of current is very low, such that it is not possible to measure it by oscilloscope current probe. Because of loss of information about current, TLM had to be modified adding a parameter analyzer used for the characterization of TFT between TLM stress pulses, as shown in Fig. 1. The TLM pulse length is set at 500 *ns* (from *t*=100 *ns* to *t*=600 *ns* in Fig. 2). Such long ESD pulse is a kind of worst

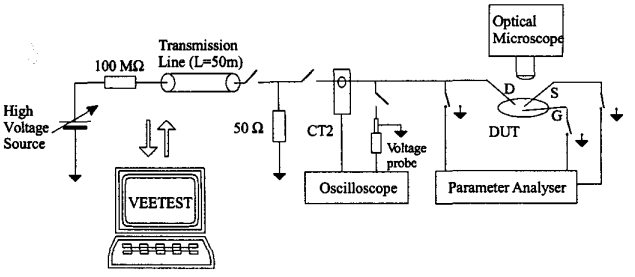

FIGURE 1. ELECTRICAL SCHEME OF THE MODIFIED TLM SET-UP

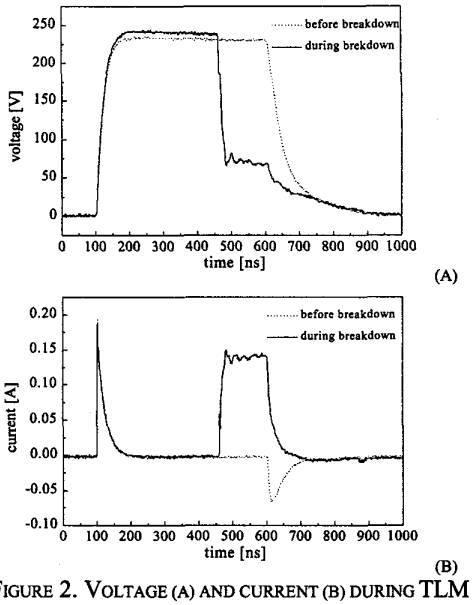

FIGURE 2. VOLTAGE (A) AND CURRENT (B) DURING TLM

case ESD pulsed voltage. It is introduced because of large capacitances of the TFT structure, which make rise and fall time of voltage and current TLM pulses to be very long (100 *ns*).

In order to follow degradation development, the transfer characteristics $I_D(V_G)$, drain output $I_D(V_D)$ characteristic and drain/gate leakage currents were measured between TLM pulses. TLM stress was applied on the drain of TFT and increased in steps up to breakdown, while the gate and source were grounded. The breakdown criterion was defined by a sharp increase of TLM current, accompanied by decreasing of TLM voltage. An example of the voltage and current

curves during two TLM pulses, one just before, and one containing a breakdown is shown in Fig. 2a and 2b respectively. The current burst shown in Fig. 2b is the indicator of catastrophic dielectric breakdown (equivalent of "second breakdown" in crystalline MOS TLM curve).

3. DEGRADATION ANALYSIS

If a TLM stress is higher than the "threshold of degradation" (V_{THDEG} ~ 180 V), electrical characteristics change. The transfer characteristic shifts to the negative side and the slope of the characteristic increases. A set of monitored $I_D(V_G)$ curves is shown in Fig. 3.

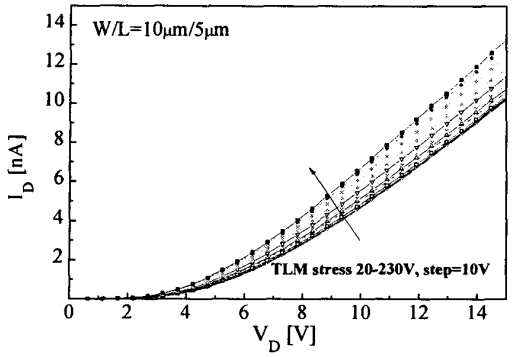

FIGURE 3. TRANSFER CHARACTERISTICS MONITORED DURING TLM.

V_T is derived from the intersection of the slope of linear transfer characteristics with x-axis. It is found that once the TLM voltage exceeds the threshold of degradation, V_T decreases linearly with applied voltage (Fig. 5). As it is shown in Fig. 4, V_T decrease varies from -0.1 V up to -5 V, depending on channel length (L) and width (W) of transistor. Appearance of the negative shift of V_T can be connected with both mechanisms, the creation of positive states (breaking the bonds) in the α-Si or near the interface and due to the charge trapping in SiN.

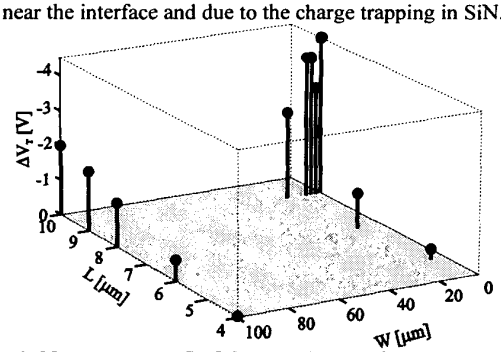

FIGURE 4. V_T SHIFT AFTER TLM SERIES (FROM 20 V UP TO 250 V) AS FUNCTION OF W, L.

Besides V_T, the transconductance is also derived from the slope of linear transfer characteristics. An increase of electron mobility is assumed and will be further explained by the analysis that follows. In α-Si TFTs, the main carriers are electrons whose room-temperature mobility is typically 0.3-0.6 cm^2/Vs. The dependence of the mobility with temperature is given by [9]:

$$\mu_n = \mu_0 \frac{N_C \cdot kT}{n} \cdot e^{\left(\frac{-E_a}{kT}\right)} \qquad (1)$$

where μ_0 is extended state electron mobility, N_C is density of states at the mobility edge, n is total electron density, and E_a is the activation energy (~1.5 eV), which reflects the tail distribution of the amorphous silicon. We suppose that shift of V_T and shift of μ are independent processes, although they can be correlated. We assume that these positive interface states help to move the current flow closer to interface α-Si/SiN and further from the bottom interface of α-Si/SiO_2, where it is more confined in higher mobility part of the band-gap. There is also another possible mechanism which can to explain observed change in the transfer characteristic's slope, assuming that electron mobility is constant and that created positive interface states attract an inversion layer that extends the drain, resulting in a shortening of the effective length of the transistor [10]. To avoid this uncertainty, the slope change will be presented through relative change of transconductance:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \mu \cdot C \cdot V_{DS} \qquad (2)$$

Stepped lowering of V_T implies stepped accumulation of positive charges. Irreversibility of this degradation is observed and confirmed by means of repeated TLM experiment under the same conditions. To investigate whether the ESD induced degradation is permanent, repeated TLM stresses were applied in the following way. In the first TLM series, V_{TLM} is stepped from 20 V up to 250 V, when the series is stopped. After 100 *min* of pause (with all electrodes grounded) the second TLM series is repeated (V_{TLM} =20-250 V). This time V_T and g_m stay inert during TLM stress. After pause of 1000 *min* the third TLM series is applied (V_{TLM} was increased from 20 V up to dielectric breakdown). Same as in the previous case, no degradation is found for voltages up to 250 V. Finally, when V_{TLM}>250 V, then degradation of V_T and g_m continues with the same rate (1 V/100 V) as in the first TLM series (Fig. 5).

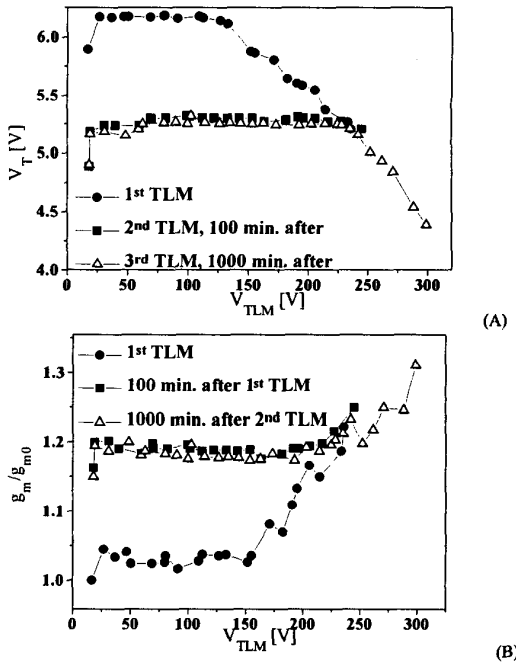

FIGURE 5. THRESHOLD VOLTAGE (A) AND TRANSCONDUCTANCE (B) BEHAVIOUR DURING THE FIRST AND THE SECOND REPEATED TLM SERIES

It should be noted that after the first TLM stress the "turnaround phenomenon" of the threshold voltage shift is noticed. This phenomena for the low negative gate bias is already known in the literature [11] and it appears when the negative threshold voltage shift caused by the hole trapping in the SiN gate dielectric are positively compensated by the states created near the conduction band in the α-Si film. This process of state creation should be distinguished from the creation of states under high electric field.

In order to distinguish whether these charges are located in the gate dielectric or at the gate dielectric/amorphous silicon interface, the sub-threshold slope of the transfer characteristics (Fig. 6) is analyzed. It appears that sub-threshold slope $S=dV_G/d(\log I_D)$ increases during TLM stressing, which can be result of interface state creation. Assuming that created defects in amorphous silicon are located at the gate dielectric/amorphous silicon interface, the effective defect density D_{it} can be related to the sub-threshold slope [12] as:

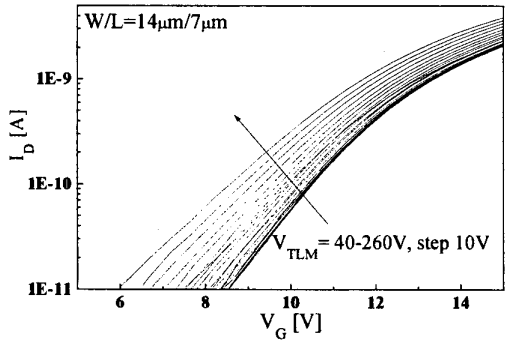

FIGURE 6. SUB-THRESHOLD SLOPE CHANGE DURING TLM.

$$S = \ln 10 \frac{kT}{q}\left(1+\frac{q^2 D_{it}}{C_i}\right) \qquad (3)$$

where q is the electron charge, k is the Boltzmann constant, C_i is gate capacitance per unit area and T is absolute temperature. The calculated values of the density of interface states vary between TFT's. For example, after a TLM series up to 250 V they are estimated to be in the order of $10^{12}\ cm^{-2}eV^{-1}$.

The sub-threshold slope increase during TLM stressing implies defect state creation. In order to determine where these defect states are located within volume of a TFT a repeated symmetrical experiment is performed as follows. After the first TLM series (V_{TLM}=50-250 V, step=10V) is applied on the source of the TFT, the second TLM series is applied on TFTs drain. In the second TLM series the V_T decrease and g_m increase continuously from the same "threshold of degradation" voltage, when compared to the first series (Fig. 7). Apparently, repetitive TLM stresses on one side of the transistor up to the highest previous level do not create additional damage, whereas an additional TLM series with the same low voltage on the other terminal does create additional damage. *It means that if TLM stress is applied on drain, the defect states are non-equally distributed along the channel; they are located close to the drain of TFT.*

An additional proof that TLM stress induces creation of fast interface states is obtained from high frequency $C(V)$ measurements. Parasitic capacitances of the drain and the source are measured before and after a TLM series up to 200 V applied on drain. The position of the Fermi level in an undoped α-Si, as used in this investigation, is shifted closer to the bottom of the conduction band. Therefore, tested

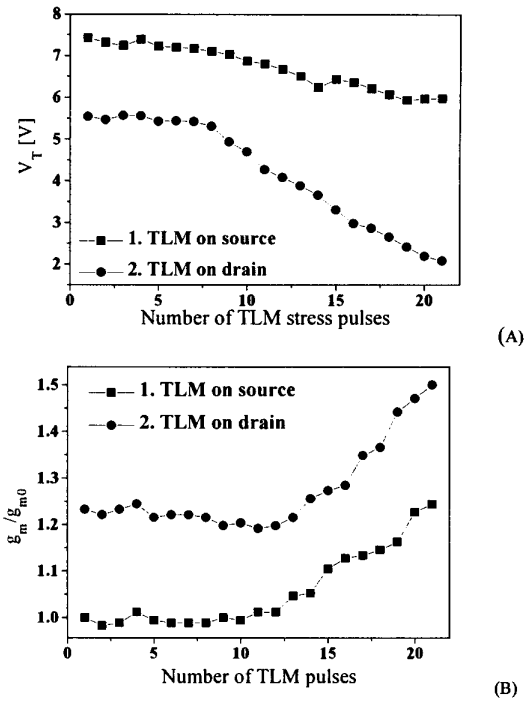

FIGURE 7. THRESHOLD VOLTAGE (A) AND TRANSCONDUCTANCE (B) VARIATION UNDER TWO REPEATED SYMMETRICAL TLM SERIES (FIRST SERIES ON SOURCE, SECOND ON DRAIN).

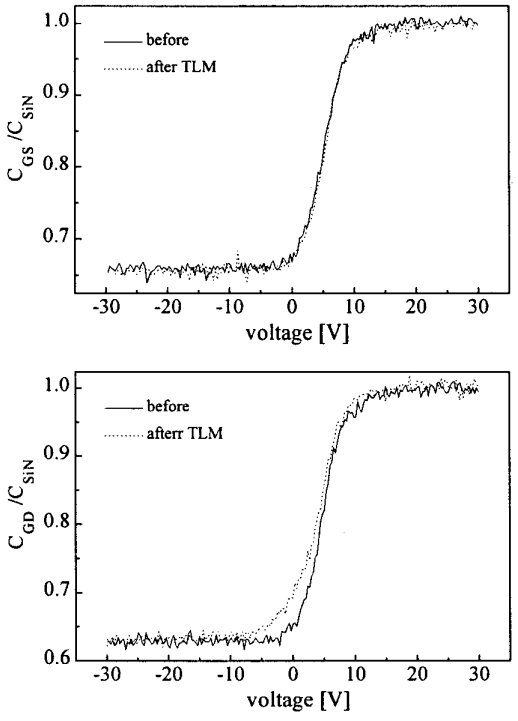

FIGURE 8. NORMALIZED HIGH FREQUENCY CAPACITANCE VS VOLTAGE IN THE G-S (A) AND G-D (B) MODES

TFTs are undoped and n-type (Fig. 8). During the TLM series the TFTs threshold voltage is decreased by 0.5 *V*, and the transconductance is slightly increased. As it is shown in Fig. 8a, the high frequency *C(V)* curves of parasitic capacitance of source before and after TLM stress are the same, meaning that TLM stress did not induce any damage at the source side. In contrast, the high frequency *C(V)* curve of the parasitic capacitance at the drain side (Fig. 8b) after TLM stress is stretched-out to negative side and degraded as compared with the curve monitored before the TLM stress.

Furthermore, the leakage current monitored on the gate between TLM pulses do not show any change under TLM stress, implying that the gate dielectric is not worn-out (Fig.9).

Due to the lowering of V_T and increasing of transconductance, the drain output characteristics $I_D(V_D)$ monitored between TLM pulses increases. In addition, the leakage current of drain measured between TLM pulses shows an increase, described by an exponential function (Fig. 9):

$$I_{Dleak} = I_{Dleak0}\left\{1 + e^{\frac{V_{TLM} - V_{THDEG}}{Const.}}\right\} \qquad (4)$$

For the fitting curve shown in Fig. 9, the fitting parameters are I_{Dleak0}= 3.7 10^{-9} *A*, V_{THDEG}= 265 *V*, *Const* = 52.

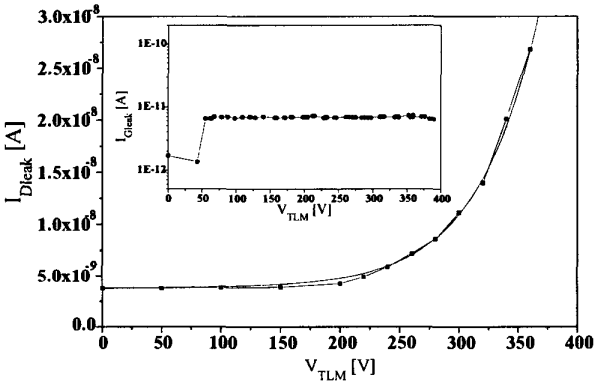

FIGURE 9. DRAIN AND GATE LEAKAGE CURRENT BEHAVIOUR DURING TLM

4. MODELLING

Firstly, the gradually distributed electric field across the gate dielectric is simulated. If threshold voltage of degradation is applied on drain, electric field close to drain has value ~ 5 *MV/cm*. This electric field level moves from drain to source, since TLM stress is stepped.

The assumption that a TLM stress creates positive interface charges, giving rise to sub-threshold slope and lowering V_T, is validated by electrical simulations. The assumed model says that the new created interface charge, induced by electric field, widens with every step along the interface from the drain to the source (Fig. 11). Transfer characteristic of the top gate amorphous silicon transistor is simulated by Silvaco simulation tools, taking into account created interface charge. Initially, the transfer characteristic is simulated without any interface charge. At each simulation step a constant quantum of interface charge is added along the length from drain to source (Fig 11). Charge parameters have been optimized, leading to: length of the cube x=0.2μm and fixed charge density quantum of $1 \cdot 10^{12}$ cm^{-2}. The result of the simulations is presented in Fig. 12. It can be seen that it describes experimentally measured characteristics, which are shown in Fig. 3.

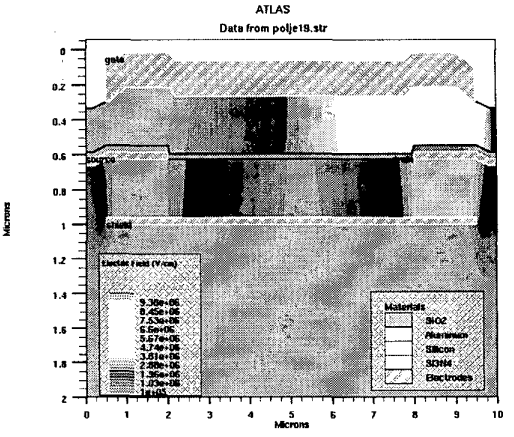

FIGURE 10. ELECTRICAL FIELD UNDER V_D=190V.

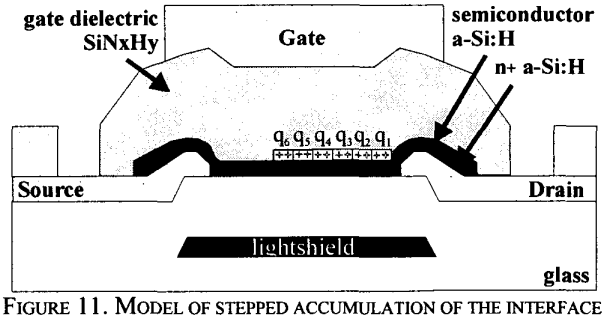

FIGURE 11. MODEL OF STEPPED ACCUMULATION OF THE INTERFACE CHARGES.

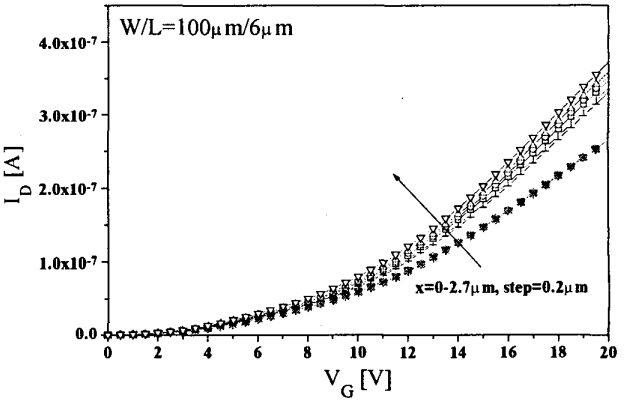

FIGURE 12. SIMULATED TRANSFER CHARACTERISTICS.

5. ANNEALING

In order to remove created interface traps, TFTs are thermally annealed. The procedure of annealing for both variations that will be presented is as follows: first thermal annealing, then the first TLM series (when threshold voltage and transonductance were monitored), a

second thermal annealing (with repeated conditions of first annealing), the second TLM series (V_T and g_m monitored). Two variations of annealing are carried out: dry annealing in the ambient of vacuum, and wet annealing in the ambient of N_2, with presence of hydrogen, which has an important role in this amorphous silicon device.

First variation: Dry annealing

After initial annealing and the first TLM series, TFT is annealed at 200°C for 1 hour in vacuum, with all electrodes open. Analyzing the behavior of V_T and g_m under second TLM series, it can be seen that they are not inert under TLM stress. It means that the annealing is sufficient to de-trap, at least partly, the created traps. During the second TLM series after thermal annealing, transonductance is completely recovered. It returns to the starting value, and behaves similarly (same threshold of degradation and rate) as during the first TLM series (Fig. 13b). It proves that created interface states, responsible for increasing of transconductance, are removed by thermal annealing at the 200°C. The threshold voltage value did not recover to the starting value (Fig 13a). It gives information that processes of change in transonductance and threshold voltage have different activation energies. Process of recovering of transconductance has lower activation energy than process of recovering of the threshold voltage. Possible explanation is that heat treatment removes only created fast states from the interface, but that the energy is not enough to remove deep states in the gate dielectric.

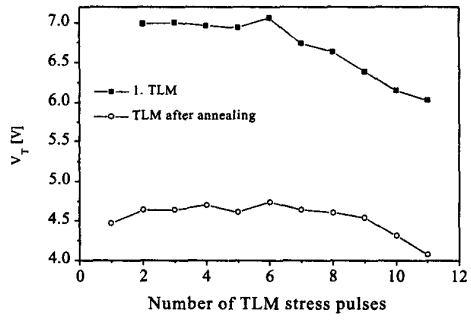

FIGURE 13. EFFECTS OF DRY THERMAL ANNEALING (200°C) ON V_T (A) AND g_m (B).

Second variation: wet annealing

A completely different result is obtained by wet open-circuit thermal annealing in the atmosphere of N_2 with the presence of H_2 at 250°C for 30 min. The results are shown in Fig. 14. As shown in Fig. 14a, the threshold voltage after thermal annealing is increased (in contrast to the dry annealing), while transconductance (Fig. 14b) is almost completely recovered, although it does not return exactly to the starting value. Both V_T and g_m under the second TLM series are active, they degrade in the same way as under the first TLM series, which implies that created states are removed from the α-Si-SiN interface. The difference in V_T shift during wet and dry annealing comes from the presence of hydrogen. Annealing without presence of hydrogen gives negative, while annealing in the presence of hydrogen gives positive shift, as hydrogen plays important role in the process of de-trapping holes.

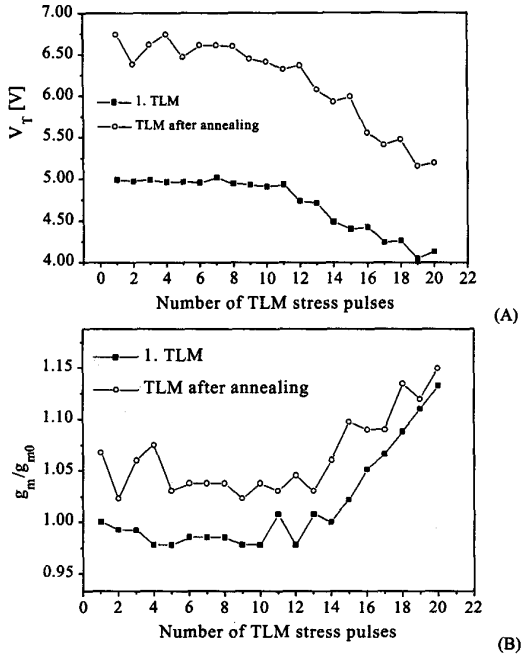

FIGURE 14. EFFECTS OF WET THERMAL ANNEALING (250°C) ON V_T (A) AND g_m (B).

6. HARD BREAKDOWN ANALYSIS

It is found that the ESD failure threshold under stepped TLM stress depends on design parameters (L, W). For a given W, failure threshold increases with L, as shown in Fig. 14.

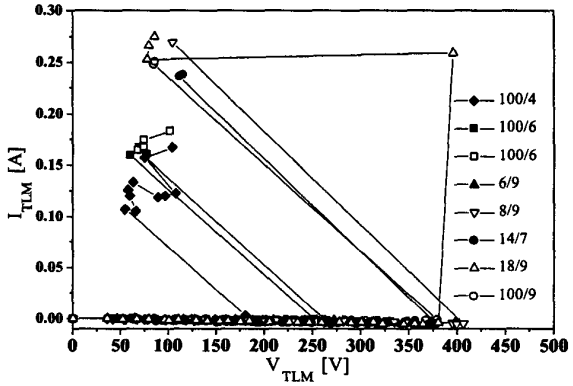

FIGURE 14. TLM I-V CURVES FOR DIFFERENT TFT'S

It is obvious that the breakdown voltage of the catastrophic breakdown does not depend on the threshold voltage shift. As they are not correlated, they must be induced by two different degradation mechanisms. TFT's with L=4μm fail at 170V and ΔV_T<1V, and some TFT's with L=9μm fail at 370V and ΔV_T>5V.

Failure analysis

All failed devices were inspected by means of SEM failure analysis. It is found that failure mechanism is dielectric breakdown, appearing in two modes:

1. *Breakdown via lightshield*: current path is created through the glass substrate. A number of melt filaments are found at both drain/gate and source/gate edges (Fig. 16a). This failure mode is identified in 10% of inspected devices.
2. *Gate dielectric breakdown:* it is manifested as large rupture of gate dielectric. This is the most often-found failure mode (90%). Center of the rupture is located at the edge of drain under the gate electrode (Fig 16b). The size and shape of the rupture implies that explosion is accompanied by an increase of the temperature. The hydrogen's motion speeds-up by high temperature and consequently the gate dielectric blows-up. It leads to the conclusion that the temperature is locally increased at the edge drain/gate, i.e. at the drain side of the channel.

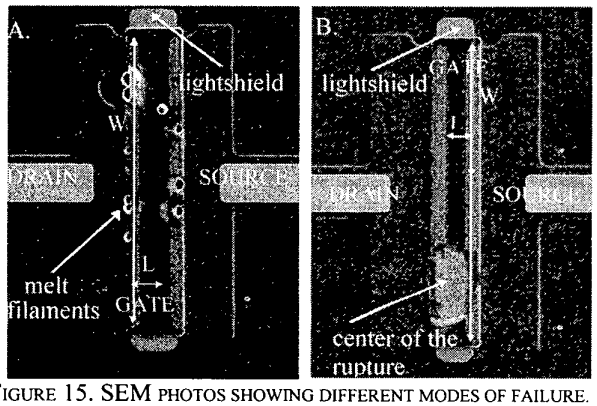

FIGURE 15. SEM PHOTOS SHOWING DIFFERENT MODES OF FAILURE.

7. CONCLUSION

In conclusion, degradation of TFT's under TLM stress was investigated. If TLM voltages are higher then 200 *V* "threshold of degradation" then V_T starts to decrease, and sub-threshold slope and transconductance start to increase. The change in sub-threshold slope is an indication that there are defects, such as interface states, created. It was experimentally proved that created interface states are located close to drain, if ESD stress is applied on drain. The effect of the stepped creation of positive interface states on electrical characteristics, observed in the experiment, is confirmed by simulation. Several annealing experiments are shown, proving that created traps can be annealed by open-circuit thermal annealing. Failure analysis showed that responsible failure mechanism is dielectric breakdown appearing in two modes: via lightshield and gate dielectric.

ACKNOWLEDGEMENT

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