19.5 A 90µW 12MHz Relaxation Oscillator with a –162dB FOM

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Both ring oscillators and relaxation oscillators are subsets of RC oscillators featuring large tuning ranges and small areas. Figure 19.5.1 shows a typical relaxation oscillator with a capacitor and two switched current sources. Such relaxation oscillators have two advantages with respect to ring oscillators: 1) they have a constant frequency tuning gain; and 2) their phase can be read out continuously due to their triangular (or sawtooth) waveform. A major disadvantage of practical relaxation oscillators is their poor phase-noise compared to ring oscillators [1,2,4].

The $1/f^2$ phase-noise performance of oscillators can be compared using the FoM definition given in Fig. 19.5.3 [1]. Navid et al. have shown that at 290K thermodynamics limits the FoM of ring oscillators and relaxation oscillators to -165.3dB and -169.1dB, respectively [2]. Interestingly, they have also shown that the FoM of practical ring oscillators is generally better than about -160dB, while the FoM of practical relaxation oscillators is about 10dB worse. So in theory relaxation oscillators can be better, but in practice they are not. Part of the explanation is given in [2]; the noise added by the comparator, which is present in relaxation oscillators (cmp_{osc} in Fig. 19.5.1) but not in ring oscillators, increases the phase-noise. We will show below that filtering this noise by exploiting a switched-capacitor discharge mechanism, the FoM of a practical relaxation oscillator can be as good as the FoM of ring oscillators.

Figure 19.5.2 shows the new relaxation oscillator. As in Fig. 19.5.1, I_1 charges capacitor C_1. However, C_1 is not grounded, but connected across an OTA, and the discharge process exploits a switched capacitor, C_2, which is reversed periodically. The operation of the circuit is described in the next sentences. The initial voltage across C_2 is $V_{ref,OTA}$. At t_0, I_1 is charging C_1 at a constant rate via the OTA, resulting in a linearly decreasing voltage V_-. At t_1, V_- crosses $V_{ref,osc}$ and cmp_{osc} reverses C_2. C_2 is then being charged from $-V_{ref,OTA}$ to $+V_{ref,OTA}$ by I_1 and the OTA. At t_2, C_2 is charged to $+V_{ref,OTA}$ and, as a result, a fixed charge packet equal to $2C_2V_{ref,OTA}$ has been subtracted from C_1. $V_3 = V_+ - V_-$ is a sawtooth waveform. Subtracting this fixed charge packet filters out the noise of the oscillator comparator. The operation is illustrated in Fig. 19.5.3, which shows the control signal X, V_3 and the output of the comparator cmp_{out}, V_{out}, is also shown, which produces an edge whenever voltage V_3 reverses polarity. Suppose now that cmp_{osc} is noisy and C_2 is reversed at t_4 instead of at t_3. Although the duty cycle of V_{out} is changed (at t_5), the *active edge* of V_{out} at t_6 *is unaffected and so is the phase-noise*. This filter technique is similar to the anti-jitter circuit (AJC) technique used in open-loop jitter filters [3]; note that we apply a switched-capacitor circuit to subtract the charge packet, which is very power-efficient.

Filtering out the noise of the oscillator comparator has two consequences: 1) the power dissipated by the oscillator comparator and its reference can be reduced without deteriorating the phase-noise; and 2) the two remaining contributions to the $1/f^2$ phase-noise are the white noise of the charging and discharging mechanisms. It can be shown that the resulting FoM of such a relaxation oscillator is given by the equation in Fig. 19.5.3, where k is the Boltzmann constant, T the absolute temperature and P_{core} is the power dissipated in the oscillator core: $P_{core} = V_{DD}I_{core}$ (in W). I_1 is the charge current and ΔV_1 and ΔV_2 (also shown in Fig. 19.5.2) are the voltage headroom reserved for the charging and the discharging mechanisms, respectively. For a good FoM we want ΔV_1 and ΔV_2 to be high and about equal, while we also want a large V_3 swing to reduce the phase-noise floor contribution of cmp_{out}.

In Fig. 19.5.1 this is not possible, since the sum $\Delta V_1 + \Delta V_2 + \Delta V_3$ has to fit in the supply V_{DD}. In Fig. 19.5.2 the voltage swing of V_3 mainly occurs at the output of the OTA, leaving the full V_{DD} for $\Delta V_1 + \Delta V_2$.

Instead of reversing C_2, C_2 could be discharged to ground before connecting it to V_+, which would be easier to implement. Reversing C_2 has some advantages though: 1) ΔV_2 can be doubled without increasing power dissipation; and 2) the time allowed for settling is doubled (C_2 needs to settle only once instead of twice every period). By reversing C_2, both a near optimal and a practical choice would be $\Delta V_1 = \Delta V_2 = 2V_{DD}/3$. In the case of a sawtooth waveform, the total core current, I_{core}, is at least $2I_1$ in steady state ($= I_1 + \bar{I}_2$); the discharge current has to be equal to the charge current. This implies a theoretical FoM of 163.2dB at 290K, which is similar to that of ring oscillators.

Figure 19.5.4 shows the actual implementation of the switched-capacitor relaxation oscillator. I_1 is implemented by a resistively degenerated PMOST to increase control linearity and decrease thermal noise. M_2 could be biased continuously by I_2, but this would worsen the FoM dramatically. Only when C_2 is reversed, S_2 is closed briefly (during $t_{osc}\cdot I_1/I_2$) and I_2 discharges C_1 through C_2 during this time. When S_2 is opened, C_2 starts settling to $V_{ref,OTA}$. Note that the accuracy of the charge packet with which C_1 is discharged is only a function of the settling of C_2; noise on I_2 does not affect the accuracy. $V_{ref,OTA}$ is implemented as the gate-source voltage of M_2 biased at current I_1.

The relaxation oscillator of Fig. 19.5.4 has been designed in a standard 65nm CMOS process (V_{DD} = 1.2V). The main design choices are: $V_{ref,OTA} = V_{DD}/3$, $V_{ref,osc} = V_{DD}/6$, $\Delta V_1 = \Delta V_2 = \Delta V_3 = 2V_{DD}/3$, $I_1 = \bar{I}_2 = I_2/4 = 25\mu A$, $C_1 = C_2 = 2.5pF$. The measurement buffers, oscillator comparator and its reference are designed to consume about 2.5mA, 10µA and 5µA, respectively. The circuitry to switch I_2 and reverse C_2 reliably consumes about 5µA. As a result, f_{osc} = 12.5MHz, $I_{core} = 2.8I_1 = 70\mu A$. According to the equation in Fig. 19.5.3, the FoM is expected to be -161.7dB at 290K, which is similar to the -161.4dB predicted by simulation. Simulation also predicts a lower oscillation frequency and lower peak voltages than calculated, mainly due to the gate-source and gate-drain capacitances of M_2.

Figures 19.5.5 and 19.5.6 show the measurement results. The circuit is measured using a battery supply. It is fully functional and the performance is similar for supply voltages between 1.0 and 1.3V. Unfortunately, S_2 is closed for somewhat less than $t_{osc}\cdot I_1/I_2$, so the waveform is slightly deformed; this can be easily corrected in a re-design. The measured FoM is -162dB, which is similar to both analysis and simulation results. Ten samples have been measured and all have similar FoMs.

Measurements illustrate the advantages of a relaxation oscillator: the phase can be read out continuously and the tuning range is both large and linear. Measurements also show an outstanding phase-noise performance; the FoM is at least 7dB better than state-of-the-art relaxation oscillators [1,2,4] and similar to state-of-the-art ring oscillators [2]. Note that we include all the core current consumption. As it seems to be increasingly more difficult to reach the minimal FoM for ring oscillators in smaller CMOS technologies [2], relaxation oscillators could well become the preferred choice of RC oscillators in low-power applications, like sensor networks.

References:

[1] S. L. J. Gierkink, A. J. M. van Tuijl, "A Coupled Sawtooth Oscillator Combining Low Jitter with High Control Linearity," *IEEE J. Solid-State Circuits*, pp. 702-710, June 2002.

[2] R. Navid, T. H. Lee, R. W. Dutton, "Minimum Achievable Phase Noise of RC Oscillators," *IEEE J. Solid-State Circuits*, pp. 630-637, March 2005.

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[4] L. B. Oliveira, et al., "Experimental Evaluation of Phase-Noise and Quadrature Error in a CMOS 2.4 GHz Relaxation Oscillator," *ISCAS*, pp. 1461-1464, 2007.

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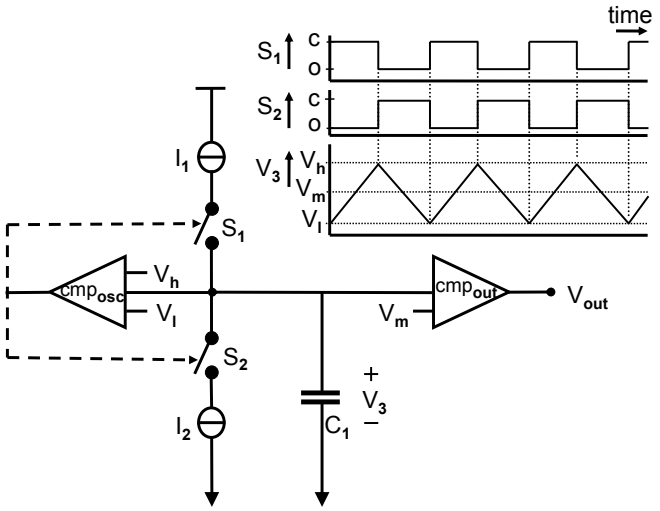

Figure 19.5.1: Relaxation oscillator based on current sources (which is part of the general class of relaxation oscillators based on resistors, like in [2]).

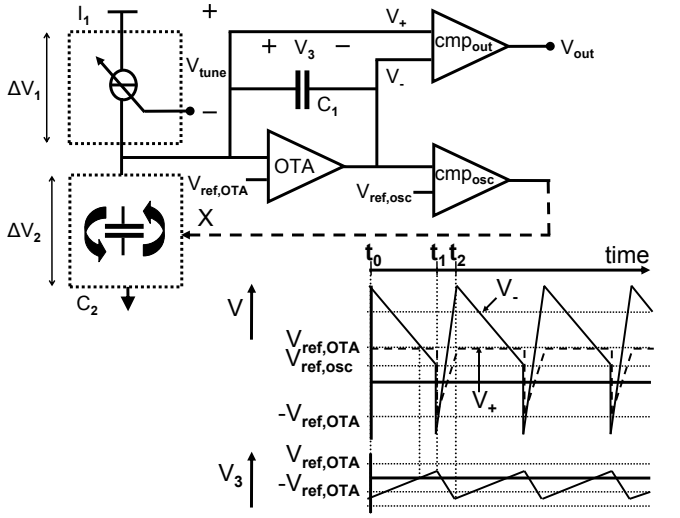

Figure 19.5.2: Block-level schematic of a switched-capacitor relaxation oscillator.

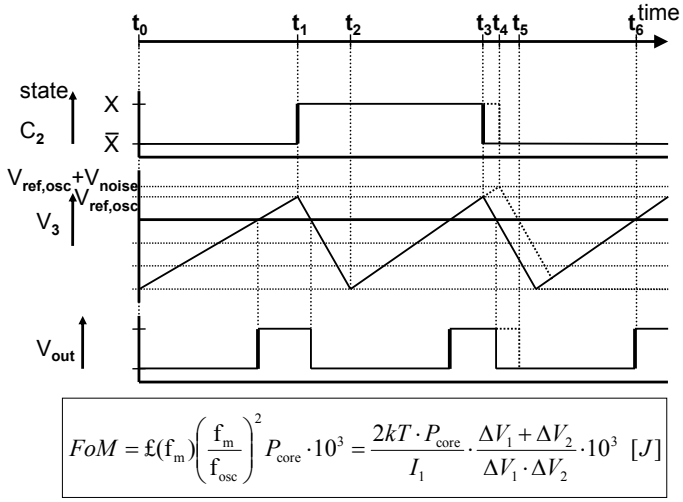

Figure 19.5.3: Technique to filter out the noise of the oscillator comparator (cmp_{osc}).

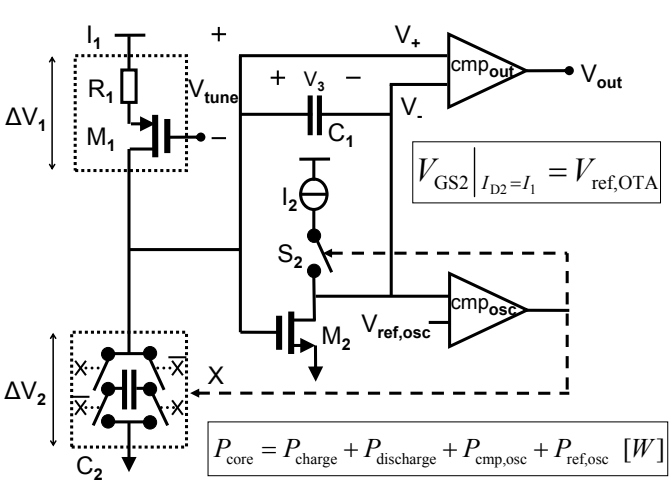

Figure 19.5.4: Actual implementation of a switched-capacitor relaxation oscillator.

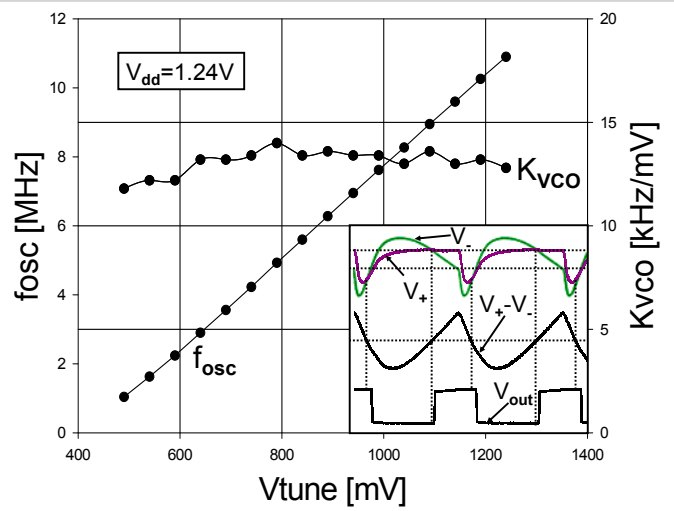

Figure 19.5.5: Measured waveforms, frequency tuning range and frequency tuning gain (Agilent DSO6104A oscilloscope and LeCroy AP033 active differential probe, R&S FSP spectrum analyzer).

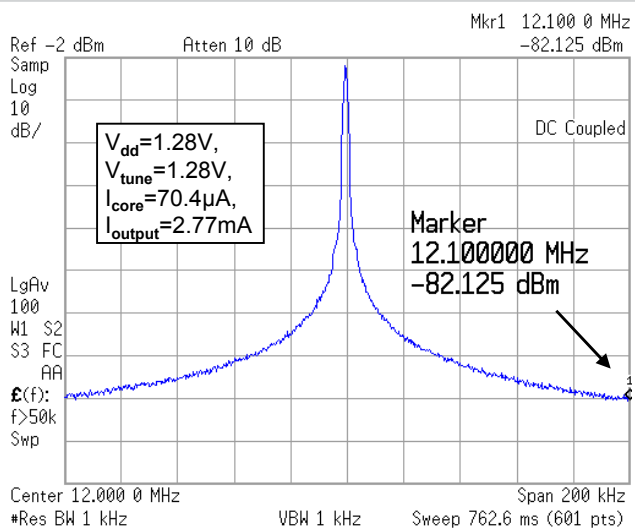

Figure 19.5.6: Measured phase-noise (Agilent E4440A spectrum analyzer, Keithley 2000 multimeter).

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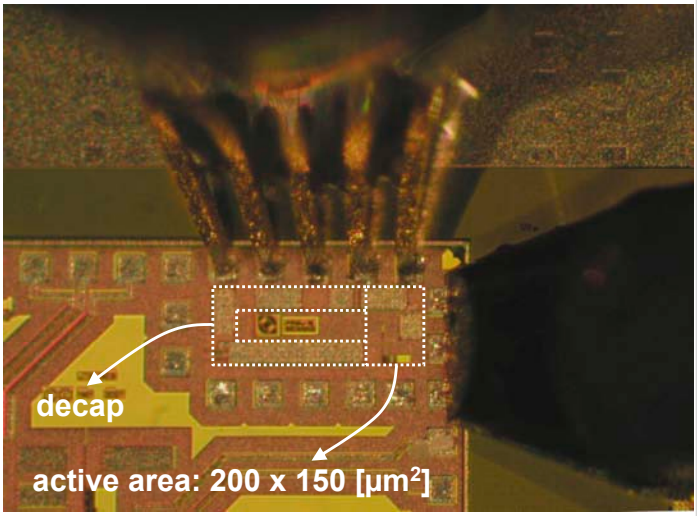

Figure 19.5.7: Die micrograph of 65nm CMOS design.

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