MESA+ Institute for Nanotechnology

Silicon Ridge Nanofabrication by Advanced Edge Lithography for Sub-10 nm NIL Applications

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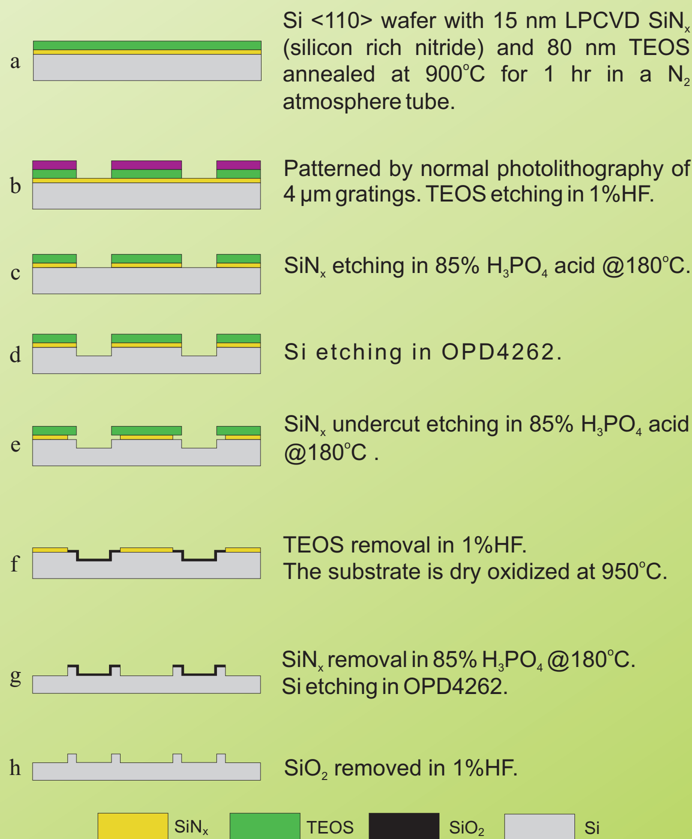
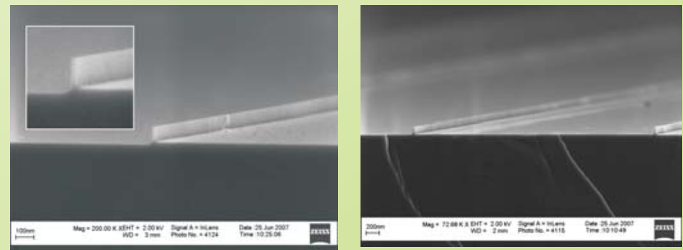
Introduction

A new nanofabrication scheme is presented to form stamps useful in thermal nanoimprint lithography (T-NIL). The stamp is created in <110> single crystalline silicon using a full-wet etch-procedure including local oxidation of silicon (LOCOS) and employing an adapted edge lithography technique (detailed review of edge lithography can be found in reference [1]) on top of conventional photo-lithography. Ridges down to 10 nm in width have been produced. The silicon ridges have no inbuilt stress and are therefore less fragile than previously fabricated oxide ridges [2,3]. The ridge sample is used as a template in T-NIL and a full 100 mm wafer size imprint has been successfully carried out in both polymethyl-methacrylate (PMMA) and mr-I 7010E polymer. Moreover, the imprinted pattern in PMMA is subsequently transferred into a device wafer.

Experimental



Si Nanoridges

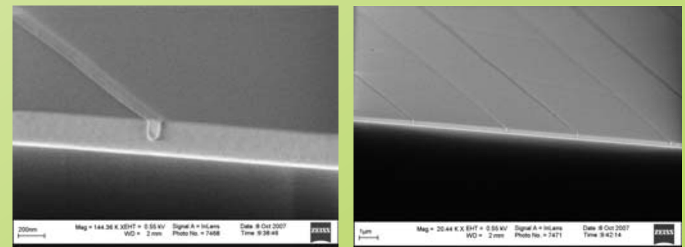


Si nanoridge with a depth of 100 nm and width down to 10 nm.

An 'overview' of Si nanoridges.

Nanoimprint

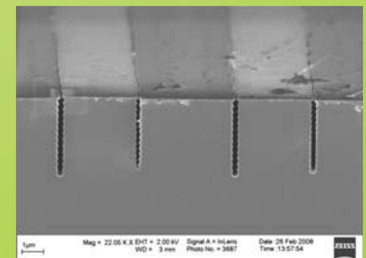
To facilitate demolding, before imprint, the wafer template is treated with 1H,1H,2H, 2H-perfluorodecyltri-chlorosilane from a gas phase under vacuum condition in a desiccator. The imprint process is performed onto a device wafer coated with an imprint polymer, both mr-I 7010E and PMMA, using an Obducat T-NIL machine.



SEM pictures of imprint in mr-I 7010E

Pattern Transfer

The grating pattern is transferred from PMMA into the silicon device wafer. The scallops are caused by the pulsed mode RIE procedure (SF_6/C_4F_8) and can be reduced by proper tuning of the etch tool.



Acknowledgment

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References

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