

A Multi-Band, High Bandwidth, Short Duration Linear Chirp Generation IC for Phased-Array Applications

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Abstract—This work presents a fully integrated multi-band frequency synthesizer that is capable of creating wide-band linear frequency sweeps of very short duration. The main aim is to create a flexible waveform generation system, requiring distribution of a low frequency reference rather than RF signals. By using a phase-locked loop, frequency multiplication (rather than shifting) occurs. This allows for a narrow band and low frequency reference signal, allowing digital reference generation and thus providing a large degree of flexibility. Chirps with a bandwidth of 1 GHz (in X-band) and duration as short as 10 μ s can be created. The chip can be operated in either pulsed or CW mode. The small external size of the package, which measures 5x5 mm², means that local RF generation is possible even in X-band arrays with small antenna element pitch.

Index Terms—Phase locked loops, Phased arrays, Ultra wide-band radar, Signal generators, BiCMOS integrated circuits,

I. INTRODUCTION

Pulse-Doppler phased-array radar systems generally use a centralized signal generator that produces a pulsed waveform with very high spectral purity. This signal is up-converted and distributed (or vice versa) over the active antenna aperture. For future phased-arrays with a high level of reconfiguration or with multiple waveforms that are simultaneously transmitted, such as MIMO systems, this approach poses strong constraints [1]. In view of these systems, sources that can be integrated at individual antenna element level are required, locked only to a central frequency or timing reference for coherency reasons.

In this work, a system is presented which can serve as a fully integrated RF source for a single array element. Where frequency up-conversion is often achieved by means of mixers, we propose to use a phase-locked loop instead. This has the advantage of multiplying, rather than shifting, the input (reference) frequency. This means that the reference signal can be narrow band, as well as relatively low frequency. This means that these signals can be created digitally with high flexibility. In the most flexible case each chip would have its own DSP, allowing distribution of a single, constant frequency, digital clock while providing a fully configurable array. Another advantage of this approach is that it is no longer required to generate and distribute a large number of RF signals.

The IC can generate signals in X-band, covering 7.2 to 12.2 GHz. In this band it can create chirps with durations down to 10 μ s and bandwidths of up to 1 GHz with an RMS frequency error of 3.088 MHz. By means of frequency division (naturally occurring in the PLL's divider) signals in C-, S- and L-band can be created too, with proportionally lower

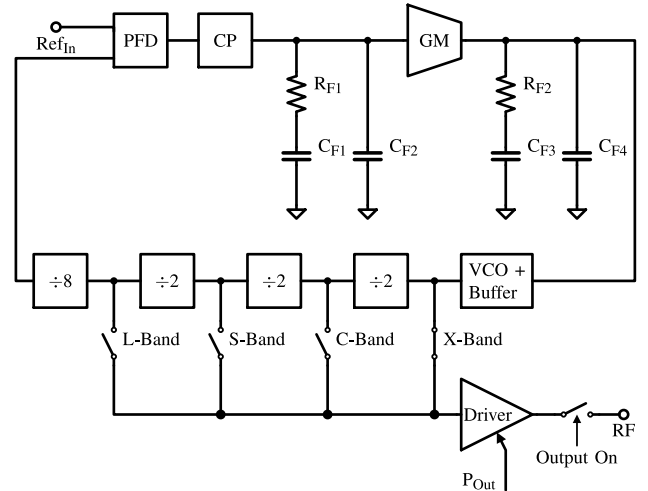


Fig. 1. System Architecture

bandwidth and frequency error. It features an output driver which can deliver a differential signal with up to 4.9 dBm into a 100 Ω load (dropping to -0.7 dBm at the highest output frequency). This driver can also fully disable the output, allowing for the generation of pulsed signals.

This paper is divided into five sections. Section II describes the design on a system-level. Measurement results are given in section III. This section is divided into some general results, a subsection treating chirp linearity and a subsection giving FMCW and range-Doppler results. A comparison with other work is made in section IV. The final conclusions are treated in section V.

II. SYSTEM OVERVIEW

A block level overview of the system can be found in figure 1. This figure depicts a phase-locked loop, which is a feedback system which operates on phase. The reader will recognize a PLL with one extra filter stage. This means one extra integrator in the loop filter compared to most PLLs. The system depicted here therefore of type III, with three integrators in the loop (two in the filter and one in the conversion of control voltage to output frequency, which is the time-integral of phase, by the VCO). In terms of dynamic behavior, a type II system can track a signal with first order behavior with no static error and a type III system, can do the same for a second order signal. This means that, ideally, this

PLL can track a signal with second order phase versus time characteristics without static errors (perfect linear frequency ramp).

The system can create frequency chirps in several frequency bands. It has two VCOs, which are designed to cover the X-band with an overlap of over 1 GHz to allow wideband chirps without switching from one VCO to the other. As can be seen in figure 1, the output can alternatively be connected to one of three divider outputs, dividing the aforementioned frequency range by two, four or eight. This allows operation in C-, S- or L-band. The total division factor of the divider is 64, thus a reference signal between 125 MHz and 187.5 MHz is required to cover the full X-band.

The signal is then fed to a differential output driver which can be set to any one of 16 possible output power levels (on a linear voltage scale for ease of implementation) and which provides 50Ω on both outputs (100Ω differentially). This termination is resistive in order to provide large bandwidth. The driver can also be switched off completely in order to create a pulsed output, functionality which is depicted as a switch in the output in figure 1. The output driver was designed to deliver -18 dBm to 6 dBm differentially.

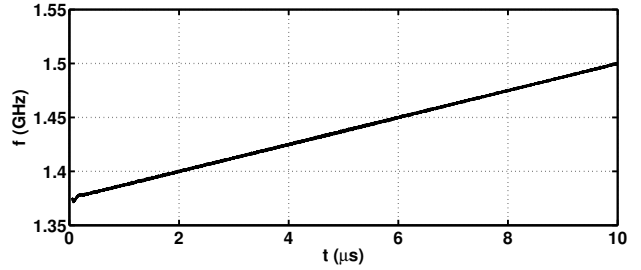
Readers who are interested in some of the circuit aspects of this work are referred to [2], which describes the actual implementation.

III. MEASUREMENT RESULTS

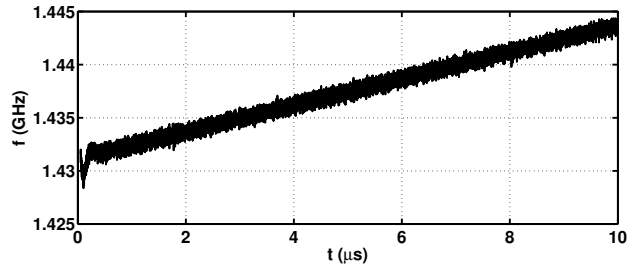
Measurements have been performed in order to verify the functionality of the IC. The ultimate frequency range over which the VCOs operate is 7.2 GHz to 10.1 GHz for the first VCO and 8.8 GHz to 12.2 GHz for the second, an overlap of 1.3 GHz. The output measured output power was -17.9 dBm to 4.9 dBm in the lower frequency bands. This value drops to -22.6 dBm to -0.7 dBm for frequencies high in the X-band. Since the IC is in a sealed package, the output cannot be measured directly at the bondpads. However the simulated bandwidth of the PA is over 16 GHz, thus it is expected that this drop is mainly caused by the bondwires and the first section of the transmission lines on the test PCB, which were shaped to fit to the IC package.

A. Chirp Linearity

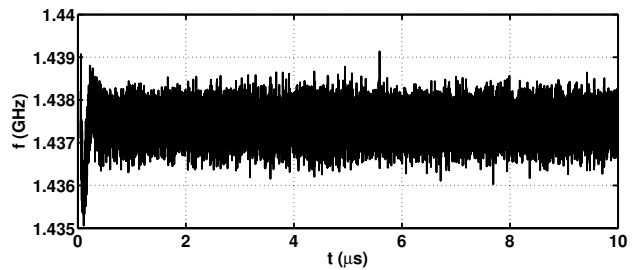
The ability of the IC to generate fast frequency ramps has been verified. An example of this for a static signal and two chirps with a pulse length of $10 \mu\text{s}$ is depicted in figure 2. These measurements were made by sampling the L-band output of the IC with a 40 GSa/s oscilloscope and post processing in Matlab to extract the frequency. A band-pass filter with cut-off frequencies at 1 GHz and 2 GHz and 60 dB out of band suppression was used to suppress any out of band spurs which give rise to frequency errors. The RMS frequency error for both chirps was found to be 386 kHz and that of the constant frequency was 391 kHz, confirming the independence of frequency error of chirp rate. That been said, there are still some spurs left inside the frequency band of the chirp, which are believed to be the main cause of the remaining



(a) 125 MHz in $10 \mu\text{s}$



(b) 12.5 MHz in $10 \mu\text{s}$



(c) Constant Frequency

Fig. 2. Frequency vs. Time

frequency errors. The higher frequency bands could not be measured directly with available equipment, but the errors can be inferred from the errors at L-band by simple multiplication (inverse of the frequency divider operation). This gives an RMS frequency error of 3.088 MHz for a bandwidth of 1 GHz in X-band.

B. FMCW and Range-Doppler Measurements

FMCW measurements have been performed by connecting the output of the chip to a programmable delay line and mixing the output of this line with the non-delayed output of the chip. Figure 3 shows the results of some of these measurements. Figure 3a shows the beat frequency spectrum of a $375 \mu\text{s}$, 300 MHz bandwidth sweep in L-band applied to a delay line that simulates a target at 28 km. Figure 3b shows the result for the same chirp in S-band with a target at 8 km and figure 3c shows the result of a $375 \mu\text{s}$ chirp over 900 MHz in X-band, also with a target at 8 km. Note that in order to create a bandwidth of 300 MHz in L-band, a bandwidth of 2.4 GHz is required in X-band. This is only possible using the high

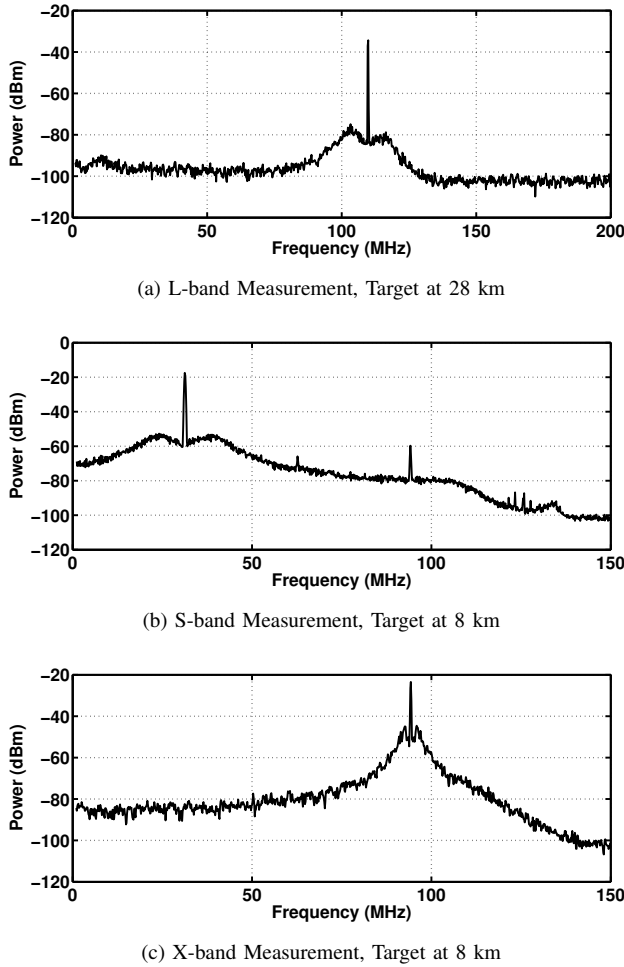


Fig. 3. FMCW Measurements

frequency VCO and therefore only in the 8.8 GHz to 12.2 GHz range. It will also give rise to more spurs in the band of the chirp. This is no problem for FMCW range measurements, as the spurs will always be at f_{Ref} distance from the beat note, but it will be detrimental for pulsed signals where the bandwidth of the filter will now include several spurs.

The phase noise of the PLL can be clearly seen in these figures, with skirts around the peak that indicate the bandwidth of the loop at that particular frequency. The additional peaks at 60 MHz and 90 MHz in figure 3b are caused by the second and third order harmonics. These give rise to (small) signals that sweep at two and three times the sweep rate of the fundamental, and thus produce two and three times the frequency difference after a fixed delay. The third order harmonic is larger than the second order harmonic because the output of the chip approaches a square wave in the lower frequency bands.

Several X-and L-band FMCW measurements were logged using a sampling oscilloscope. These data were used to create range-Doppler representations of the measurements. The first step in this process is to take an FFT over the data in each sweep, giving frequency (and thus range) information. This

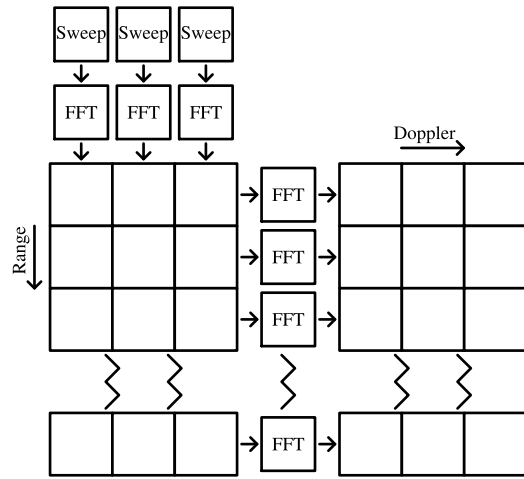


Fig. 4. Graphical Representation of Range-Doppler Processing

result is stored in a 2-D matrix where each column contains the range data for one sweep. Subsequently FFTs over the rows of this matrix are taken, creating a new matrix with range information along its columns and Doppler information along its rows. A graphical representation of this procedure is displayed in figure 4.

A slow moving target will give rise to a negligible Doppler shift and thus small range error during one sweep. Its changing distance to the radar will however give rise to small phase shifts over a longer period of time. Such phase shifts become evident after range-Doppler processing, producing a peak in a non-zero Doppler bin. This also means that a range-Doppler plot displays the phase stability over several frequency ramps when a static target is emulated, such as was done here. A linear phase drift will cause the signal to be in a non-zero Doppler bin, and a random phase drift will cause it to be smeared out over several Doppler bins.

Figure 5 shows the results of range-Doppler processing over 32 sweeps in both S- and X-band (targets again at 8 km). For both cases the peak is narrow, containing significant power in three range and three Doppler bins after which it falls off rapidly. The fact that the response is not smeared out along the Doppler axis indicate good phase correspondence between subsequent sweeps. Note that the range is less than 8 km. This is mainly due to extra delays in the reference path of the setup that were not calibrated out, as these measurements were performed to characterize the IC and not to build an actual radar. The plot for the X-band configuration shows more noise than the S-band setup. This is due to the extra frequency (and hence phase noise) division that occurs when lower bands are output. It also has a spur like component along the range axis (which is hidden behind the main lobe in figure 5b, the origin of which is as yet unknown).

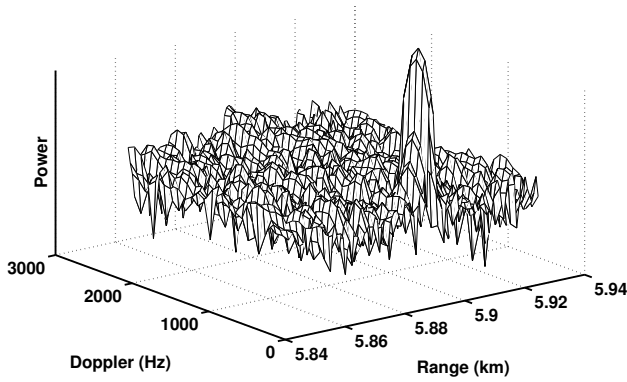
IV. COMPARISON TO OTHER WORK

As the authors are not aware of previous publications of pulsed systems with this level of integration on silicon, a

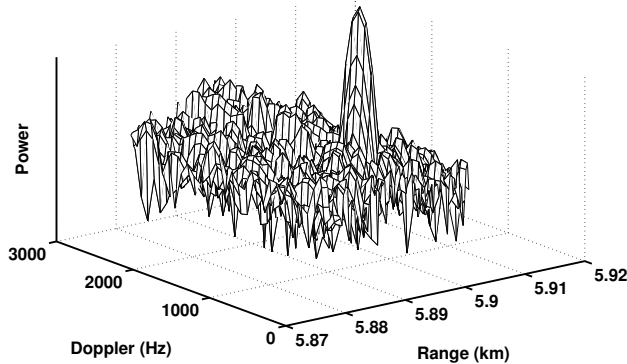
TABLE I
COMPARISON TABLE

Type	[3] FMCW	[4] FMCW	[5] FMCW	[6] FMCW	[7] FMCW	This Work Pulsed	
Technology	65 nm CMOS	90 nm CMOS	65 nm CMOS	SiGe Bipolar ^d	Board	250 nm BiCMOS	
Active Area	1.05	6.8	1.7	3 ^a	?	3	mm ²
Supply Voltage	1.2	1.2	1.2	5 ^a	?	2.5	V
Power Consumption	188 ^b	406 ^b	152	488 ^a	?	380 ^c	mW
Output Frequency	75.6 to 76.3	78.1 to 78.8	82.1 to 83.8	67.2 to 92.8	76 to 78	7.2 to 12.2 ^d	GHz
Chirp BW	0.7	0.7	1.5	25.6	2	1 ^d	GHz
Fractional Bandwidth	1.3	1.3	2.3	32	2.6	10	%
RMS Frequency Error	<300 ^e	1050 ^e	180	?	?	3088 ^d	kHz
Chirp Time	0.5 ^{f,g}	0.25 ^{f,g}	0.5 to 5 ^f	4 ^f	1 ^{f,g}	≥ 0.01	ms
Output Power	5.1	-2.8	?	-3 to -1	10	-17.9 to 4.9	dBm
Phase Noise @ 1 MHz	-85.3	-85	-84	-90	?	-86.0 to -81.4 ^d	dBc/Hz

^a Core IC; requires external ICs ^b Synthesizer + TX ^c Max power, CW Mode ^d In X-band, divide by 2, 4 or 8 for lower bands
^e Including turn-around points ^f Only increasing freq. part ^g Lowest value reported



(a) S-band Measurement, Target at 8 km



(b) X-band Measurement, Target at 8 km

Fig. 5. FMCW Range-Doppler Processing

comparison is made with several FMCW systems. The real benefits, however, are present for fast-chirping pulse-Doppler systems. This comparison can be found in table I. As can be seen, the frequency error can be improved upon, but the chirp rate is by far the highest reported. Fractional bandwidth is surpassed only by [6], which has a far lower level of integration than this work.

V. CONCLUSIONS

The feasibility of a single chip solution for the creation of very fast and wide-band linear frequency chirps is proven in this work. A 5x5 mm² device was created that can generate 1 GHz chirps in X-band with durations as low as 10 μs from a relatively low frequency, easily distributed, reference signal. On-chip frequency division allows for chirp generation in C-, S- and L-band as well. An output driver that provides output power control, CW and pulsed signal generation and wideband matching is included on the IC. A step towards future phased-arrays with a high level of reconfiguration, or with multiple waveforms that are simultaneously transmitted, has been made.

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