Mixed-Signal Testability Analysis for Data-Converter IPs

Araldo van de Kraats and Hans G. Kerkhoff
Testable Design and Testing of Nanosystems Group
MESA+ Institute for Nanotechnology
7500AE Enschede, the Netherlands
Email: h.g.kerkhoff@utwente.nl

***Abstract*— In this paper, a new procedure to derive testability measures is presented. Digital testability can be calculated by means of probability, while in analog it is possible to calculate testability using impedance values. Although attempts have been made to reach compatibility, matching was somewhat arbitrary and therefore not necessarily compatible. The concept of the new approach is that digital and analog can be integrated in a more consistent way. More realistic testability figures are obtained, which makes testability of true mixed-signal systems and circuits feasible. To verify the results, our method is compared with a sensitivity analysis, for a simple 3-bit ADC.**

I. Introduction

With the rapid evolution of mixed-signal technology to support a broad spectrum of electronics, efficient testing techniques become increasingly important. In digital circuits, efficient automatic test pattern generation (ATPG) algorithms have been known for some time. Unfortunately, such algorithms are not yet matured for analog circuits, where functional testing is still the norm. Essentially, each IC must be verified against a predefined set of critical specifications, which usually is not the most efficient method. In the past the quality and the cost of functional testing were not a serious issue [1]. However, with ever increasing circuit complexities and integration of both digital and analog parts on one chip, mixed-signal testing has become a major concern for the microelectronics industry.

The relatively large costs and declining quality of functional testing of mixed-signal systems calls for a different approach. A possible solution may be found in structural testing, which takes advantage of the structural differences in defective and non-defective circuits. By constructing fault-dictionaries as a start for the ATPG—a common strategy in digital testing algorithms—circuits may be tested in a more efficient manner.

Previous work on analog and mixed-signal testing frequently have their limitations which makes them difficult to use in practice. The authors of references [2], [3] make use of circuit-transfer functions to generate tests. These approaches are only useful for the limited class of linear analog circuits. The method in [4] relies on wrapper cells, to separate the analog and digital parts. Pure mixed-signal circuits, with interwoven analog and digital parts may be difficult to handle using this approach. Impractical are techniques that require numerous time-consuming circuit simulations. For example, in [5] each fault needs to be separately simulated in HSPICE. In [6], analog macros are used. Although calculation times are short, a library of macros needs to be constructed. Furthermore, it is impossible to structurally test all internal nodes in the circuit.

In recent years, several publications in the area of testability analysis have appeared. In [5], [7]–[9], testability transfer factors are discussed. However the derived test patterns have a complex shape and difficult to generate in practice. Adjustments to this method have been proposed in [11] and [12]. However, few of the publications on testability satisfactorily examines the validity of the testability measures calculated. In the next chapter it becomes clear that the results produced by these methods are questionable and can be enhanced to a great extend.

This paper discusses a new method to compute quantitative testability measures for each node in true mixed-signal circuits. The information obtained can be used to guide the ATPG process in structural testing algorithms. An efficient and compact test set can be generated more easily this way.

First is described how to conduct the testability analysis using the new method. A comparison with previous work is given in a few simple examples. In the third section the testability analysis of digital circuit components is deduced and compared to testability calculated via probability. A brief overview of the method used to solve the set of equations follows. The results of a testability analysis of a typical mixed-signal circuit are presented and compared to a SPICE sensitivity analysis. Finally, some conclusions are given.

II. Testability analysis of analog components

The testability measure consists of two components. The *Controllability* and the *Observability*.

The controllability of a node in a circuit represents the difficulty of applying an arbitrary signal value at that node by full control of the primary inputs of the circuit. $Z(\omega) = 0$ represents perfect controllability, while an infinite impedance represents a completely uncontrollable node.

The observability of a node represents the difficulty of determining whether or not the expected signal value occurs at the node by observing the primary outputs of the circuit. A value of $Z(\omega) = 0$ represents a perfect observable node, while a node with an infinite impedance value is totally unobservable.

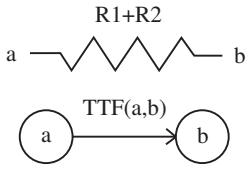

Fig. 1. A resistance with value $R1 + R2$

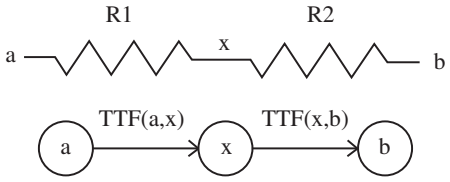

Fig. 2. Two resistances in series with values of $R1$ and $R2$

For comparison purposes, it is possible to normalize the controllability on a scale between 0 (uncontrollable) and 1 (perfect controllability) using:

$$C_N = 1 - \frac{\log |C|}{\log(OC)} \tag{1}$$

with C the controllability in terms of impedance, C_N the normalized controllability and OC the open circuit impedance, which is chosen to be 10 MΩ [12]. For observability, an equation similar to (1) is used.

The first step in the testability analysis is to create a signal flow graph that shows the topology of the circuit. Nodes can be connected by unidirectional or bidirectional edges. Each edge is assigned a TTF (Testability Transfer Factor) that represents the ease of propagating information in that direction. Controllability is propagated in the direction indicated by the edge, while observability propagates in the opposite direction. In principle, both have the same TTF value. Exceptions to this rule are the controllability of primary inputs and the observability of primary outputs, which are not influenced by other nodes. By definition primary inputs are perfectly controllable and primary outputs are perfectly observable.

In figure 1, a resistance with value $R1 + R2$ is shown. For simplicity, unidirectional edges are used. However, the usual model for impedances consists of bidirectional edges. Let us assume node a is a primary input ($C_N(a) = 1$). According to [5], [7]–[9], the controllability of node b will be:

$$C(b) = 1 - \frac{R1 + R2}{OC} \tag{2}$$

Essentially the same circuit is shown in figure 2. Using the same model, the controllability of b is now equal to:

$$\begin{aligned} C(b) &= \left(1 - \frac{R1}{OC}\right)\left(1 - \frac{R2}{OC}\right) \\ &= 1 - \frac{R1 + R2}{OC} + \frac{R1\,R2}{OC^2} \end{aligned} \tag{3}$$

Although equivalent circuits have been used, an error of $(R1\,R2)/OC^2$ is introduced by the model. As can be seen in (3), without this error the result is just an addition of $R1$ and $R2$, normalized by 1-Z(ω)/OC, where Z(ω) is equal to the total impedance $R1 + R2$.

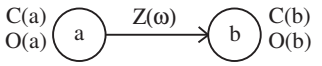

Fig. 3. A basic Signal Flow Graph (SFG)

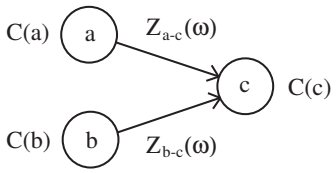

Fig. 4. SFG with two edges directed to one node

To overcome this problem, we propose the following relations for the basic SFG in figure 3. The controllability of node b is:

$$C(b) = C(a) + |Z(\omega)| \tag{4}$$

and the observability of node a is:

$$O(a) = O(b) + |Z(\omega)| \tag{5}$$

Next consider the SFG in figure 4. Assume the following extreme, but very common situation: node a and node b have a perfect controllability. The impedance $Z_{a-c}(\omega)$ has some low value, while $Z_{b-c}(\omega)$ is an open circuit. In this instance, it is reasonable to assume node c is only controlled by node a. Thus node b has no influence on the controllability of node c. However, in the model of [5], [7]–[9], the contribution of each edge towards a certain node is summed and divided by the total number of edges. Clearly, erroneous results are obtained. Instead we propose to take the contribution of each edge as parallel combination of impedance values. For the situation described this results in:

$$\begin{aligned} C(c) &= (C(a) + |Z_{a-c}(\omega)|) \parallel (C(b) + |Z_{b-c}(\omega)|) \\ &= |Z_{a-c}(\omega)| \parallel |Z_{b-c}(\omega)| \\ &\approx |Z_{a-c}(\omega)| \end{aligned} \tag{6}$$

In general, the controllability of node j with n edges directed toward it is:

$$C(j) = \frac{1}{\sum_{i=1}^{n} \frac{1}{C(i)+|Z_{i-j}(\omega)|}} \tag{7}$$

Similar, the observability of node j with n edges directed away from it is:

$$O(j) = \frac{1}{\sum_{i=1}^{n} \frac{1}{O(i)+|Z_{i-j}(\omega)|}} \tag{8}$$

where $Z_{i-j}(\omega)$ is the impedance between node i and j.

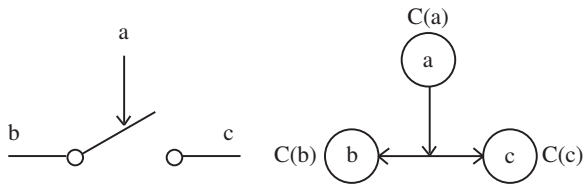

Fig. 5. An ideal switch and its SFG

A simplified SFG for MOSFETs used in the analog domain has been derived in [7]. In [13] a more advanced model is given.

III. Testability analysis of digital components

The analog MOSFET model can only be utilized when small-signal inputs are used and the transistor is in saturation. Thus, this model can no longer be used in case a digital signal is applied to the gate.

To derive a model for use in the digital domain, first consider the ideal switch in figure 5. Obviously, the switch should be closed to transfer the controllability from b to c and vice versa. To which degree the switch can be closed depends solely on the controllability of node a. Basically $C(a)$ modulates the testability transfer factor from b to c. Therefore, we can write for the controllabilities of node b and c:

$$C(b) = C(c) + C(a) \tag{9}$$
$$C(c) = C(b) + C(a) \tag{10}$$

The ideal switch is an adequate model when node b and c are digital signals. However, when they are analog instead, the resistance between these nodes should be taken into account. An extra impedance, usually the output resistance of a transistor, can be added, which gives:

$$C(b) = C(c) + C(a) + Z(\omega) \tag{11}$$
$$C(c) = C(b) + C(a) + Z(\omega) \tag{12}$$

Note that this model is only applicable to controllability calculations. Observability calculations are a bit more complicated, as will be shown later.

To deal with digital signals, the controllability and observability are each split into two components.

- $C0(x)$: zero-controllability, representing the difficulty of setting node x to a logic 0.
- $C1(x)$: one-controllability, representing the difficulty of setting node x to a logic 1.
- $O0(x)$: zero-observability, representing the difficulty of observing a logic 0 on node x at the outputs.
- $O1(x)$: zero-observability, representing the difficulty of observing a logic 1 on node x at the outputs.

Typically, the gate of PMOS transistors will be controlled by $C0$ and the gate of NMOS transistors by $C1$. It is assumed that the supply voltage VDD always has perfect one-controllability ($C1(VDD) = 0\,\Omega$) and the ground GND always has perfect zero-controllability ($C0(GND) = 0\,\Omega$)

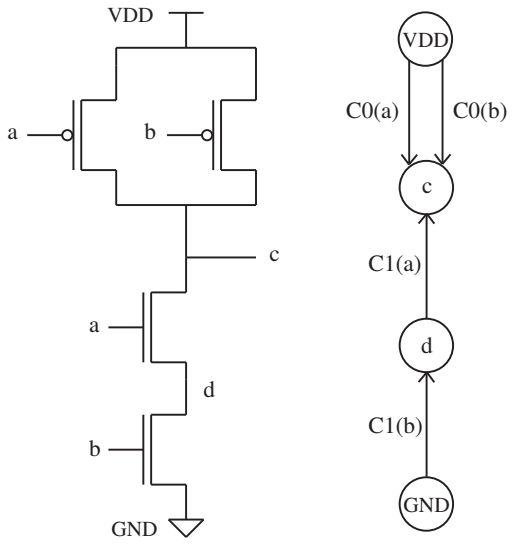

Fig. 6. A common CMOS implementation of a NAND-gate and its SFG

In mixed-signal circuits, when a signal is passed from the analog to the digital domain, C0 and C1 will be set to the controllability value of the analog part:

$$C0(x) := C(x) \tag{13}$$
$$C1(x) := C(x) \tag{14}$$

To recombine $C0$ and $C1$ if a signal is passed from the digital to analog domain, the following expression is used:

$$C(x) := \sqrt{C0(x)\,C1(x)} \tag{15}$$

Since both controllability and testability are important for testing, a testability measure T is defined as [8]:

$$T(x) := \sqrt{C(x)\,O(x)} \tag{16}$$

To clarify the concepts discussed before, the controllabilities of a typical 2-input NAND-gate shown in figure 6 will be computed. Looking at the SFG of the NAND-gate, the zero-controllability for node c will be:

$$\begin{aligned} C0(c) &= C1(a) + C0(d) \\ &= C1(a) + C1(b) + C0(GND) \\ &= C1(a) + C1(b) \end{aligned} \tag{17}$$

and the one-controllability of node c is:

$$\begin{aligned} C1(c) &= (C0(a) + C1(VDD)) \,\|\, (C0(b) + C1(VDD)) \\ &= C0(a) \,\|\, C0(b) \\ &= \frac{C0(a)C0(b)}{C0(a) + C0(b)} \end{aligned} \tag{18}$$

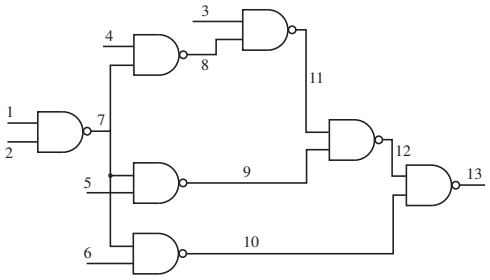

Fig. 7. Example circuit used for controllability comparison

TABLE I

ONE-CONTROLLABILITIES OF THE CIRCUIT IN FIGURE 7

Node #	$C1_P$ **(prob.)**	$C1$ **[$k\Omega$] (this work)**	$C1_N$ **(this work)**
1	1/2	10.0	0.429
2	1/2	10.0	0.429
3	1/2	10.0	0.429
4	1/2	10.0	0.429
5	1/2	10.0	0.429
6	1/2	10.0	0.429
7	3/4	5.0	0.472
8	5/8	6.7	0.454
9	5/8	6.7	0.454
10	5/8	6.7	0.454
11	11/16	6.0	0.460
12	19/32	7.9	0.443
13	41/64	6.9	0.452

Although testability calculation is only shown for a 2-input NAND gate, the approach works just as well for other types of logic gates. In addition, most conceivable implementations should give correct results.

To test the validity of these calculations, the controllability has been calculated for the example circuit shown in figure 7. A probability-based controllability (C_0P and C_1P) computation of the same circuit has been shown in [14]. In table I, the results are given. In figure 8, both the probability based one-controllability and the normalized one-controllability using the method featured in this work are shown. Apart from the scale, both methods produce similar results.

Next the observabilities of the circuit shown in figure 7 will be deduced. For a logic zero to be observable at node a, two conditions are necessary:

- The PMOS controlled by node b should be turned off ($b = 1$). In other words, a good one-controllability of b is required.
- The logic *one* at the output c should be observable.

Therefore, the zero-observability of a is equal to:

$$O0(a) = O1(c) + C1(b) \tag{19}$$

For the one-observability of a the following conditions are necessary:

- Again, the PMOS controlled by node b should be turned off ($b = 1$).
- The logic *zero* at the output c should be observable.

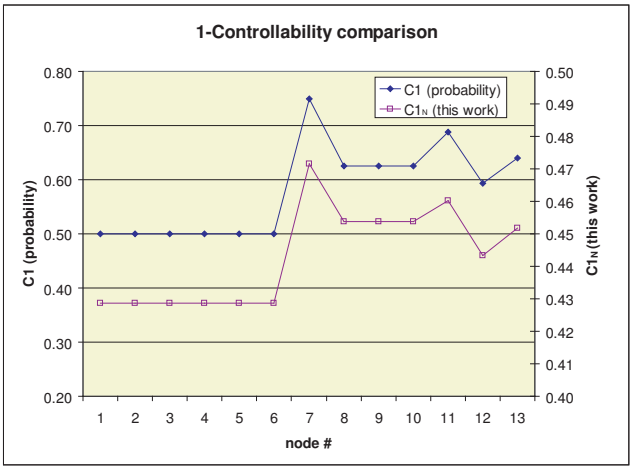

Fig. 8. Comparison of one-controllabilities calculated via probabilities and via the method in this work, for the circuit in figure 7.

The one-observability of a will be:

$$O1(a) = O0(c) + C1(b) \tag{20}$$

In [14], a method to calculate the probability based observabilities ($O0_P$ and $O1_P$) is demonstrated. For the NAND gate, the zero-observability is:

$$\begin{aligned} O0_P(a) &= O1_P(c)\, Prob(b = 1\,|a = 0) \\ &= O1_P(c)\frac{Prob(b = 1, a = 0)}{Prob(a = 0)} \\ &= O1_P(c)\frac{C1_P(b)\, C0_P(a)}{C0_P(a)} \\ &= O1_P(c)\, C1_P(b) \end{aligned} \tag{21}$$

and the the one-observability is:

$$\begin{aligned} O1_P(a) &= O0_P(c)\, Prob(b = 1\,|a = 1) \\ &= O0_P(c)\, C1_P(b) \end{aligned} \tag{22}$$

Independence between the signals at a and b is assumed. The probability-based observabilities (21) and (22) are similar to the observabilities obtained through our method in equation (19) and (20).

IV. Implementation and Results

A. Solving the testability equations

Due to the fact that additions are used for the propagation of testability measures instead of multiplications, the system of equations is no longer linear. Also the fact that some TTF edges are modulated by controllabilities, makes the calculation more complex. A summary of the procedure to solve the testability equations is given in figure 13. The initialization of all controllabilities and observabilities is arbitrarily chosen to be 10 $k\Omega$.

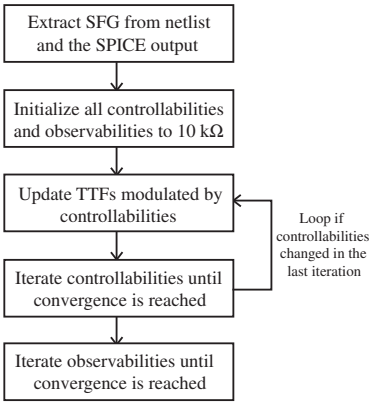

Fig. 9. Process flow used for solving the set of testability equations.

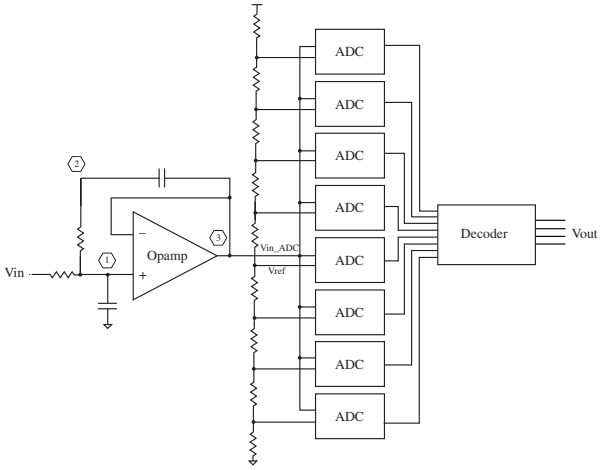

Fig. 10. Sample circuit used for controllability calculations: A low pass filter followed by a 3-bit ADC.

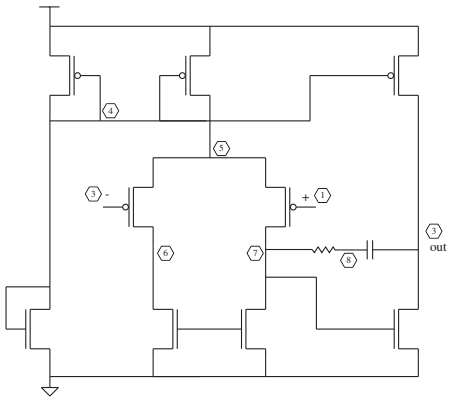

Fig. 11. Opamp implementation.

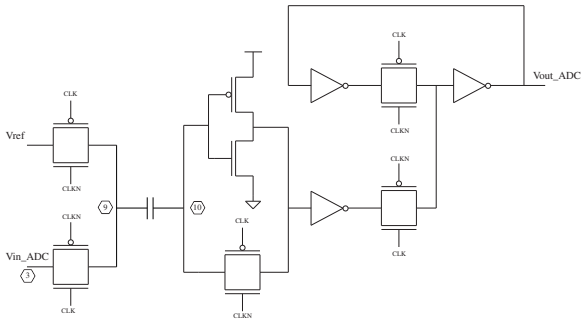

Fig. 12. ADC implementation.

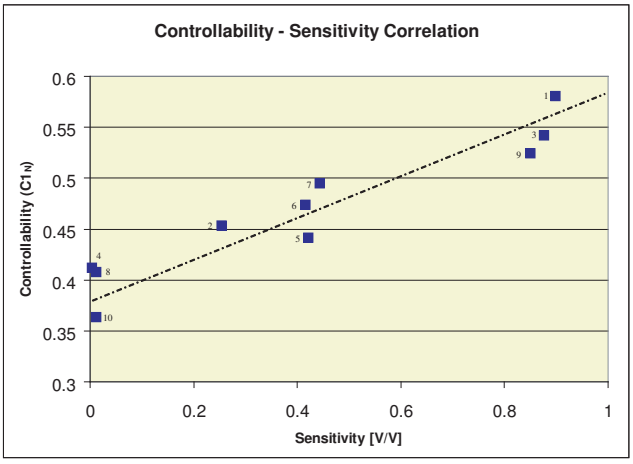

Fig. 13. Correlation between the normalized controllability and the sensitivity of several nodes in a sample circuit.

B. Results and evaluation

To validate our method, the controllability of various nodes in a sample circuit have been calculated and compared to a HPSICE sensitivity analysis. The small-signal sensitivity provides the voltage variation that appears at a certain node, with respect to some other circuit-parameter. In this instance, the input voltage of the circuit is chosen. This is also the primary input for the controllability computations. The sensitivity of a node tells us to which degree the node can be controlled via the chosen circuit-parameter. Therefore results similar to our controllability calculations can be expected.

The circuit used for the calculations is a low-pass filter followed by the 3-bit ADC [12], shown in figure 10. The filter is a well-known two pole low-pass filter, with resistances of 10 $k\Omega$ and capacitors of 10 pF. This gives the filter a 3 dB frequency of approximately 1.1 MHz. A reference operational amplifier [15] has been used for the low-pass filter, shown in figure 11. The implementation of one mixed-signal ADC block can be seen in figure 12.

A frequency of 1.0 MHz has been used for the testability and sensitivity analysis. Testability analysis can be done for all nodes. Unfortunately, small-signal sensitivity analysis only gives meaningful results for analog signals. Therefore only analog nodes have been selected for comparison. Moreover,

the digital part has already been validated when they were compared to the probability figures. The selected analog nodes which have been analyzed are indicated with numbers in polygons.

While extracting the circuit parameters from the SPICE output file, care should be taken that the transistors are in the correct operation area. For example, to obtain the output resistances of the transmission gates in the ADC, the gates have to be set manually to the right value to ensure that the transistors are conducting. Multiple simulations may be required, which makes automation of the process difficult. Another problem arises due to the supply and ground nodes. Testability information may travel through these nodes to other parts of the circuit. In most cases this may not be realistic, which means corruption of the results. This is circumvented by setting the *analog* supply and ground nodes to a high controllability value (uncontrollable).

The results in figure 13 show the controllability versus the sensitivity. The numbers at each intersection correspond to the nodes shown in the circuit diagrams. A certain amount of correlation can be recognized between the controllability and the sensitivity. Therefore, these results add some validity to the testability theory presented. Both methods give an indication for the controllability. Nevertheless, they are quite different, which may explain the deviations from full correlation.

V. Conclusion

A new method for calculating testability of nodes in true mixed-signal circuits has been presented. The method concentrates on making digital and analog testability measures compatible. Testing the method on a example mixed-signal circuit showed a correlation between our results and the (time-consuming) sensitivity analysis. A limitation is that signals are assumed to be independent, while frequently they are not. This may result in slightly inaccurate testability measures. However, it is unlikely this will cause significant errors in its applications.

In analog and mixed-signal testing, no effort should be wasted on testing nodes that have bad testability. On the other hand, nodes with good testability should have a priority in testing. Testability analysis may provide valuable data to guide ATPG for structural tests. Also the area of test set compaction can greatly benefit from testability data.

References

[1] M. Soma, "Automatic test generation algorithms for analogue circuits," *Proc. IEE Circuits, Devices, and Systems*, vol. 143, no. 6, December 1996, pp. 366-373.

[2] R. Ramadoss and M.L. Bushnell, "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs" *Journal of Electronic Testing: Theory and Applications*, vol. 14, 1999, pp. 189-205.

[3] Z. Guo and J. Savir, "Analog Circuit Test Using Transfer Function Coefficient Estimates," *IEICE Trans. on Information & Systems*, vol. E87-D, no.3, March 2004, pp. 642-646.

[4] M. Stancic, L. Fang and H.G. Kerkhoff, "Analogue Core-Based Test-Pattern Generation," Proc. IEEE ProRISC, 1999, pp. 461-466.

[5] S. Huynh, J. Zhang, S. Kim, G. Devarayanadurg and M. Soma, "Efficient Test Set Design for Analog and Mixed-Signal Circuits and Systems," *Proc. 8th Asian Test Symposium (ATS)*, Shanghai, China, November, 1999, pp. 239-244.

[6] V. Kaal and H.G. Kerkhoff, "Compact Structural Test Generation for Analog Macros," *Proc. IEEE European Design and Test Conference*, Paris, France, 1997, pp. 581-587.

[7] S. Huynh, S. Kim, M. Soma and J. Zhang, "Dynamic Test Set Generation for Analog Circuits and Systems," *Proc. 7th Asian Test Symposium (ATS)*, Singapore, December 1998, pp. 360-365.

[8] M. Soma, S. Huynh, J. Zhang, S. Kim and G. Devarayanadurg, "Hierarchical ATPG for Analog Circuits and Systems," *IEEE Design & Test of Computers*, vol. 18, No. 1, January/February 2001, pp. 72-81.

[9] J. Zhang, S. Huynh and M. Soma, "A Test Point Insertion Algorithm for Mixed-Signal Circuits," *Proc. 17th IEEE VLSI Test Symposium*, San Diego, USA, April 1999, p. 319-324.

[10] P. Goel, "An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits," *IEEE Trans. on Computers,"* , vol. C-30, no.3, March 1981, pp. 215-222.

[11] M. Stancic and H.G. Kerkhoff, "Testability-analysis driven test-generation of analogue cores," *Microelectronics Journal*, vol. 34, 2003, pp. 913-917.

[12] H.G. Kerkhoff, "TTF-Based Test-Selection of Mixed-Signal Cores in a SoC," *Proc. 10th International Mixed-Signal Testing Workshop (IMSTW)* , Portland, USA, June 2004, pp. 136-141. Also to appear in *JETTA*.

[13] M. Stancic, "Selection for Analogue Cores Based on the Testability Transfer Function", chapter 3, submitted Ph.D. thesis, University of Twente, Enschede, the Netherlands.

[14] S.C. Seth and V.D. Agrawal, "A new model for computation of probabilistic testability in combination circuits," *Integration, the VLSI journal*, vol. 7, 1989, pp. 49-75.

[15] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Huertas, B. Kim, A. Rueda and M. Soma, "Analog and Mixed-Signal Benchmark Circuits - First Release," *Proc. International Test Conference (ITC'97)*, Washington D.C., USA, November 1997, pp. 183-190.