26.2 3Gb/s Monolithically Integrated Photodiode and Pre-amplifier in Standard 0.18μm CMOS

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For cost, size, and assembly reasons monolithically integrated CMOS optical detectors are preferred in (very) short-range optical data communication [1,2] and in optical storage systems [3]. Another advantage of an integrated photodiode is that high interconnect capacitances and inductances are avoided. Furthermore many parallel optical receivers can be placed on a single chip at low cost, opening the door to optical interconnect. However the serious disadvantage of photodiodes integrated in standard CMOS is the low speed, reported up to 700Mb/s [2].

In this work a fully integrated photodiode with pre-amplifier for bit-rates up to 3Gb/s in standard 0.18μm CMOS is presented. This represents more than half an order of magnitude speed-increase.

For Gigabit Fiber Ethernet [5] 850nm light is used. For photodiodes in modern CMOS at this wavelength the majority of the generated carriers slowly diffuse towards junctions, resulting in a physical (intrinsic) bandwidth of the photodiodes in the low MHz range. This effect typically forms the speed bottleneck in integrated CMOS optical receivers. One solution [1,2] achieves 700Mb/s by cancelling the effect of the slowly diffusing carriers by subtracting two diode responses; this, however, results in lower responsivity and hence lower sensitivity. A solution is described for high-speed data communication with integrated photodiodes without reducing circuit responsivity, achieving 3Gb/s datarate by exploiting an analog equalizer.

A minimal-distance finger n-well/p-substrate diode, (see Fig. 26.2.1), is used as the optical detector. Its overall response consists of three current contributions: two slow diffusion responses (in the n-well and in the p-substrate) and one fast drift current response. The latter is frequency-independent up to frequencies in the GHz range. The typically dominant substrate current has a bandwidth that is several orders of magnitude lower than the bandwidths of the other current components. This substrate current component limits the overall photodiode bandwidth.

The overall intrinsic photodiode response shows a slow decay starting in the low MHz range, due to the combination of the three current components. It can be shown [6] that the roll-off in the overall photocurrent response is only about 5dB/decade for frequencies between roughly 10MHz and the lower GHz range. In the low-GHz range, the roll-off is even lower (<4dB/decade) because the fast depletion region response dominates the overall photocurrent. Signals from the photodiode are low bandwidth (MHz range), but still relatively strong at very high frequencies (GHz range). Therefore an analog equalizer is introduced that compensates (in gain and phase) for the diode photocurrent roll-off in the range from DC to 1GHz. As a result, a 3Gb/s data-rate with a BER<10^{-11} is achieved.

The presented analog equalizer is designed to compensate the frequency characteristic of the applied photodiode from DC to 1GHz, using four high-pass filters. Although a parallel configuration shown in Fig. 26.2.2 is optimum w.r.t. equalization, the current implementation uses three parallel HPF sections (R_2C_2, R_3C_3 and R_4C_4) and one HF peaking section for area and power efficiency. With the circuit of Fig. 26.2.3 it is fairly straightforward to compensate the diode-characteristic for frequencies where the roll-off is low (for ≤5dB/decade). This is for frequencies up to $f_{3dBdrift}=0.4v_s/W$, where v_s is saturation velocity of charge carriers and W is a depletion region depth. For 0.18μm CMOS, this frequency is about 8GHz.

Important in the design of equalizers is spread both on the characteristic to be compensated and on the equalizer itself. Due to the low roll-off of the photodiode the robustness against spread is high, which is conformed by Monte-Carlo simulations including +/- 20% component spread in the equalizer: only 10% decrease in the data eye amplitude results. Hence adaptive equalization is not required: the system is inherently robust. Figure 26.2.4 shows the simulated pulse response with and without equalization and with component spread.

The current design is optimized for 850nm light. For shorter light wavelengths, the photodiode bandwidth is higher but shows a similar low roll-off. Also then, the application of an analog equalizer increases the diode bandwidth considerably, with the equalization required over a smaller frequency range. A similar result holds for other CMOS generations.

Apart from the intrinsic bandwidth of the diode and the equalization of its response, also the electrical bandwidth of the diode and the pre-amplifier are important. Usually this bandwidth is determined by the diode capacitance in combination with the pre-amplifier's input impedance. For our system the capacitance is dominated by the photodiode capacitance of roughly 1.3pF, requiring an input resistance of the TIA (see Fig. 26.2.2) below 50Ω for 3Gb/s data rates; an LNA-like circuit is used for the TIA.

Important for the BER of optical systems is the SNR. With the proposed circuit, the responsivity (signal level) of the photodiode is maximal since the total photocurrent is amplified. However, the equalizer also boosts the gain for high frequency noise thereby degrading the SNR. The total noise in the circuit is dominated by the TIA (~75%), while the equalizer's frequency response is band-limited to maximize the SNR [4]. Then, with approximately 60% more photocurrent available in comparison with [1,2], for the same SNR more than four times higher data-rates are achieved. With respect to conventional CMOS detectors a few orders higher data-rates are achieved.

The chip micrograph is shown in Fig. 26.2.7. The dimensions are 145×305μm². The photodiode size is 50×50μm², corresponding to a multimode fiber's core size. BER versus input optical power is shown in Fig. 26.2.5. The sensitivity is comparable to [1,2]. An eye diagram measured at 3Gb/s and 2^{31}-1 PRBS input signal for -19dBm input power (25μW peak-peak) is shown in Fig. 26.2.6. The overall transimpedance is 5000Ω. Power consumption with 1.8V supply voltage is 34mW plus 16mW for the 50Ω output buffer for evaluation.

References:

[1] J.Genoe et al., "Calculation of the Current Response of the Spatially Modulated Light CMOS Detectors," *IEEE Tr. El. Dev.*, vol. 48, no. 9, pp. 1892-1902, 2001.

[2] C. Rooman et.al, "Inter-Chip Optical Interconnects Using Imaging Fiber Bundles and Integrated CMOS Detectors," *ECOC'01*, pp. 296-297

[3] G.W.de Jong et al., "A DC-to-250MHz Current Pre-Amplifier with Integrated Photo-Diodes in Standard CBiMOS, for Optical-Storage Systems," *ISSCC Dig. Tech. Papers,* pp. 362-363, Feb. 2002.

[4] P.Amini and O.Shoaei: "A Low-Power Gigabit Ethernet Analog Equalizer," *ISCAS 2001*, pp 176-179

[5] IEEE 10 Gigabit Ethernet Standard 802.3ae

[6] S. Radovanovic´ et al., "Physical and Electrical Bandwidths of Integrated Photodiodes in Standard CMOS Technology," accepted for EDSSC2003

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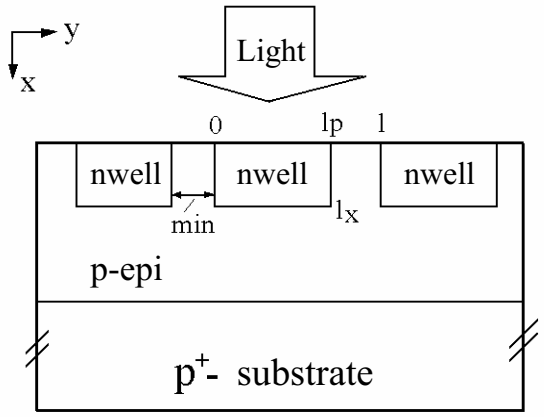

Figure 26.2.1: Cross-section of the finger nwell/p-substrate photodiode in standard CMOS technology.

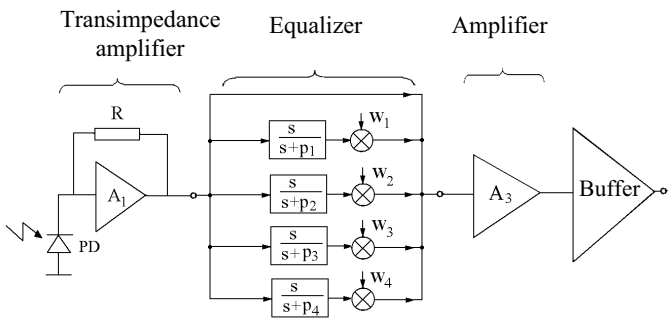

Figure 26.2.2: Block-diagram of integrated photodiode and preamplifier system using an analog equalizer.

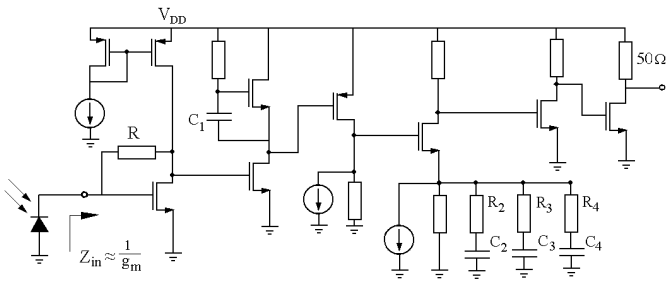

Figure 26.2.3: Circuit topology of the preamplifier including an analog equalizer.

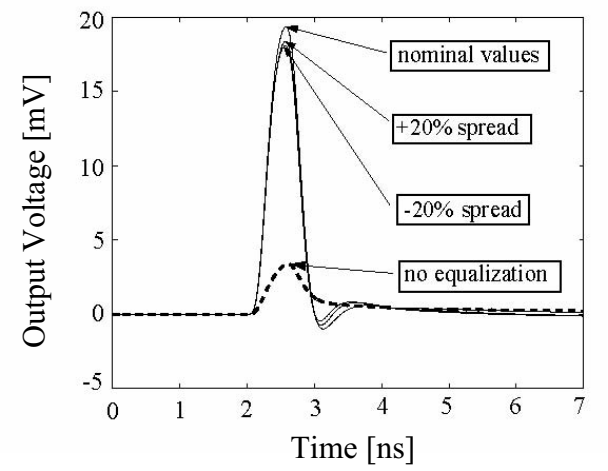

Figure 26.2.4: Simulated time responses without and with the equalizer with its nominal values and ±20% spread in the component values.

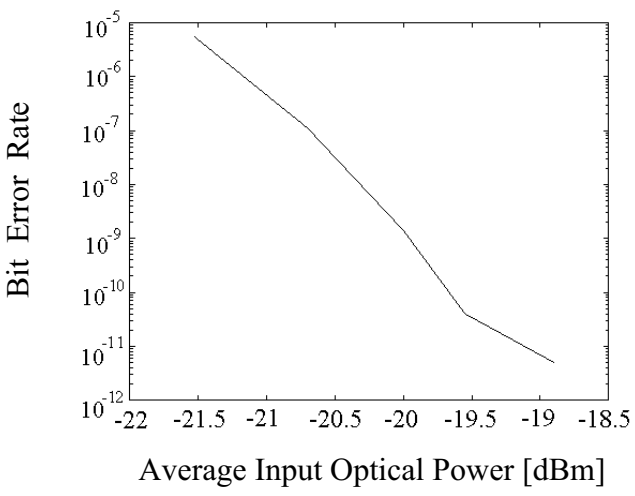

Figure 26.2.5: Bit-error rate vs. input optical power.

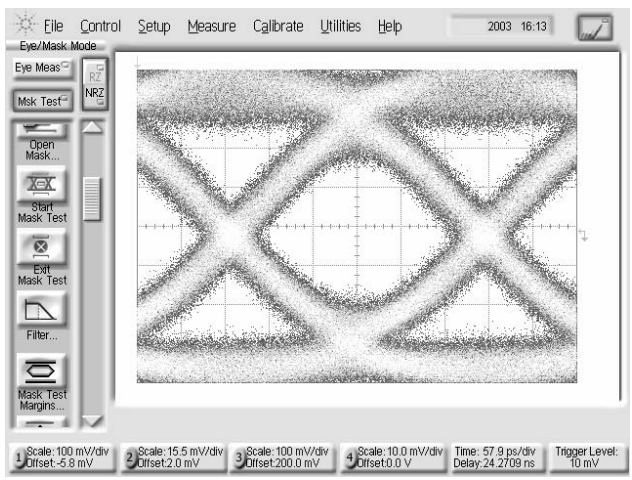

Figure 26.2.6: Eye-diagram of the equalizer output with 3Gb/s PRBS input signal. Y-scale: 15.5mV/div, X-scale: 57.9ps/div.

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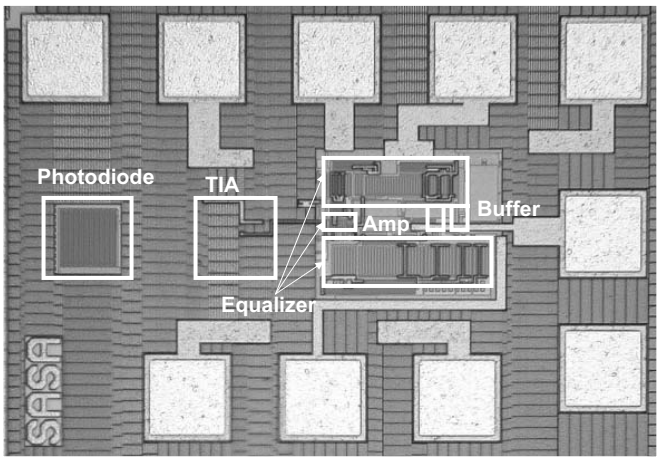

Figure 26.2.7: Chip micrograph of the integrated photodiode and pre-amplifer with an analog equalizer in a fully standard CMOS.

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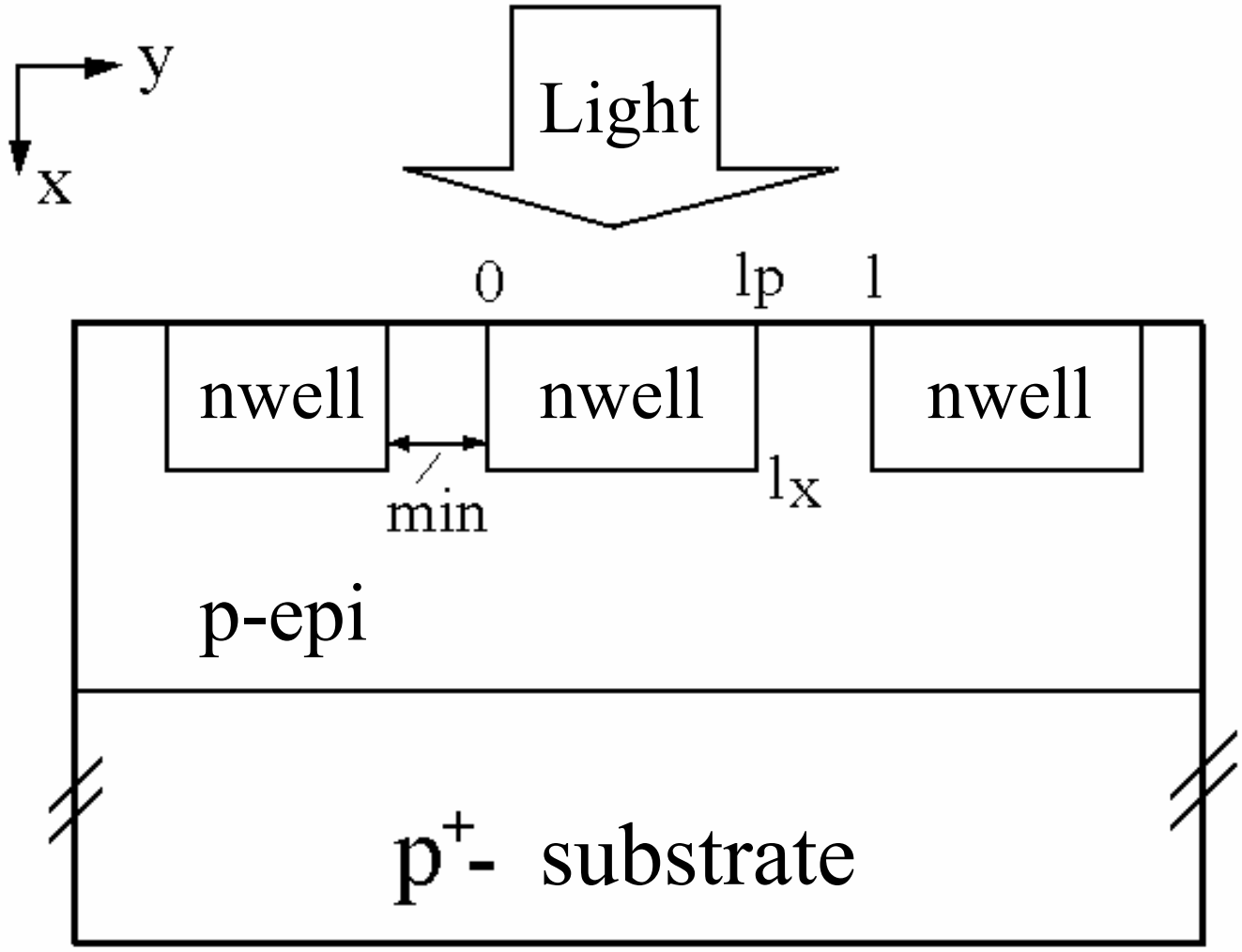

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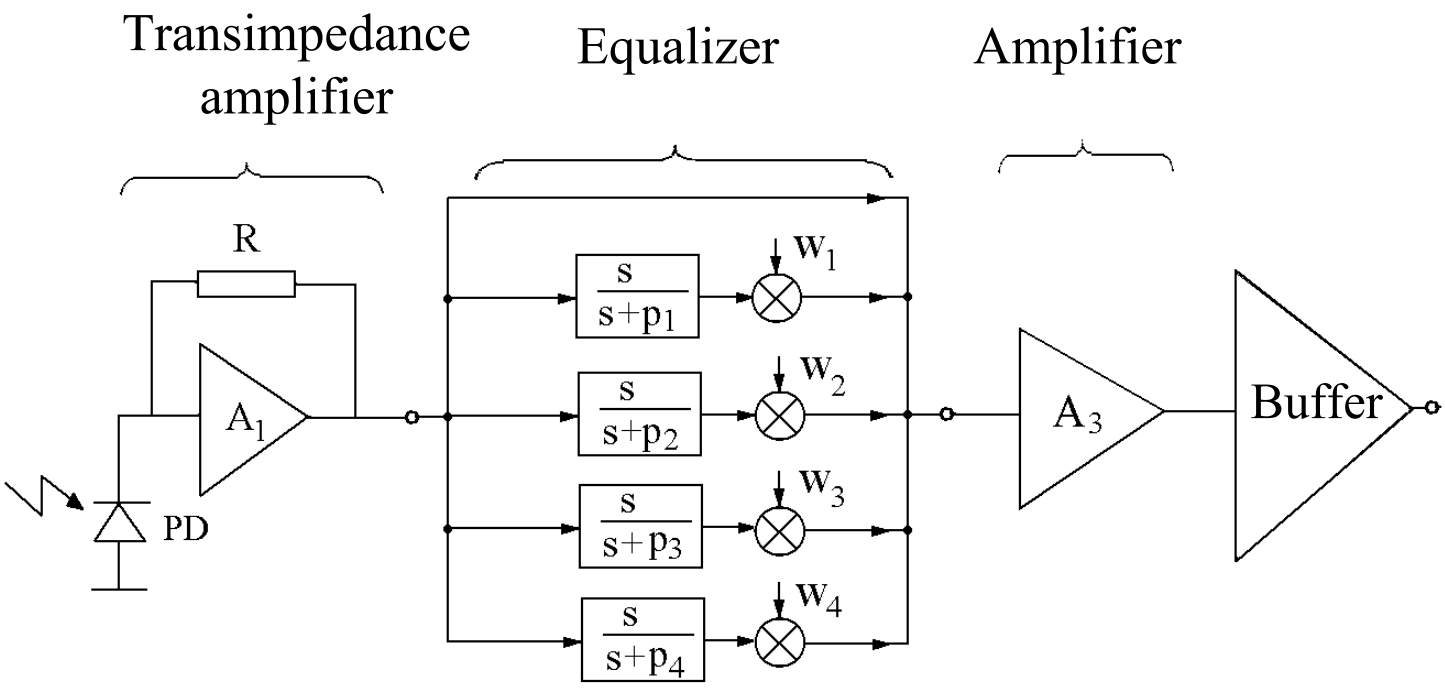

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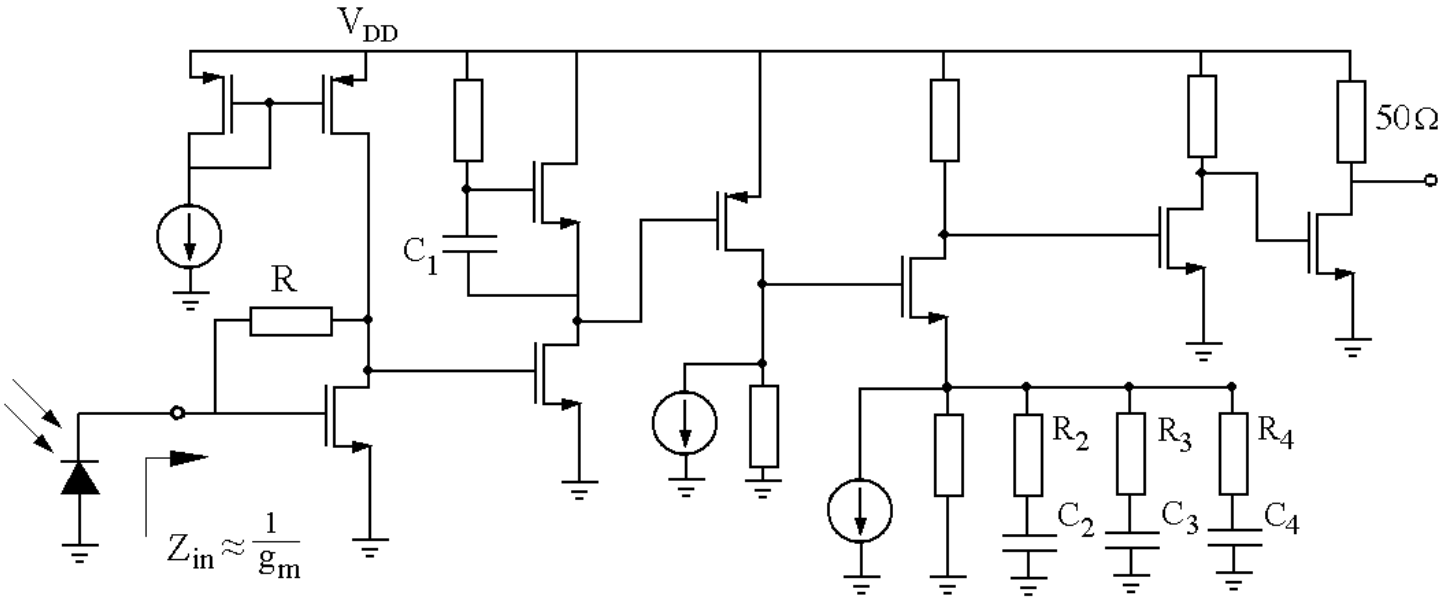

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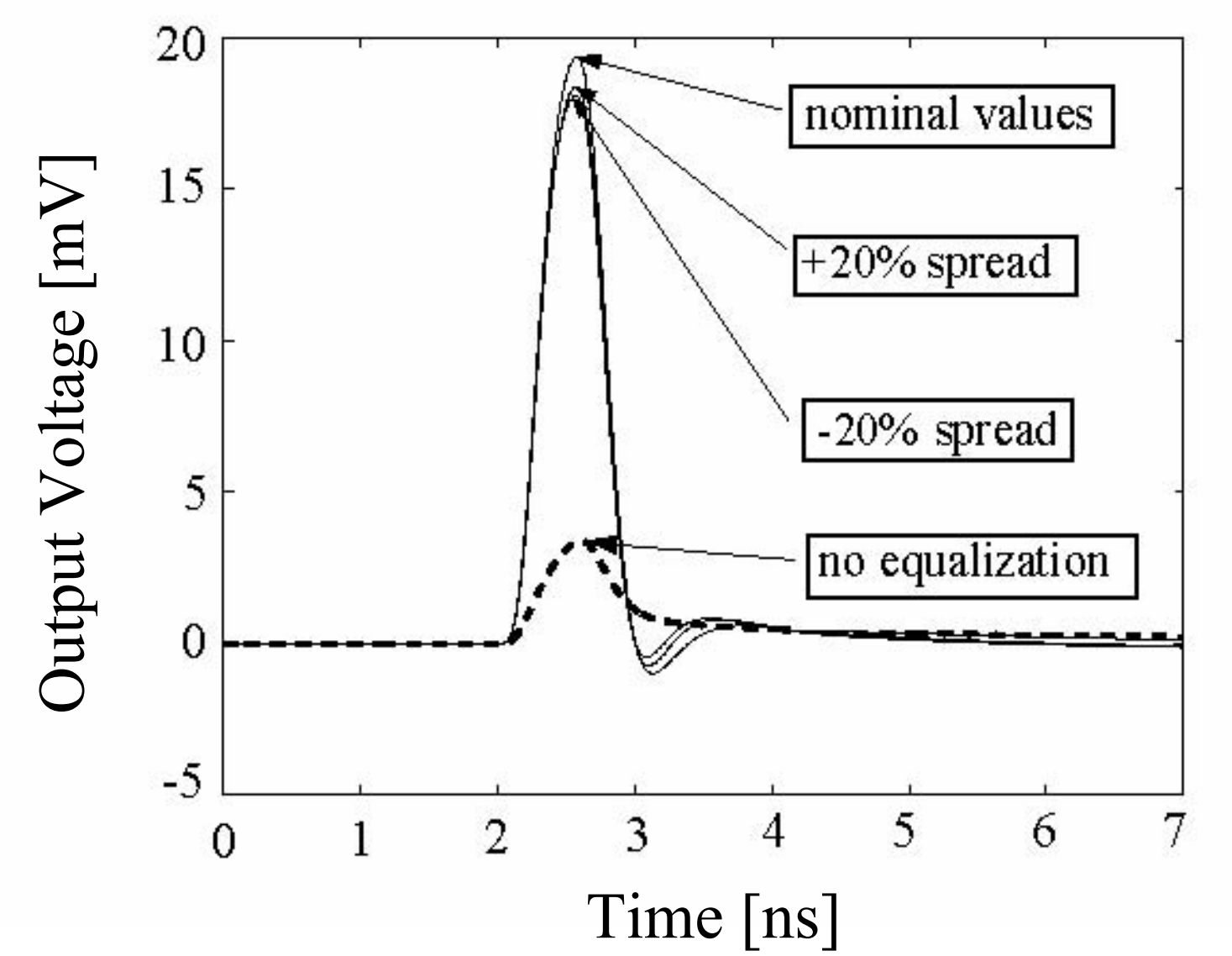

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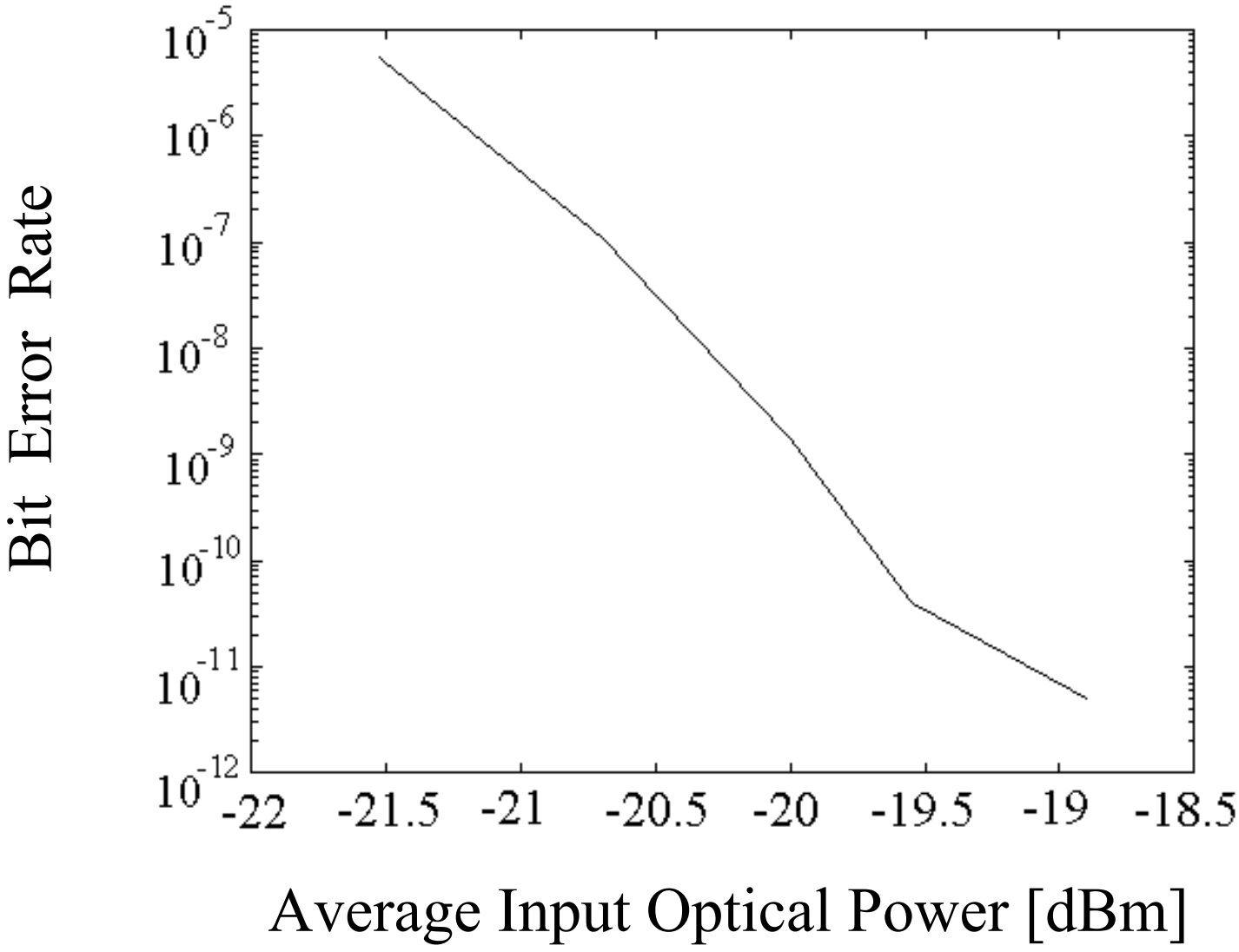

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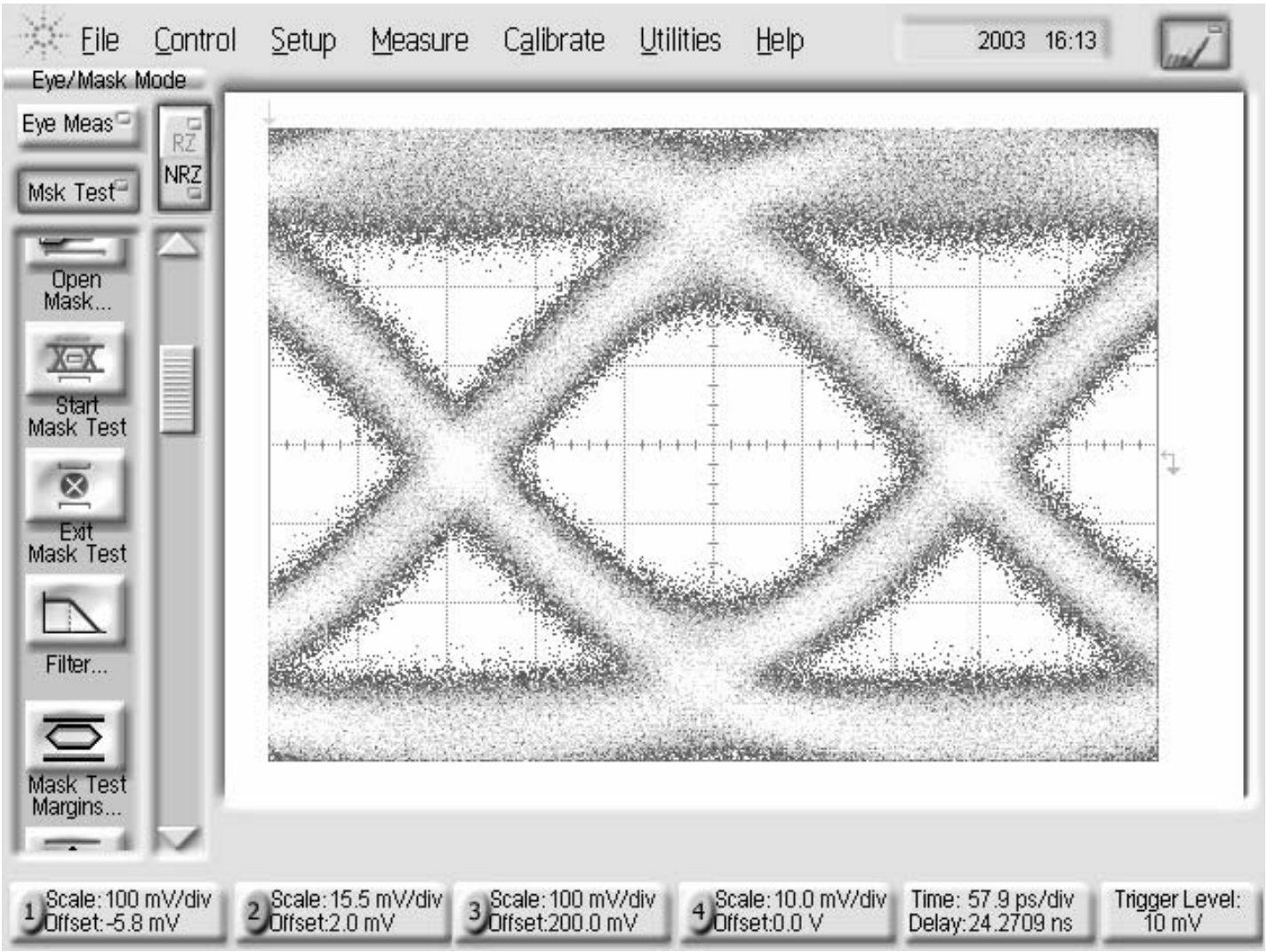

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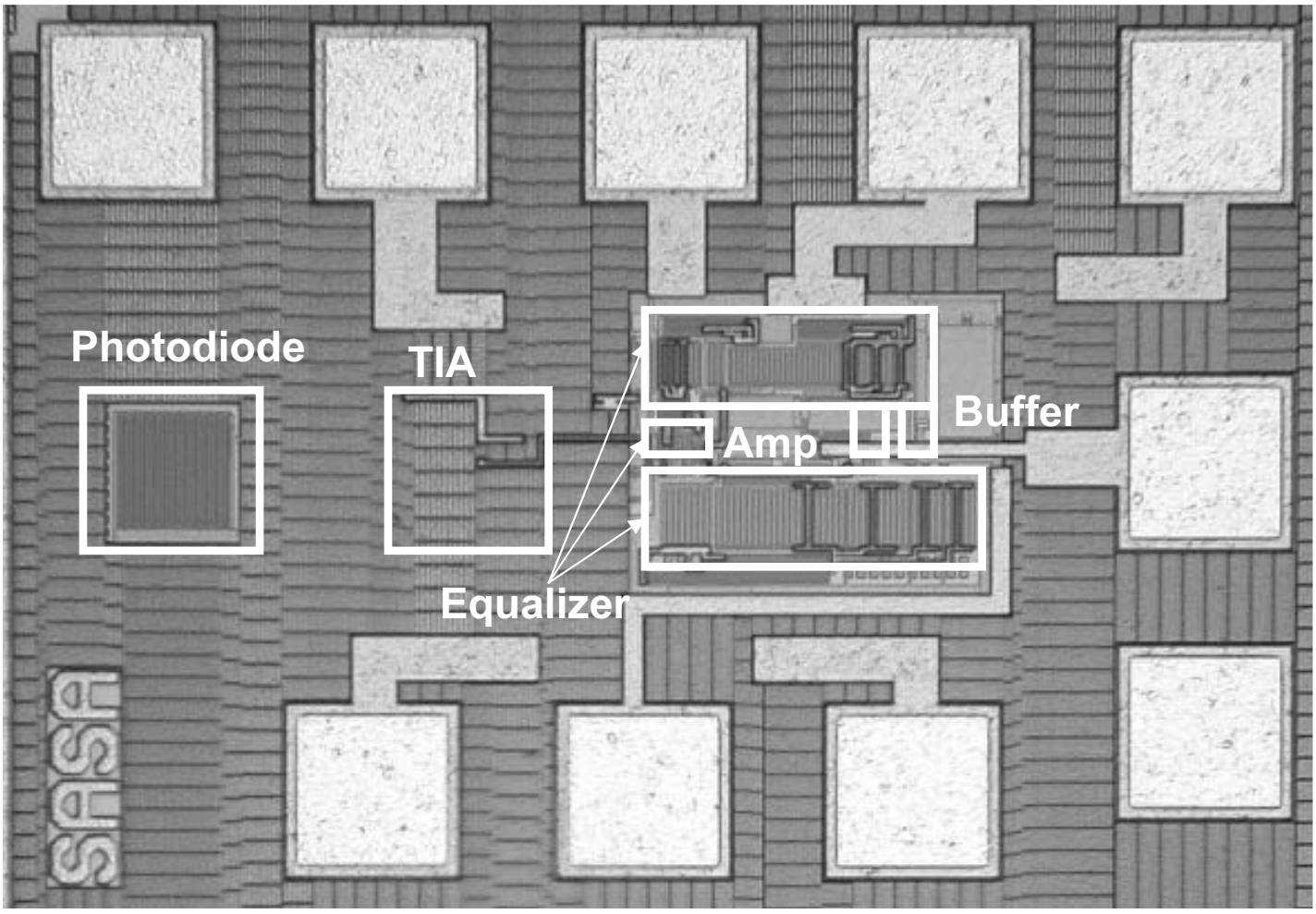

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