A TEST CHIP FOR AUTOMATIC RELIABILITY MEASUREMENTS OF INTERCONNECT VIAS

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Abstract

This paper describes a test chip that was especially designed for via-hole electromigration reliability measurements. The test chip allows a high degree of automation for this type of measurement, using only a small number of measurement instruments.

1. Introduction

For modern VLSI/ULSI fabrication the use of multilevel interconnects is of crucial importance. For electromigration reliability characterizations, time-consuming stress measurements have to be carried out [1,2]. During these measurements a via-hole chain is stressed because of high temperature and high current densities, and the resistance is determined. This type of measurement usually takes much measurement equipment, e.g. current sources, heating equipment and voltmeters. In this paper the design and verification of a test chip that allows automation of via stress measurements and reduces the number of used measurement instruments is described.

2. Conventional Stress Measurements

In this section, conventional stress measurement techniques used and the evaluation of the measured results is discussed.

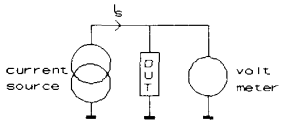

Figure 1. Typical stress measurement setup.

2.1. Measurement Setup

Figure 1 shows a typical measurement setup for stress measurements. The device under test (DUT) is in our case a via-hole chain as shown in figure 2. The DUT is heated up to a constant temperature between 150°C and 200°C. The current source forces a current through the DUT. The value of the forced current is chosen in such a way that a current density of 1E6 A/cm^2 is achieved. The voltage across the DUT is measured by a voltmeter.

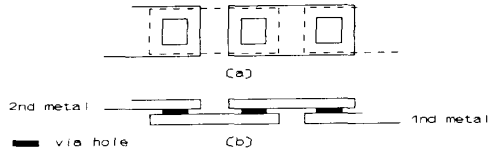

Figure 2. Via-hole chain, (a) Top view, (b) Cross-sectional view.

2.2. Test Procedure

As figure 3 shows, the via-hole resistance increases with time during an electromigration test. This is due to void formation in interconnect lines. The failure time was defined as the time at which the resistance of the via-hole chain has increased by 20 %. The resistance at the start of the stress measurement is denoted by R_0 while R_t is the resistance at time 't' in hours.

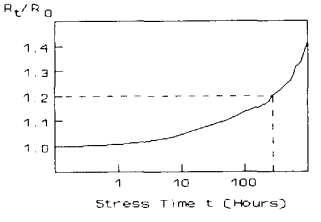

Figure 3. Sketch of the time dependence of via-hole resistance increase (typical behavior).

The lifetime is determined by measuring the resistance under given testing conditions. The median time to failure, MTTF, is a function of the current density J and the absolute temperature T according to equation 1.

$$MTTF \propto J^{n}\exp\left(-\frac{E_a}{kT}\right), \qquad (1)$$

where:

- J = current density in A/cm^2
- n = current acceleration factor (1-2)
- E_a = Activation energy in eV

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k = Boltzmann's constant

T = Device temperature in °K

2.3. Practical Measurement Setups

For statistical analysis the measurements have to be carried out on a number of via-hole chains and at a number of different temperatures. In this section two measurement setups are discussed that allow simultaneous stressing of a number of DUTs.

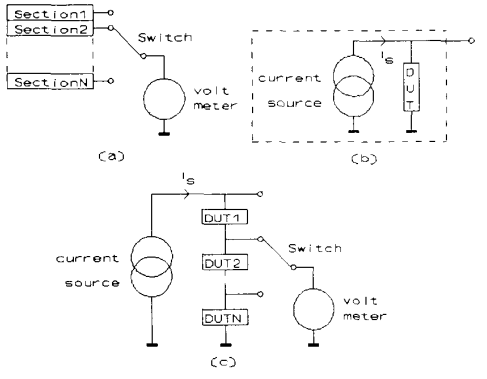

Figure 4. (a) Parallel measurement setup, (b) Single stress section, (c) Series measurement setup.

2.3.1. DUTs connected in parallel

A measurement setup as shown in figure 4a is used. The setup consists of a number of single stress sections, each consisting of a current source and a DUT (figure 4b). The voltage of each DUT is measured by means of a voltmeter which is connected to the stress sections by means of a switch. Thus, only one voltmeter is necessary. However, for continuous current stressing, N current sources are required, where N is the number of DUTs that have to be stressed simultaneously.

2.3.2. DUTs connected in series

The measurement setup for these tests is shown in figure 4c.
The setup consists of a number of single DUTs. The voltage drop across each DUT is indirectly measured by means of a voltmeter that is connected to the DUT by means of a switch. Hence, only one voltmeter and one current source are necessary.
This measurement method can only be used if the total resistance of all DUTs is not too high. This is because the terminal voltage of an electronic current source is limited. The number of DUTs should not be too large because the voltage drop across each DUT cannot be determined with sufficient accuracy. Another drawback is that if a fatal error occurs in one of the DUTs, e.g. a void, the test circuit will provide no useful information.

3. Test Circuit For Stress Measurements

In the section 2.3 the problems that can arise if traditional measurement setups are used, were discussed.
A test circuit for stress measurements should be simple, require few measurement instruments, enable simultaneous measurements and provide reliable test results. A block diagram of a stress-measurement test circuit that meets these criteria is depicted in figure 5. The cental feature of this testcircuit is a new test chip that provides on-chip current sources and switching.

The current, I_{in}, of a current source is applied to a set of parallel current mirrors. Each current mirror copies the current and applies it to a DUT. The voltage of an arbitrary DUT can be measured by applying the corresponding DUT select code. The multiplexer circuit switches the voltage of the selected DUT to the voltmeter.

4. Test Chip Design

In this section the design of the test

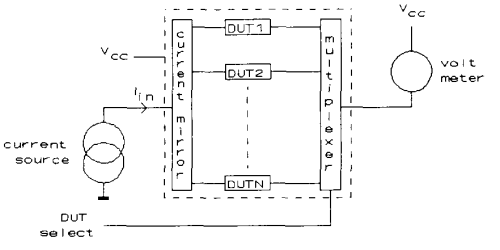

Figure 5. Block diagram of the stress measurement circuit.

chip will be discussed. The test chip contains the test circuit that enables stressing of four via-hole chains simultaneously. The number four was an arbitrary choice; a larger number, however, is also possible.

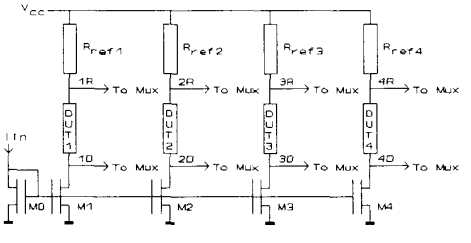

Figure 6. Circuit diagram of the current mirror including the DUTs.

4.1. Stress Section

The circuit diagram of the stress section is shown in figure 6. The actual stress sections consist of four equal transistors M1 to M4 with DUT1 to DUT4, via-hole chains consisting of 300 contacts each. R_{ref1} to R_{ref4} are equal poly-resistors. By measuring the voltage drop across each resistor, the value of the stress current of each DUT can be determined.

The value of the actual stress current depends on the value of the input current I_{in} of transistor M0, and the width and length ratios of transistor M0 and the transistors M1 to M4. The output voltage of the DUT and R_{ref} is connected to a multiplexer circuit.

4.2. Multiplexer Circuit

Figure 7 shows the multiplexer circuit for the test chip. The circuit consists only of PMOS transistors because the expected value of the DUT voltage V_{out} is in the range of V_{cc}. In the design the shift of the transistor parameters due to the high operating temperature was taken into account. Therefore the measurement of V_{out} can be carried out with sufficient accuracy.

4.3. Design Considerations

The high operating temperature of the test chip can cause problems. In order to minimize electromigration-related problems in the transistors and resistors, special attention was paid to their layout. All interconnects are made of tungsten.
Single elements of the current mirror and the multiplexer circuit were included

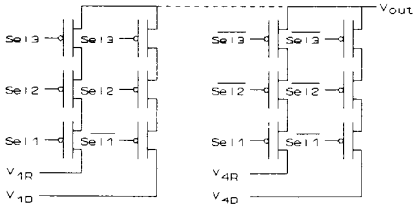

Figure 7. Multiplexer circuit.

on the test chip. This enables monitoring of high temperature effects, e.g. shift in threshold voltage etc.
Furthermore an extra poly-resistor, R_{Temp}, was added to be able to monitor the on-chip temperature.
In order to correlate the measurement results of the test circuit with test results of a conventional via-hole chain, a single via-hole chain was included on the test chip.

5. Measurements

Figure 8 shows one stress section and elements used during the measurement.
The test circuit is heated to the desired stress temperature. Then value of a calibration resistance, R_{cal}, is determined.
The on-chip temperature can be determined by measuring the value of R_{Temp} during the stress measurement.
The value of R_{cal}, a poly-resistor, is equal to the value of the resistor R_{ref1} (and R_{ref2} to R_{ref4} of the other stress sections). From the value of the voltage drop across R_{ref1} and the value of R_{ref1} the stress current I_s of the section can be calculated.
Due to the inherent non ideal behavior of the current mirror, e.g. shift in threshold voltage and mobility of the transistors due to the high temperature, I_s cannot be calculated with sufficient accuracy out of the width and length ratios of the transistors and the input current I_{in} of the current mirror.
The variation in the resistance of the DUT can be expressed as:

$$\frac{R_t}{R_0} = \frac{V_{DUTt} \cdot V_{ref0}}{V_{DUT0} \cdot V_{reft}} \cdot \frac{R_{reft}}{R_{ref0}}, \qquad (2)$$

where:

R_{ref0} = Value of Rref at time=0

R_{reft} = Value of Rref at time=t

V_{DUT0} = DUT voltage at time=0

V_{DUTt} = DUT voltage at time=t

V_{ref0} = Voltage across resistor at time=0

V_{reft} = Voltage across resistor at time=t

This equation deals with the variation of thecurrent I_s in the section due to device

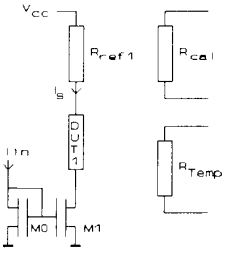

Figure 8. Measurement circuit.

degradation in the current mirror, and the variation of the R_{ref} due to temperature changes.

6. Experimental Results

The test circuit was fabricated in the UT-BICMOS process [3] and used for measurements of the electromigration reliability of via-hole structures.
Figure 9 shows the tested via-hole structure; first metal tungsten and second metal aluminum.
Figure 10 shows the results of the measurements using the new test circuit and compare them to the results of the measurements using a traditional via-hole chain structure.

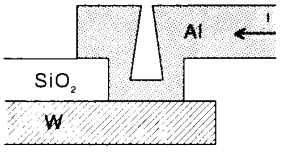

Figure 9. Cross sectional view of via-hole structure.

7. Conclusions

A test circuit for electromigration reliability measurements of via-hole chains (DUTs) was designed and tested. The test circuit enables simultaneous measurements of a number of DUTS, and a fatal error of one DUT does not influence the measurement results of the other DUTs. Measurements require only a few measurement instruments.
Comparing the measurement results of a single DUT to the measurement results of the test circuit shows that a test circuit may be used for reliability measurements.

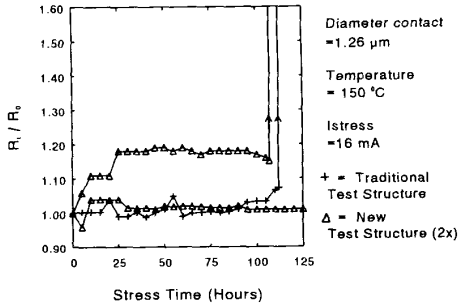

Figure 10. Measurement results.

The test circuit is a very useful tool for electromigration reliability measurements.

Acknowledgements

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