Characterization of platinum lift-off technique

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Abstract- In micro electromechanical systems (MEMS) and micro electronic devices there has been a strong demand for the fabrication of electrodes. Platinum (Pt) is a good candidate for this, because it combines some attractive properties: low electrical resistance, high melting point and high chemical stability. However, the latest leads to very difficult for patterning Pt by wet chemical or dry etching. Besides, etching damages the surface making wafer bonding impossible. Lift-off seems to be a solution to this problem. A big problem in using lift-off is that platinum particles or ears may remain at the edges after lift-off. These ears protrude from the surface and may cause electrical shortcuts with an opposite electrode. Some authors reported shortly about a modified lift-off technique to overcome this problem. Before deposition of the metal, a small cavity is etched in the insulator, which is mostly SiO_2, thereby breaking the metal during deposition. In this paper the effect of cavity depth and metal thickness on ear forming is investigated. A surface roughness and a resistance of the as-deposited metals are measured. The results of method have been applied successfully for Load Cell sensors in our lab.

I. Introduction

Many micro electromechanical systems and micro electronic devices require metallizations that can withstand high temperatures. For example, a microfabricated chemical reactor system needs thin metal films for heating and temperature sensing that can withstand prolonged 1000^0C exposure [1]. Moreover, in MEMS very often the metal has to survive

cleaning procedures and pretreatment of wafers in an oxygen rich environment before wafer bonding [2]. Most metals are destroyed if subjected to one or more of these conditions. However, platinum (Pt) does not (or hardly) have any of these problems while having a resistance that is only four times higher than the resistance of aluminum. With a melting point of 1772 °C and its inertness for many chemicals like HNO_3 and Piranha (3), it has been widely used. For instance, in [1,4,5,6] Pt is used as electrode material or sensing element in MEMS devices. Also, it is often applied as electrode material for advanced memory chips such as DRAMs (dynamic random access memories) [7], FRAMs (nonvolatile random access memories) [8], opto-electronic devices [9] and many other applications in IC technology.

For deposition of Pt on SiO_2, a layer of titanium (Ti) is required to ensure proper adhesion of the Pt thin film [10]. Besides, the Ti layer also prevents the formation of Pt silicides, which have a quite high resistance [11,12],

A big problem of Pt metallization is that it is difficult to pattern because of its high chemical stability. Although many methods such as wet etching [13], dry etching [14] and a combination of wet and dry etching [15] have been developed to etch Pt, still some problems remain. For example, Pt redeposition during dry etching is still not very well controlled [14]. This problem will make direct wafer bonding impossible, because the bonding surface is polluted with metal. Besides, etching can attack silicon and SiO_2, thereby making the bonding surface too rough for direct wafer bonding. Pt etching by ion milling could be an alternative solution but it is quite expensive [16].

Lift-off of Pt seems to be an attractive solution to overcome the aforementioned problems. In this method a layer of photoresist is used, which is patterned. Then, after depositing Pt the resist layer is removed by acetone in ultrasonic batch. By doing so, the Pt

layer remains at the areas where it should be (17). Due to the positive slope of the photoresist, a thin sheet of metal is deposited on the slope itself. Then, when the metal deposited is relatively flexible, or when the ratio between metal structure size and photoresist thickness is too small, lift-off etching will remove all photoresist, but will not remove the metal, which is deposited on the sidewall [18]. This metal forms ears. An example of an ear is shown in figure 1. In this case, the thickness of Shipley positive photoresist and Pt/Ti are 2 μm and 310 nm, respectively. The height of the ear forming is estimated about 500 nm.

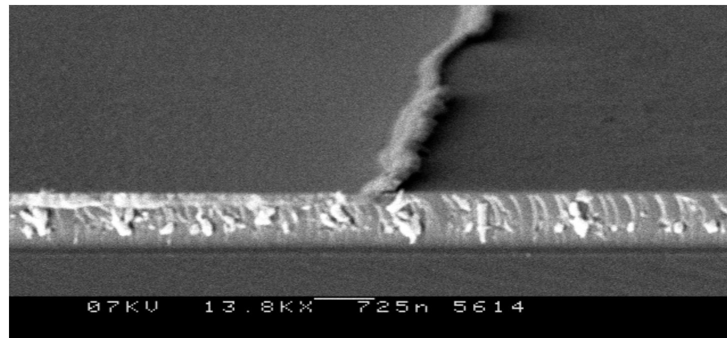


Fig.1.A SEM image of a Pt ear protruding from the wafer surface. The height of Pt ear is about 500 nm.

In MEMS devices (5), these ears can cause electrical short cuts with an opposite electrode that is placed within 1 or 2 um distance. In order to prevent ear forming a modified lift-off technique was developed which is presented in [18,19]. The process is shown in figure 2.

However, in literature no elaborate study was found on the modified lift-off technique. In this paper this technique is characterized with respect to Pt/Ti at different thickness. In Fig.2, M is defined as the total thickness of the deposited metal layers and S is defined as the depth of $Si0_2$ cavity. Then the influence of different K = M/S ratios on ear forming is investigated by Scanning Electron Microscope (SEM). The surface roughness and resistance of

the deposited metal layer are measured by Dimension 3100 Atomic Force Microscope (AFM) and Matheson Resistivity Prober, respectively. The technique is also applied to pattern for other metals such as Ta.

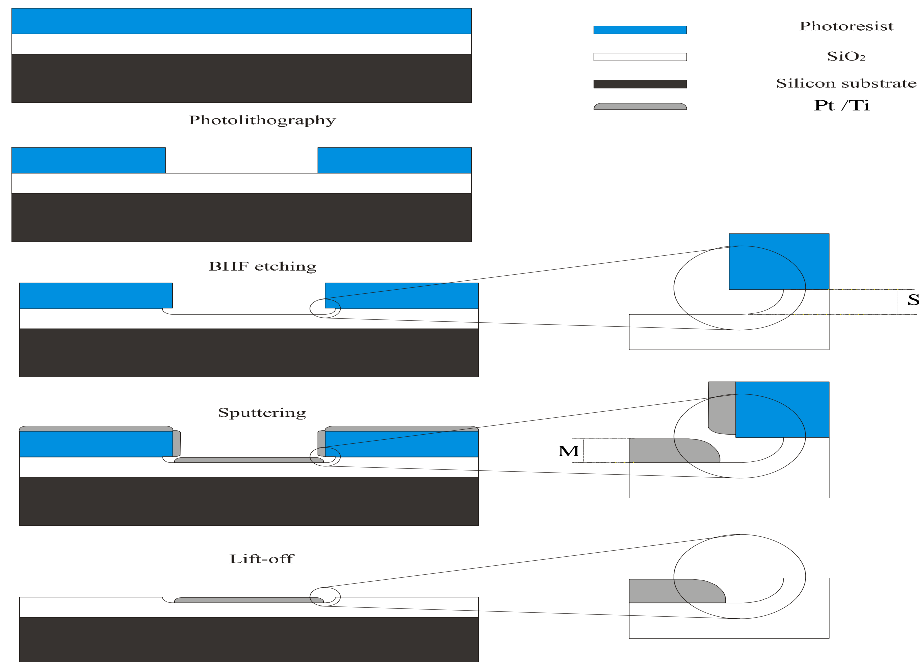


Fig.2. Schematic overview of the modified lift-off process.

II. Experimental setup

Figure 2 shows a schematic overview of the modified lift-off process. First of all, a layer of 1 μm wet thermal SiO_2 was grown on a 3-inch silicon wafer. Evaporated hexamethyldisilazane (HMDS) served as an adhesion promoter for the subsequent resist layer. Positive resist Shipley 907/17 was coated by spinning, resulting in a thickness of 2 μm. Then a conventional lithography process was carried out to define the windows n. After development, the wafers were given a post-bake at 120 ^{0}C for 45 minutes to strengthen the photoresist. Then, the cavity in the SiO_2 was isotropically etched in a buffered HF-solution (1:7), the

etching speed being 70 nm/min. Due to isotropic etching of SiO_2, underetching of the photoresist occurs [18,20]. Then, the wafers were rinsed in deionized water, dry spinning and directly followed by DC magneton sputtering of the metal/metals. The Pt layers were deposited at different thickness with 40 nm Ti as the adhesion layer. The bi-layer was sputtered onto the sample without breaking the vacuum. Moreover, 260 nm thick tantalum (Ta) was also deposited in order to investigate a feasibility of applying method for other metals. The lift-off process was carried out in acetone supported by ultrasonic for 30 minutes. In table 1, the parameters of the different experiments are shown.

	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
Metal	Pt/Ti	Pt/Ti	Pt/Ti	Pt/Ti	Ta/Ti
S(nm)	400	300	200	200	300
M(nm)	300	400	400	500	300
K	0.75	1.33	2	2.5	1
Resist thickness (μm)	2	2	2	2	2
SEM number	N_0.1a	N_0.2a	N_0.3a	N_0.4a	N_0.5a
AFM number	N_0.1b	N_0.2b	*	N_0.4b	
Ra (nm)	3.2	2.7	*	2.9	
Maximum peak value (nm)	5	4	*	4	
Ra* (nm)	3.1	2.5	*	2.9	
R (Ω/□)	0.61	0.43	0.43	0.31	
R* (Ω/□)	0.57	0.41	0.40	0.29	

Table 1: Parameters for the different samples

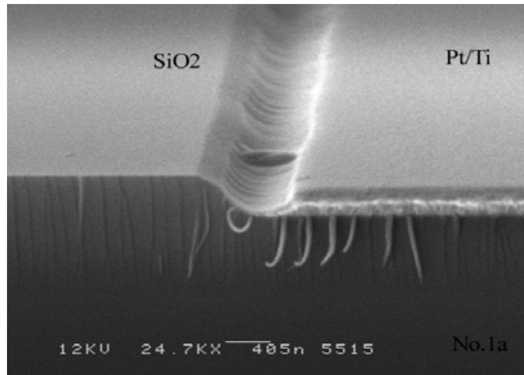
- AFM pictures of sample 2 and sample 3 are expected the same
- Ra is an average roughness of the as deposited metals
- Ra* is an average roughness of the Pt/Ti was sputtered directly onto clean SiO_2/Si substrate in the same conditions

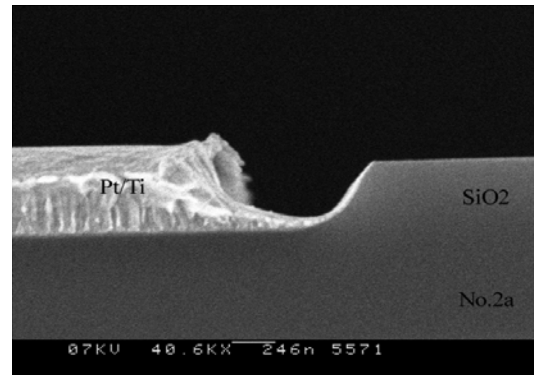
- R is a resistance of the deposited metals that patterned by lift-off
- R* is a resistance of the Pt/Ti was sputtered directly onto clean SiO_2/Si substrate in the same conditions

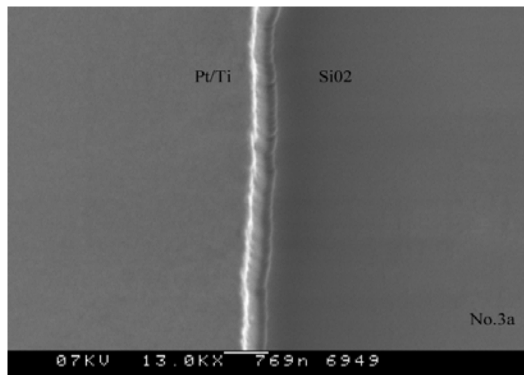
III. Results and discussion

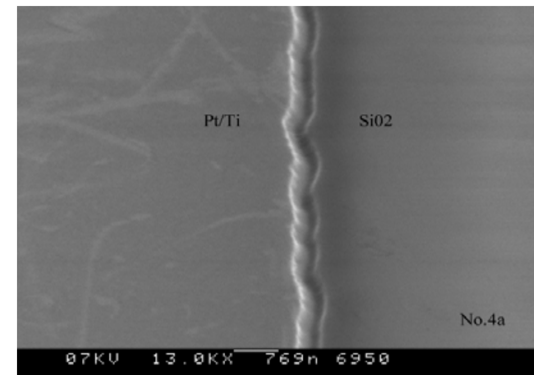
1. Metals deposited at different K ratios

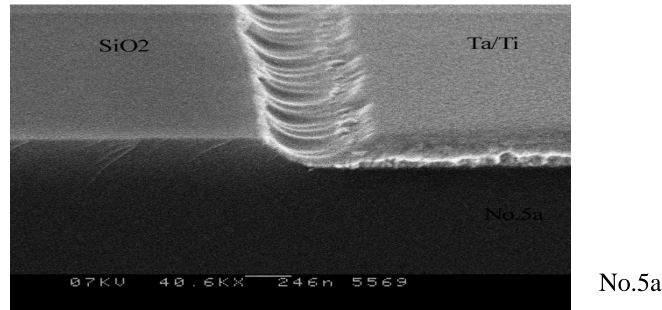
Many layers of Pt/Ti at different K ratios were deposited and patterned . After removing photoresist in acetone supported by ultrasonic, samples were divided into small pieces and took to investigate by SEM. SEM pictures of the samples 1 to 5 are shown in figure 3, with No.1a to No.5a, respectively. As can be seen from SEM that no ears or islands of Pt is remained at the edges of membrane. SEM pictures also demonstrate that the metals were well defined with the wide range of K ratios.











No.5a

Fig.3. SEM pictures of the as deposited layers using the modified lift-off technique.

Depending on situations and purposes of applications one has to use some kind of materials and in many cases etching to define wanted structures is necessary. For instance, during device fabrication one need sometimes to etch Ta, Ta_2O_5, W or Au. Of course, these metals can be etch by wet or dry method but it is hardly to etch them all away or not convenient to carry out (11,21) As in the case of Pt dry etching, redeposition of Ta also happened. Thus, we utilized the technique to pattern for other metals and the results are promising. Picture No.5a shows Ta was successfully patterned by this technique .

2. Roughness and resistance of as deposited metals

In lift-off technique one is able to consider that a photoresist layer is patterned and used as a closed shadow mask. However, the use of organic photoresist tends to leave organic residue behind which maybe have influences to the as-deposited thinfilm (22). These influences to quality of thinfilm are characterized in terms of its roughness and resistance. The roughness and resistivity of as-deposited Pt/Ti thinfilms were compared to those in which Pt/Ti was sputtered directly onto clean SiO_2/Si substrate in the same conditions. The roughness and resistance were measured by Dimension 3100 Atomic Force Microscope (AFM) and Matheson Resistivity Prober, respectively. The differences between two cases are also shown in table1.

And AFM pictures of surface roughness of as-deposited Pt/Ti thinfilms are shown in figure5, with number No.1b to No.4b, respectively.

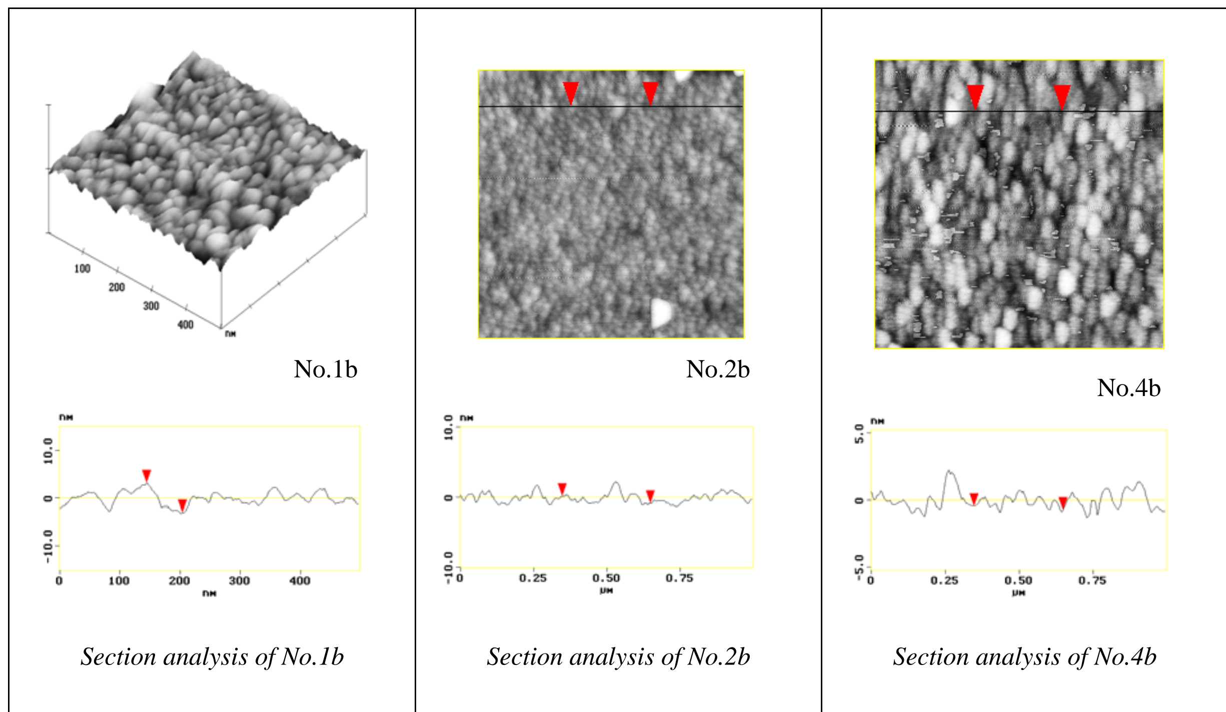


Fig.4. AFM surface measurements

From the beyon data we see that the resistance and roughness of the lift-off deposited Pt/Ti thinfilms are always higher than those of normal sputtering Pt/Ti thinfilms are. But the differences are quite small and not to be considered. The maximum of peak height is always small than 10 nm.

IV. Conclusions

The normal, low-cost modified lift-off technique was investigated in detail. In this technique, SiO2 is removed partly to create underetching, which is necessary to prevent the formation of Pt ears at the edges of membrane .The results shows that this technique was

applied to deposit and pattern Pt successfully . Moreover, the results for other materials seem promising. The wide range of K ratios was investigated and the successful results demonstrate that the method can be utilized flexibly.

In this study, the influences of residue organic to roughness and resistivity of lift-off deposited thinfilm were investigated. Fortunately, the influences are very small and it is not necessary to take in to account .

All above results allow us to conclude that the modified lift-off can be come a powerful mean of depositing and patterning for Pt as well as some materials.

The results of the research have been applied to pattern successfully Pt electrodes for Silicon Load Cell Sensors in our lab (23).

Acknowledgements

The STW foundation is kindly for financial support. Our thanks are also due to all staffs of MESA, University of Twente for technical supports, especially to Bert Otter for AFM and SEM measurements.

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