(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 October 2004 (07.10.2004)

PCT

(10) International Publication Number
WO 2004/086615 A1

(51) International Patent Classification[7]: H03G 3/00, 7/00, H03M 7/00

(21) International Application Number: PCT/IB2004/050324

(22) International Filing Date: 24 March 2004 (24.03.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03100799.0 27 March 2003 (27.03.2003) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SCHINKEL, Daniel** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **VAN TUIJL, Adrianus, J., M.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **NUIJTEN, Petrus, A., C., M.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

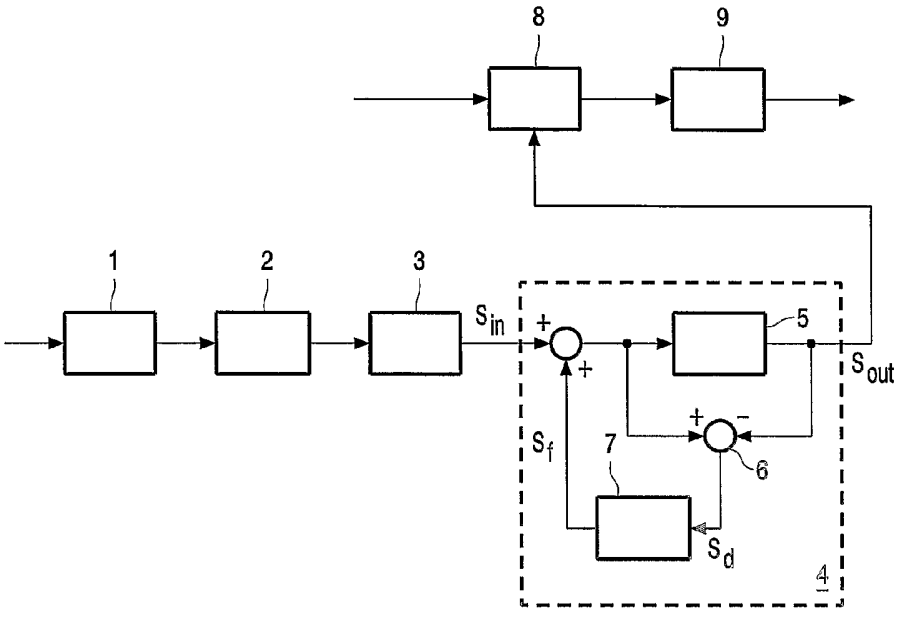
(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK,

[Continued on next page]

(54) Title: VOLUME CONTROL DEVICE FOR DIGITAL SIGNALS



(57) Abstract: A digital volume control device comprises a logic unit for volume control of digital input signals. Successively supplied m-bits words with maximally k bits active, derived from the output signals of or supplied by a volume control (4) with a quantizer (5) element the filtered m-bits workds are passed, however, with only the j most significant active bits of these filtered signals. The noise shaper operates with a frequency that is a k/j-fold of the frequency by which the m-bits words are supplied. An up-sampler (3) is provided for operation frequency adjustment of the filtered m-bits words to the noise shaper. This operation frequency is at least a factor k/j greater than the sample rate of the digital input signals. The control signals for the logic unit are formed by the m-bits words passed by the quantizer.

WO 2004/086615 A1

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Volume control device for digital signals

The invention relates to a digital volume control device and particularly to a volume control device for digital audio signals, comprising a logic unit to which digital input signals to be controlled are supplied and which provides for volume controlled digital output signals, the volume control of said digital input signals being determined by control signals, derived from output signals of a volume control element.

The volume control element can have the form of a manually controlled device, as may be the case in audio apparatus, it can be part of an automatic volume control or a computer which provide for the output signals from which the control signals are derived.

On the current market various volume control devices for digital audio signals are available, sometimes implemented in software and executed on a digital signal processor or implemented in hardware, often integrated together with other signal processing blocks. In practice, digital volume control devices implemented in hardware have a logic unit in the form of a multiplier, in which the multiplication word-length is quite large. When, for example, pulse code modulated (PCM) audio input signals with a common word-length of 24 bits are applied and the volume of these audio input signals must be controlled in a range between about –83 dB and about +11,5 dB, a control signal must be applied of at least 18 bits in order to obtain a 2 dB resolution over the entire control range. To obtain a 1,5 dB resolution over the entire control range at least a 20-bits control signal is required. However, a multiplication of a 24-bits audio input signal with an 18 or 20-bits control signal requires a large and relatively expensive multiplier. Further, during volume transitions, i.e. the dynamic mode of the volume control device, even a resolution of about 1,5 dB is not sufficient to avoid audible 'clicks'.

A digital volume control device as described in the opening is known from US-A-6,405,092. The logic unit in said patent specification is, in a first embodiment, formed by a bit-shifter, whereas by means of control signals the supplied words may be bidirectionally shifted. This means that only a 6 dB resolution is obtained. To obtain a more fine resolution, for example 1,5 dB, in a further embodiment in said patent specification a

multiplier is used with adders to add a number of shifted input words, while during volume transitions with 1,5 dB volume steps clicks will still be audible.

The purpose of the invention is to provide for a digital volume control device in which a large and expensive multiplier is avoided and a high resolution in volume control is obtained.

Therefore, according to the invention the digital volume control device as described in the opening paragraph is characterized in that the digital volume control device further comprises

- conversion means for receiving the control signal in the form of a succession of m-bits words having k active bits at a first sample frequency and converting the control signal into an intermediate comprising a succession of m-bits words having j active bits at a second sample frequency at least k/j greater than the first sample frequency;
- averaging means for generating an multiplied signal by multiplying the intermediate signal with the digital input signal and generating the output signal by averaging the multiplied signal.

Particularly, when the quantizer is designed to supply m-bits words with only the most significant active bit of the words supplied to the noise shaper, i.e. the case wherein j=1, the logic unit may be constituted by a simple shift register. In such a case, instead of a complicated multiplication, only a number of successive shift operations can be carried out. With a value j = 2 or 3 simple multiplications in the logic unit are still necessary.

An advantage of the application of the low-pass filter is that audible clicks are avoided. During volume transitions a large number of volume steps, much smaller than for example the 1,5 dB volume steps occur. While in the stationary state for example 1,5 dB steps occur, in the dynamic state, i.e. during volume transitions, the low-pass filter introduces much smaller volume steps.

Often, in audio systems oversampled digital input signals are available. With, for example, a standard sample-rate for a CD-player of a value f_s of about 44,1 kHz and because digital input signals in other parts of the audio system require a sample-rate of about 11 MHz, i.e. $256*f_s$, besides an amplitude-resolution a time-resolution may be possible. When the low-pass filter runs at a clock-frequency of $64*f_s$, the up-sampler can provide for words at a four times higher frequency, i.e. $256*f_s$. This means that during each four clock periods of the up-sampler one signal formed by a low-pass filtered signal and three signals consisting of only zero's are supplied to the noise shaper, so that by successively generating four multiplication factors in time consisting of powers of 2, an average multiplication can be

obtained corresponding with a desired multiplication factor. A desired multiplication, corresponding with a fine volume control resolution, as is the case with complicated multipliers, is thus realized by only a number of successive shift operations without use of adders.

The invention does not only relate to a digital volume control device, but also to an audio apparatus comprising such a digital volume control device.

The invention will further be explained by the following description of some preferred embodiments and with reference to the accompanying drawings:

Fig. 1 shows a block diagram of an embodiment of a digital volume control according to the invention;

Fig. 2 shows diagrams to further elucidate the operation of this block diagram.

In the block diagram of Fig. 1 showing a volume control device for digital audio signals a dB-to-linear decoder is indicated with reference number 1. To this decoder input signals are supplied in the form of n-bits words coming from a hand operated volume control element for digital audio input signals and covering a predetermined volume range. When, for example, these input signals are formed by 6-bits words and cover a volume range of about 94,5 dB, from –83 to +11,5 dB, they have a resolution of about 1,5 dB. In the decoder 1 the n-bits words, covering a logarithmical scale, are decoded to output signals formed by m-bits words with m>>n, covering a linear scale. To maintain the resolution of 1,5 dB over at least the whole volume range in the present example, the output signals may be formed by 20-bits words, with k=4 bits (4 one's) maximally active.

00000000001101100000, corresponding with	58,7 dB
00000000010000000000	60,2 dB
00000000010011000001	61,7 dB
00000000010110100000	63,2 dB
00000000011011000000	64,7 dB
00000000100000000000	66,2 dB

In this and the following examples the above values are taken with reference to a 0 dB value. The real volume value must be diminished with a value of –83 dB.

The output signals of the decoder 1 are supplied to a low-pass filter 2. From the point of view of costs saving a first order IIR (infinite impulse response) filter is used. Nevertheless higher order IIR filters are acceptable.

To obtain slow volume changes, the low-pass filter 2 has a cut-off frequency of 3,5 Hz and is further so designed that, some time after the start of a volume transition, its output signal will always reach a value equal to that of its input signal. By this measure the output signal of the low-pass filter shall still contain words with, in the stationary state, only 4 bits active maximally. Not only IIR filter are applicable, but also FIR (finite impulse response) filters can be used. The length of such filters is dependent on the cut-off frequency. For low values of the cut-off frequency, as is the case in this embodiment, a relatively long filter, i.e. a filter with a large number of filter coefficients, must be used, which can be considered as a disadvantage.

Next, the output signals of the low-pass filter 2 are supplied to a pure up-sampler 3 wherein the volume gain is up-sampled with a factor 4. The up-sampler produces one sample equal to the input every 4^{th} clock period and the other clock periods samples with value zero. The up-sampling factor 4 is chosen in connection with the maximal number of active bits in the 20-bits words of the present example as will be clear after having explained the operation of the following stage, the noise shaper 4 to which the samples from the up-sampler are supplied.

The noise shaper 4 is formed by a quantizer 5 and a feed back loop 6 with a one clock cycle delay element 7 to feed back the difference between the input signal ($S_{in} + S_f$) and the output signal (S_{out}) of the quantizer, i.e. the error signal (S_d), to the input of the noise shaper (S_{in}). The sum of the input signal of the noise shaper and the delayed error signal (S_f) will be used to feed the quantizer in the subsequent clock cycle. In this example, in the quantizer only the most significant active bit will be passed, while the other bits of the 20-bits words will be made zero. In the stationary state the operation of the noise shaper will be clear by looking to the signals S_{in}, S_{out}, S_d, and S_f in subsequent clock periods t_0, t_1, t_2 and t_3:

	t_0	S_f	=	0000000000000000000
		S_{in}	=	0000000010011000001 (61,7 dB)
		$S_f + S_{in}$	=	0000000010011000001
		S_{out}	=	0000000010000000000
		S_d	=	0000000000011000001
	t_1	S_{in}	=	0000000000000000000
		$S_f + S_{in}$	=	0000000000011000001
		S_{out}	=	0000000000010000000
		S_d	=	0000000000001000001
	t_2	S_{in}	=	0000000000000000000
		$S_f + S_{in}$	=	0000000000001000001
		S_{out}	=	0000000000001000000
		S_d	=	0000000000000000001
	t_3	S_{in}	=	0000000000000000000
		$S_f + S_{in}$	=	0000000000000000001
		S_{out}	=	0000000000000000001
		S_d	=	0000000000000000000

Thus, after 4 clock periods the error signal is zero again and a next cycle of 4 clock periods can begin. The output signals of the noise shaper 4 in these 4 clock-periods are:

0000000010000000000

0000000000010000000

0000000000001000000

0000000000000000001

These output signals form the multiplication factors by means of which the volume of, for example, a 24-bits audio signal is controlled. These multiplication factors are generated with a frequency of, in this example, four times the frequency with which the digital input signals are supplied to the volume control device. In the stationary state this sequence of multiplication factors will be repeated and is illustrated in fig. 2A. Instead of a multiplication of the 24-bits audio signal with a 20-bits multiplication factor, the multiplication is reduced to four multiplications with words having only one active bit. Instead of a logic unit in the form of a complicated multiplier, the logic unit can now be constituted by a simple shift register (barrel shifter) 8 with 20 shift positions in which successive shift operations are performed. With the multiplication factors as indicated in fig. 2A and a digital input signal

indicated in fig. 2B, the output signal of the shift register is as indicated in fig. 2C. It is emphasized that these figures only show a stationary state, i.e. a state wherein no volume transitions occur.

In the present example, only the 28 most significant bits of the shift register 8 are passed. By means of the low-pass filter 9, which may be carried out as a first order IIR filter, the output words of the bitshifter 8 are filtered and reduced again to 24-bits words. Higher order IIR filters or a FIR filter are possible too. When a FIR filter is applied, the output signal thereof is as indicated in fig. 2D. When a 1st order IIR filter is used some high frequency components will still be present.

In the stationary state the 4-cycle multiplication process is functionally equivalent to an up-sampling of the digital input signals from $64*f_s$ to $256*f_s$, followed by a 4-taps FIR filter. Such a conceptual FIR filter does not suppress frequencies around $64*f_s$ and $128*f_s$ if its coefficients are arranged in this fashion with the largest values first, followed by decreasing values. Thus the output contains aliases around $64*f_s$ and $128*f_s$, which are filtered when an additional IIR or FIR filter 9 is used.

In case of a volume transition, for example a 4,5 dB transition, from:
00000000001001100001 (55,5 dB) to
00000000010000000000 (60 dB),
the low-pass filter 2 realizes a gradual volume change in order to eliminate audible artefacts during the volume transition. This means that the filter output signal will be formed by a relatively long sequence of 24-bits words with values between the above two transition values, which words can have also more than 4 active bits. This means that, in general, each time after 4 clock periods, the error signal S_d will not be zero.

When at a certain moment, directly before the end value 00000000010000000000 is reached, the signal $S_f + S_{in}$ is 00000000001111111111, the signals S_{in}, S_{out}, S_d, and S_f in subsequent 4 clock periods will be:

	t_0	$S_f + S_{in}$	=	00000000001111111111
		S_{out}	=	00000000001000000000
		S_d	=	00000000000111111111
	t_1	S_{in}	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000111111111
		S_{out}	=	00000000000100000000
		S_d	=	00000000000011111111
	t_2	S_{in}	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000011111111
		S_{out}	=	00000000000010000000
		S_d	=	00000000000001111111
	t_3	S_{in}	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000001111111
		S_{out}	=	00000000000001000000
		S_d	=	00000000000000111111

and a new series of 4 clock periods will start, taking into account the error of the passed 4 clock periods:

	t_0	S_{in}	=	00000000010000000000
		$S_f + S_{in}$	=	00000000010000111111
		S_{out}	=	00000000010000000000
		S_d	=	00000000000000111111
	t_1	S_{in}	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000000111111
		S_{out}	=	00000000000000100000
		S_d	=	00000000000000011111
	t_2	Sin	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000000011111
		S_{out}	=	00000000000000010000
		S_d	=	00000000000000001111
	t_3	Sin	=	00000000000000000000
		$S_f + S_{in}$	=	00000000000000001111
		S_{out}	=	00000000000000001000
		S_d	=	00000000000000000111

Although the output of the low-pass filter 2 has reached its stationary state, there is still an error signal S_d. This error signal will disappear in the next four clock periods:

t_0	Sin	=	00000000010000000000
	$S_f + S_{in}$	=	00000000010000000111
	S_{out}	=	00000000010000000000
	S_d	=	00000000000000000111
t_1	S_{in}	=	00000000000000000000
	$S_f + S_{in}$	=	00000000000000000111
	S_{out}	=	00000000000000000100
	S_d	=	00000000000000000011
t_2	Sin	=	00000000000000000000
	$S_f + S_{in}$	=	00000000000000000011
	S_{out}	=	00000000000000000010
	S_d	=	00000000000000000001
t_3	Sin	=	00000000000000000000
	$S_f + S_{in}$	=	00000000000000000001
	S_{out}	=	00000000000000000001
	S_d	=	00000000000000000000

Now, the noise shaper has reached its stationary state. The output signals of the noise shaper are successively:

00000000001000000000
00000000000100000000
00000000000010000000
00000000000001000000
00000000010000000000
00000000000000100000
00000000000000010000
00000000000000001000
00000000010000000000
00000000000000000100
00000000000000000010
00000000000000000001

and further as in the stationary state:

0000000001000000000
0000000000000000000
0000000000000000000
0000000000000000000
0000000001000000000
0000000000000000000
etc.

Again the multiplication factors are powers of 2, so that the volume transition is realized by only a time-sequence of shift operations.

In another case of a volume transition, for example a -4,5 dB transition, from:
0000000001000000000 to
0000000000001001100001

the low-pass filter 2 again realizes a gradual volume change in order to eliminate audible artefacts during the volume transition. This means again that the filter output signal will be formed by a relatively long sequence of 24-bits words with values between the above two transition values, which words can have also more than 4 active bits.

When at a certain moment, directly before the end value 0000000000001001100001 is reached, the signal $S_f + S_{in}$ is 0000000000001001100010, the signals S_{in}, S_{out}, S_d, and S_f in subsequent 4 clock periods will be:

t_0	$S_f + S_{in}$	=	0000000000001001100010
	S_{out}	=	0000000000001000000000
	S_d	=	0000000000000001100010
t_1	S_{in}	=	0000000000000000000000
	$S_f + S_{in}$	=	0000000000000001100010
	S_{out}	=	0000000000000001000000
	S_d	=	0000000000000000100010
	t_2 S_{in}	=	0000000000000000000000
	$S_f + S_{in}$	=	0000000000000000100010
	S_{out}	=	0000000000000000100000
	S_d	=	0000000000000000000010
	t_3 S_{in}	=	0000000000000000000000
	$S_f + S_{in}$	=	0000000000000000000010
	S_{out}	=	0000000000000000000010
	S_d	=	0000000000000000000000

and the error signal is zero again, while the stationary state is reached.

In the present example k is chosen 4, while 20-bits words with only the most significant bit of the supplied m-bits words is passed by the quantizer, the other bits being made zero, i.e. the case wherein j=1.

It will be clear that other values of k are possible. With the maximum number of active bits k=3, transitions in steps of about 2 dB will be possible with the following 20-bits control words:

00000000000100000000, corresponding with about	48 dB
00000000000101000100	50 dB
00000000000110010000	52 dB
00000000001000000000	54 dB
00000000001010001 000	56 dB

In this case the up-sampler inserts between two successive 20-bits filtered words only two 20-bits words consisting of zero's, while the operation frequency of the noise shaper is 3 times the frequency with which the dB-to-linear decoder 1 generates the 20-bits control signals. Other k-values will be possible depending on the desired step size of the volume control transitions.

In the preferred embodiment the output words of the noise shaper have only one active bit (j=1). Nevertheless two or more active bits will be possible (j=2 or more). With k=4 and j=2 in a cycle of 2 clock periods two active bits in the output words of the noise shaper imply 2 times a simple multiplication, to obtain an average multiplication corresponding with a desired multiplication of the digital input signals.

When the volume range is smaller than about 94 dB, the output words of the dB-to-linear decoder can comprise less than 20 bits. When this volume range is larger than about 94 dB even more than 20 bits may be necessary, of course depending on the desired volume step size.

This type of volume control is applicable when a volume control implemented in hardware is needed. A clock frequency of at least k/j times the input sample rate (with k and j as defined above) is required for its operation. Possible application areas include sigma-delta D/A converters and digital audio-amplifiers, because the devices use oversampled signals and often lack a signal processing core with a multiplier. The dynamic volume control does not need a multiplier and can be integrated with very few hardware elements and thus low chip-area. The volume control can handle all common types of current signal formats,

such as signals coming from a CD-, DVD- or SACD source, provided that the available clock frequency is high enough.

Although in the embodiments discussed comprise a noise-shaper, it will be clear to a person skilled in the art that other bit-stream converters, such as sigma-delta modulators may be used instead.

CLAIMS:

1. A digital volume control device to which a digital input signal to be controlled is supplied which provides for a volume controlled digital output signal, the volume control of said digital input signal being determined by a control input signal, characterized in that the digital volume control device further comprises:

- conversion means for receiving the control signal in the form of a succession of m-bits words having k active bits at a first sample frequency and converting the control signal into an intermediate comprising a succession of m-bits words having j active bits at a second sample frequency at least k/j greater than the first sample frequency;
- averaging means for generating an multiplied signal by multiplying the intermediate signal with the digital input signal and generating the output signal by averaging the multiplied signal.

2. A digital volume control device as claimed in claim 1, characterized in that the conversion means comprises an up-sampler for up-sampling of the control signal and a bit-stream converter for converting the up-sampled control signal into the intermediate signal.

3. A digital volume control device as claimed in claim 2, characterized in that the bit-stream converter is a noise-shaper having a combiner for generating an m-bit combination signal by combining the control signal with an m-bit error signal, a quantizer for generating the intermediate signal by passing-on only the j most significant bits of the combination signal setting the remaining bits to zero, and a feed back loop for generating the error signal out of the quantizer errors.

4. A digital volume control device as claimed in any of the claims 1 to 3, characterized in that $j = 1$, whereas the averaging means comprises a shift register for multiplying the intermediate signal with the digital input signal.

5. A digital volume control device as claimed in any of the claims 1 to 4, characterized in that the conversion means comprises a low-pass filter is provided for filtering the control signal before up-sampling.

6. A digital volume control device as claimed in claim 5, characterized in that the low-pass filter is an infinite impulse response filter.

7. A digital volume control device as claimed in any of the claims 1 to 6, characterized in that the averaging means comprise a low-pass output filter.

8. A digital volume control device as claimed in claim 7, characterized in that the low-pass output filter is a infinite impulse response filter.

9. A digital volume control device as claimed in claim 7, characterized in that an up-sampler is provided for up-sampling the digital input signal with a factor k/j, and the low-pass output filter is formed by a finite impulse response filter having k/j taps.

10. A digital volume control device as claimed in any of the claims 1 to 9, characterized in that a dB-to-linear decoder is provided for generating the control signal in dependence upon an n-bit logarithmic control signal.

11. A digital volume control device as claimed in claim 10, characterized in that the output signal of the volume device covers a range of about 94 dB, whereas $n = 6$, $m = 20$, and $k = 4$.

12. An audio apparatus comprising a digital volume control device according to any of the preceding claims.

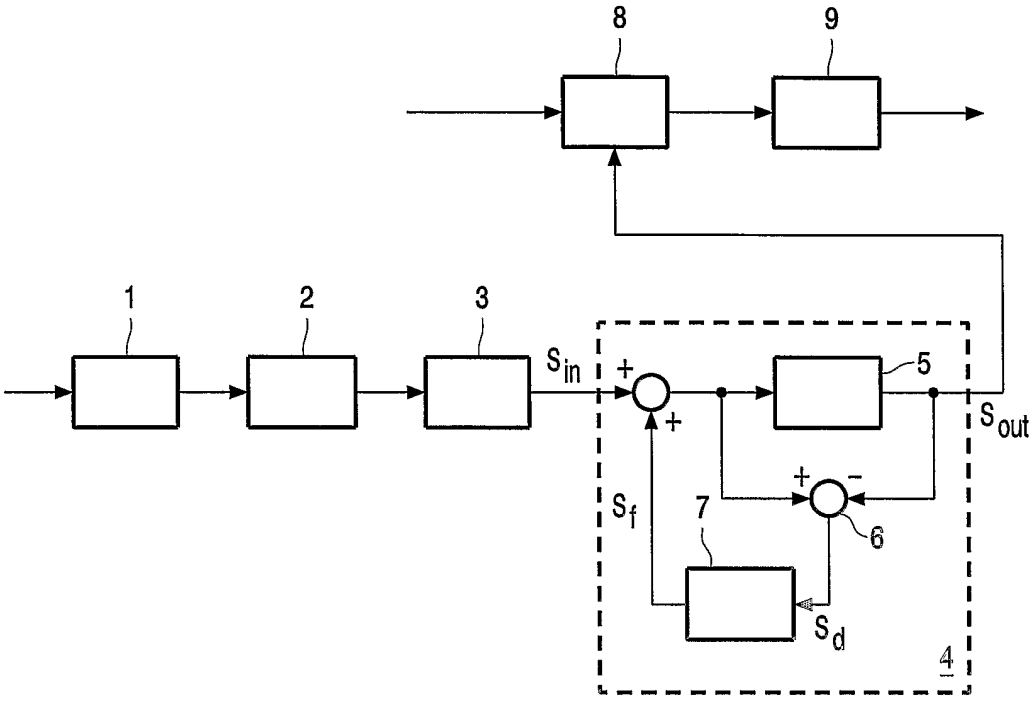


FIG. 1

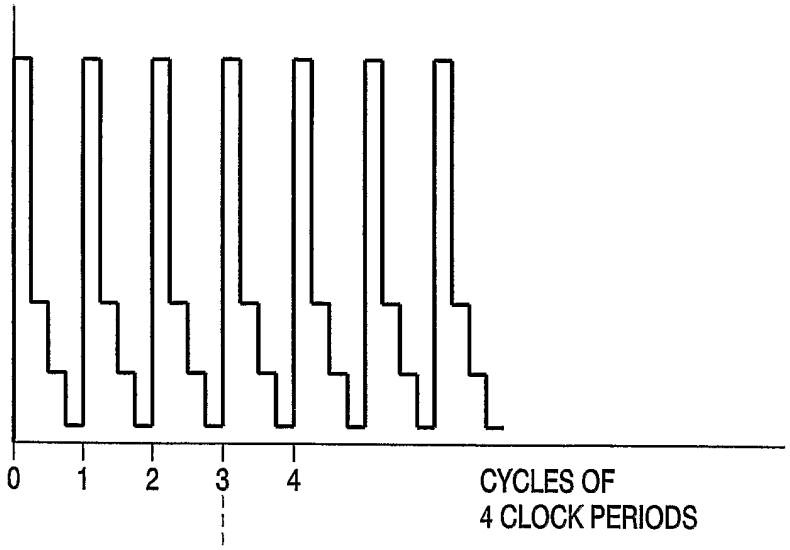


FIG. 2A

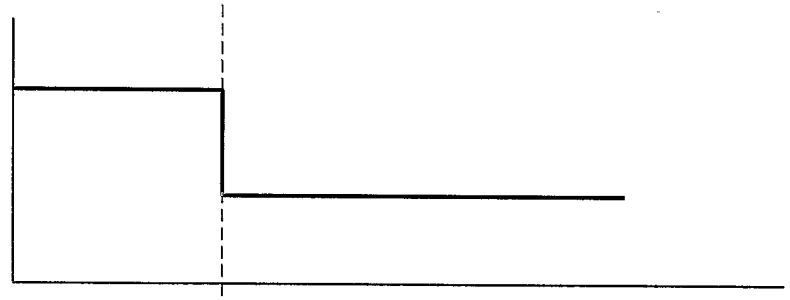


FIG. 2B

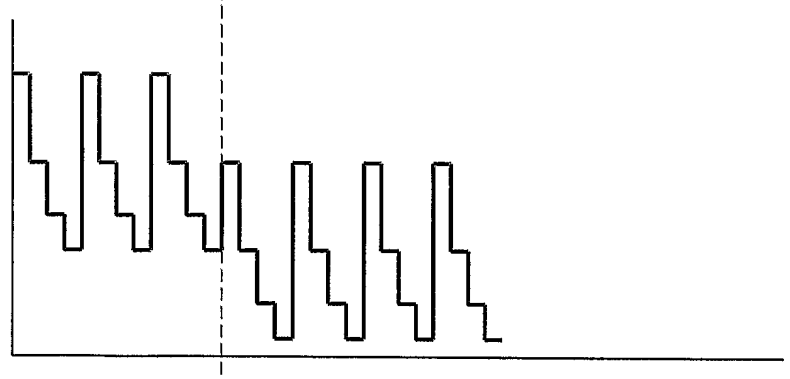


FIG. 2C

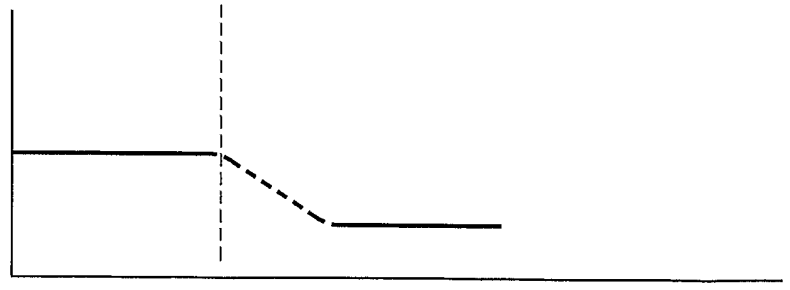


FIG. 2D

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2004/050324

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03G3/00 H03G7/00 H03M7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 482 927 A (NIPPON ELECTRIC CO) 29 April 1992 (1992-04-29) figure 1	1-12
A	US 6 405 092 B1 (OXFORD WILLIAM VINCENT) 11 June 2002 (2002-06-11) cited in the application figure 3	1-12
A	"STEREO DIGITAL VOLUME CONTROL A CRYSTAL SEMICONDUCTOR APPLICATIONS" ELEKTOR ELECTRONICS, ELEKTOR PUBLISHERS LTD. CANTERBURY, GB, vol. 22, no. 243, 1 April 1996 (1996-04-01), pages 46-47,49, XP000583422 ISSN: 0268-4519 figure 2	1-12

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 July 2004	09/08/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Winkler, G

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2004/050324

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 40 36 730 A (THOMSON BRANDT GMBH) 21 May 1992 (1992-05-21) abstract; figure 1	1-12
A	EP 0 887 797 A (THOMSON BRANDT GMBH) 30 December 1998 (1998-12-30) abstract	1-12
A	MACSORLEY O L: "HIGH-SPEED ARITHMETIC IN BINARY COMPUTERS" PROCEEDINGS OF THE INSTITUTE OF RADIO ENGINEERS, IEEE INC. NEW YORK, US, vol. 49, no. 1, January 1961 (1961-01), pages 67-91, XP001002205 page 72, left-hand column, line 27 - line 42	12
A	US 4 566 076 A (VAN DER STEEN ANTONIE C A M) 21 January 1986 (1986-01-21) abstract; figure 2	1-12

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB2004/050324

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0482927 A	29-04-1992	JP 2671595 B2	29-10-1997
		JP 4160844 A	04-06-1992
		AU 638362 B2	24-06-1993
		AU 8674791 A	30-04-1992
		CA 2054173 A1	26-04-1992
		DE 69110103 D1	06-07-1995
		DE 69110103 T2	04-01-1996
		EP 0482927 A2	29-04-1992
		US 5533064 A	02-07-1996
US 6405092 B1	11-06-2002	NONE	
DE 4036730 A	21-05-1992	DE 4036730 A1	21-05-1992
EP 0887797 A	30-12-1998	DE 19727133 A1	07-01-1999
		CN 1204124 A ,C	06-01-1999
		EP 0887797 A2	30-12-1998
		JP 11146233 A	28-05-1999
		US 6654471 B1	25-11-2003
US 4566076 A	21-01-1986	NL 8100307 A	16-08-1982
		CA 1184304 A1	19-03-1985
		DE 3200895 A1	12-08-1982
		ES 8305542 A1	01-07-1983
		FR 2498848 A1	30-07-1982
		GB 2091918 A ,B	04-08-1982
		IE 52516 B1	25-11-1987
		IT 1149711 B	10-12-1986
		JP 1768160 C	11-06-1993
		JP 4045859 B	28-07-1992
		JP 57145415 A	08-09-1982