(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 June 2003 (12.06.2003)

PCT

(10) International Publication Number
WO 03/049280 A1

(51) International Patent Classification[7]: H03F 1/30, 3/193

(21) International Application Number: PCT/IB02/05024

(22) International Filing Date:
26 November 2002 (26.11.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
01204748.6 7 December 2001 (07.12.2001) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ANNEMA, Anne, J.** [NL/NL]; Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL). **LEENAERTS, Dominicus, M., W.** [NL/NL]; Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL). **DE VREEDE, Petrus, W., H.** [NL/NL]; Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

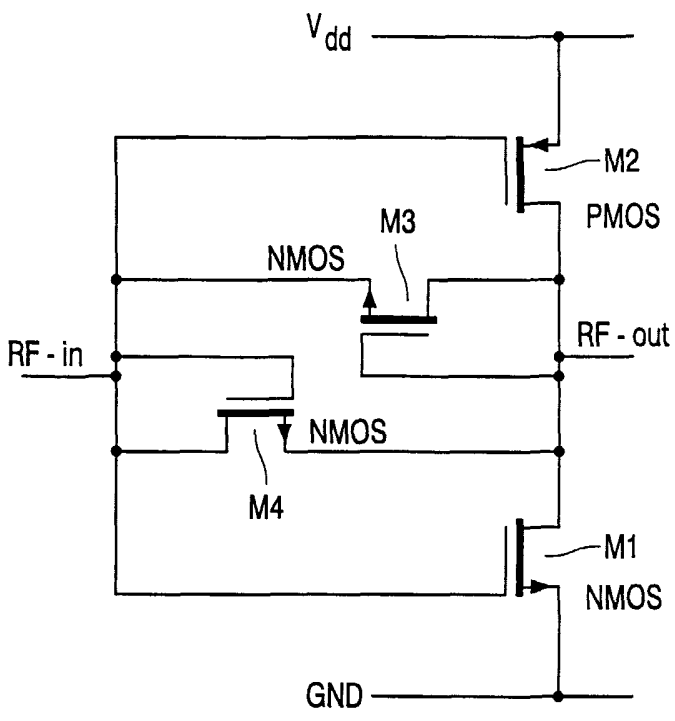
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: A LOW NOISE ELECTRONIC CIRCUIT



(57) Abstract: An electronic circuit, which can be used as a Low Noise Amplifier (LNA), comprises two complementary Field Effect Transistors (M1, M2; M5, M6), each having a gate, a source and a drain. The gates are connected together as a common input terminal, and the drains are connected together as a common output terminal. The electronic circuit further has a feedback circuit, e.g. in the form of two anti-parallel Field Effect Transistors (M3, M4; M7, M8), connected between the common input terminal and the common output terminal. This feedback circuit has an impedance at radio frequencies which is high-ohmic compared to impedance levels of the two transistors. This ensures a high gain at radio frequencies, and at the same time it can be implemented with only a few components. It also ensures high linearity and a very low current in the feedback circuit, and thus little or no noise is added to the circuit.

WO 03/049280 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A low noise electronic circuit

The invention relates to an electronic circuit comprising two complementary Field Effect Transistors, each having at least a gate terminal, a source terminal and a drain terminal, wherein the gate terminals of the two transistors are connected together as a common input terminal, and the drain terminals of the two transistors are connected together as a common output terminal. The invention also relates to the use of such an electronic circuit as a Low Noise Amplifier.

An electronic circuit of this type may e.g. be used as a Low Noise Amplifier (LNA), which is one of the main and key building blocks in any front-end telecommunications system, and which is also often found in radio systems. The purpose of such amplifiers is to amplify an input signal, which will normally be a radio frequency signal, while only a minimum of noise and distortion is added to the signal. Further, in order to relax the specifications for other components in a front-end device, it is important to have a linear LNA consuming as little power as possible. Thus LNAs are important components in e.g. radios, TV sets and telecommunications products.

Many prior art LNAs are based on the use of MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), and typically an input MOSFET is cascoded with a similar transistor in order to obtain sufficient gain and a good signal-to-noise ratio. An example of such an amplifier is disclosed in US 6 150 882, in which two pairs of cascoded MOSFETs are coupled as a differential amplifier in order to improve the gain, which is typically required. Alternatively, the gain may be improved by adding a further gain stage. However, in both cases the circuit tends to become rather complicated which results in a reduced signal-to-noise ratio and a higher power consumption. The complicated circuit with several components also means a higher cost. Further, the single cascoded pair of MOSFETs as well as two pairs coupled differentially require a relatively high supply voltage due to the stacking of the MOSFETs.

US 6 150 882 also shows a circuit comprising two complementary MOSFETs having their gate terminals connected together and their drain terminals connected together. The source terminals of the two MOSFETs are connected to the supply voltage and ground, respectively. This circuit, however, is only used as an inverter internally in the amplifier

circuit. It is not suited as an amplifier circuit in itself, because the DC operating point cannot be controlled.

Therefore, it is an object of the invention to provide a circuit of the above-mentioned type which is as simple as possible, i.e. uses only a minimum of components, resulting in low cost and low power consumption, and which also provides a low noise figure and a high linearity. Further, it should not require a high supply voltage.

According to the invention the object is achieved in that the electronic circuit further has a feedback circuit connected between the common input terminal and the common output terminal, said feedback circuit having an impedance at radio frequencies which is high-ohmic compared to impedance levels of the two transistors. The feedback circuit having a high-ohmic impedance ensures a DC operating point without influencing the RF performance due to the high impedance level of this feedback circuit, and at the same time it can be implemented with only one or a few components. The high impedance of the feedback circuit also ensures a very low current in the feedback circuit, and thus little or no noise is added to the circuit. Further, the circuit does not require a high supply voltage, because only two transistors are stacked.

In one embodiment, which is stated in claim 2, the feedback circuit comprises a high-ohmic resistor, which has the advantage that the feedback circuit can be implemented with a single component.

In another embodiment, which is stated in claim 3, the feedback circuit comprises two transistors connected in anti-parallel to each other. In e.g. integrated circuits semiconductor components are often more expedient to use than e.g. a resistor. Further, this embodiment provides a better stabilization of the DC bias voltage. As stated in claim 4, the two transistors of the feedback circuit may be Field Effect Transistors, which has the advantage that the entire circuit can be implemented with Field Effect Transistors. In this case the Field Effect Transistors of the feedback circuit may be P-channel MOSFETs, as stated in claim 5, or they may be N-channel MOSFETs, as stated in claim 6.

As mentioned, the invention also relates to the use of an electronic circuit of the type described above as a Low Noise Amplifier. Due to the advantages mentioned above, especially the low amount of noise added by the feedback circuit, the circuit is well suited for this application.

The invention will now be described more fully below with reference to the drawings, in which

Figure 1 shows an example of a circuit according to the invention,

Figure 2 shows a circuit similar to that of Figure 1, but with MOSFETs of P- and N-type exchanged,

Figure 3 shows the circuit of Figure 1 modified to use MOSFETs of P-type in the feedback circuit,

Figure 4 shows the circuit of Figure 1 modified to use bipolar transitors in the feedback circuit, and

Figure 5 shows a circuit according to the invention in which a resistor is used as a feedback circuit.

Figure 1 shows an example of how a circuit according to the invention can be implemented in a preferred embodiment. The two MOSFET transistors M1 and M2 are the amplifying elements. The MOSFET transistor M1 of N-type has its gate terminal connected to an input terminal RF-in, while its drain terminal is connected to an output terminal RF-out. The source terminal of M1 is connected to a ground terminal GND. Similarly, the MOSFET transistor M2 of P-type has its gate and drain terminals connected to the input terminal RF-in and the output terminal RF-out, respectively. The source terminal of M2 is connected to a supply voltage terminal Vdd.

A radio frequency input signal applied to the input terminal RF-in will thus be amplified by the two MOSFET transistors M1 and M2 and the amplified signal is presented on the output terminal RF-out. Due to the use of two complementary MOSFET transistors the coupling provides a high voltage gain.

Two other MOSFET transistors M3 and M4 of N-type constitute a bias circuit for the DC operating point by forming a feedback loop which sets the DC biasing voltages at the points RF-in and RF-out. The feedback loop is slow by using small low frequent transistors for it. Due to this feedback loop the DC bias voltage on the two points will be the same.

If the DC voltage at point RF-out increases, M3 starts conducting, which decreases the DC voltage at point RF-out. If the DC voltage at point RF-out decreases, M4 starts conducting which increases the DC voltage at point RF-out. This is ensured by the anti-parallel connection of M3 and M4. Because of this opposite behaviour, the DC voltage at point RF-in and RF-out will stabilize at such a value that the DC currents flowing through M1 and M2 are the same.

When the feedback loop has stabilized, no DC current flows through M3 and M4. The voltage at points RF-in and RF-out depends on the size of M1 and M2. If the width of the PMOS M2 is roughly a factor 2.5 to 3 greater than the width of the NMOS M1, then the DC voltage at the points RF-in and RF-out will be roughly half the supply voltage Vdd.

Because no DC currents flow through M3 and M4 when the feedback loop has stabilized, they do not add noise to the circuit. This makes the circuit suitable in low noise amplifier applications. As mentioned above, the circuit has a high voltage gain because both transistors M1 and M2 contribute to the amplification of the RF signal. Further, it has a low power consumption because M3 and M4 do not consume any current. The low number of components used in the circuit, actually only four MOSFETs, also results in a low production cost for the circuit.

In the ideal situation mentioned above, where the widths of M1 and M2 are selected so that the DC voltage at RF-out is half the supply voltage Vdd, the available voltage space is optimally used, which means that the voltage swing of the output signal has more headroom, resulting in a high linearity for the amplifier circuit.

As mentioned, the circuit is very suitable in low noise amplifier applications. However, it can be used in other applications as well. For example, it is usable in any application where an amplifier is needed. It can also be used as a bias circuit to generate a certain bias voltage that lies between Vdd and ground. This bias voltage can be set by changing the size of M1 and M2.

In Figure 1 the source terminal of N-type MOSFET M1 is connected to ground, while the source terminal of P-type MOSFET M2 is connected to the supply voltage. However, as shown in Figure 2, the P and N-type MOSFETs may also be exchanged. Here, the P-type MOSFET M5 is connected to ground while the N-type MOSFET M6 is connected to the (negative) supply voltage. The function of the circuit of Figure 2 is the same as that of Figure 1.

As shown in Figure 3, the two N-type MOSFETs M3 and M4 may also be changed to P-type MOSFETs M7 and M8. Again, one of the MOSFETs will conduct when the DC voltage at RF-out increases, while the other will conduct when the DC voltage at RF-out decreases. As a further alternative, which is shown in Figure 4, M3 and M4 may also be substituted by two bipolar transistors Q1and Q2. Transistor Q1 will conduct when the DC voltage at RF-out increases, while transistor Q2 will conduct when the DC voltage at RF-out decreases.

An alternative embodiment of the invention is illustrated in Figure 5. In this embodiment a high ohmic resistor is placed between the points RF-in and RF-out. This resistor will have the same function as M3 and M4, i.e. it will ensure that the DC voltages at RF-in and RF-out will stabilize to the same level. The general principle is making a (slow) feedback loop set the DC bias voltage at points RF-in and RF-out. The value of the resistor must be much higher than the impedance level of the circuit at radio frequencies, which is easily met.

Although a preferred embodiment of the present invention has been described and shown, the invention is not restricted to it, but may also be embodied in other ways within the scope of the subject-matter defined in the following claims.

CLAIMS:

1. An electronic circuit comprising two complementary Field Effect Transistors (M1, M2; M5, M6), each having at least a gate terminal, a source terminal and a drain terminal, wherein the gate terminals of the two transistors are connected together as a common input terminal, and the drain terminals of the two transistors are connected together as a common output terminal,
characterized in that the electronic circuit further has a feedback circuit (M3, M4; M7, M8; Q1, Q2; R1) connected between the common input terminal and the common output terminal, said feedback circuit having an impedance at radio frequencies which is high-ohmic compared to impedance levels of the two transistors.

2. An electronic circuit according to claim 1, characterized in that the feedback circuit comprises a high-ohmic resistor (R1).

3. An electronic circuit according to claim 1, characterized in that the feedback circuit comprises two transistors (M3, M4; M7, M8; Q1, Q2) connected in anti-parallel to each other.

4. An electronic circuit according to claim 3, characterized in that the two transistors of the feedback circuit are Field Effect Transistors (M3, M4; M7, M8).

5. An electronic circuit according to claim 4, characterized in that the Field Effect Transistors of the feedback circuit are P-channel MOSFETs (M7, M8).

6. An electronic circuit according to claim 4, characterized in that the Field Effect Transistors of the feedback circuit are N-channel MOSFETs (M3, M4).

7. Use of an electronic circuit according to any one of claims 1 to 6 as a Low Noise Amplifier.

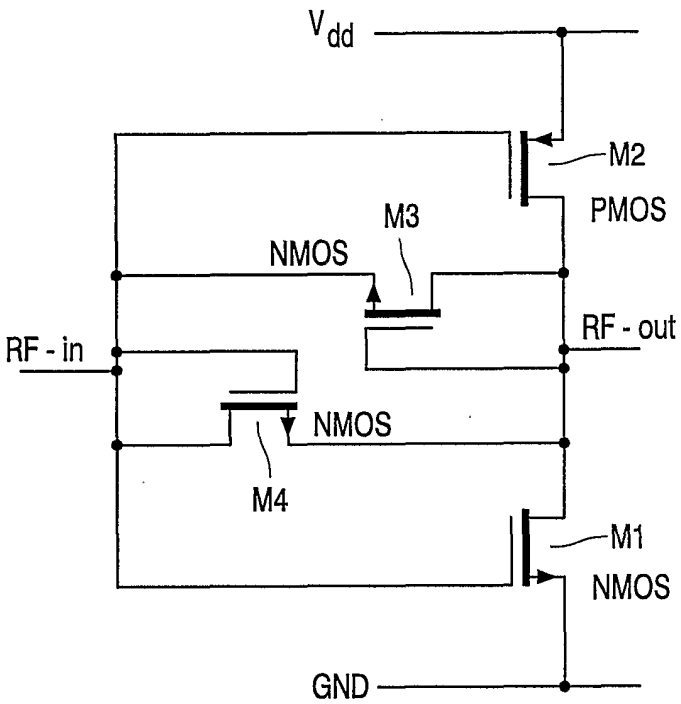

Vdd
M2
PMOS
M3
NMOS
RF - out
RF - in
NMOS
M4
M1
NMOS
GND

FIG. 1

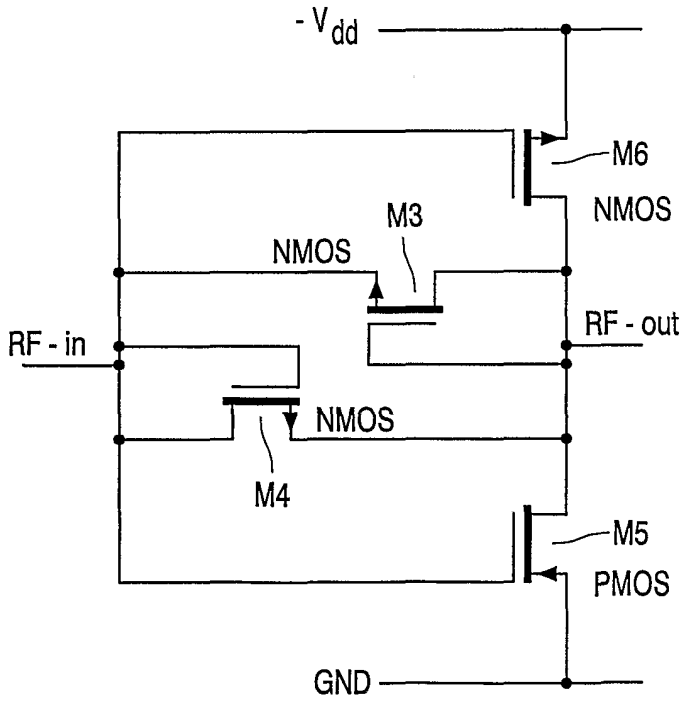

- Vdd
M6
NMOS
M3
NMOS
RF - out
RF - in
NMOS
M4
M5
PMOS
GND

FIG. 2

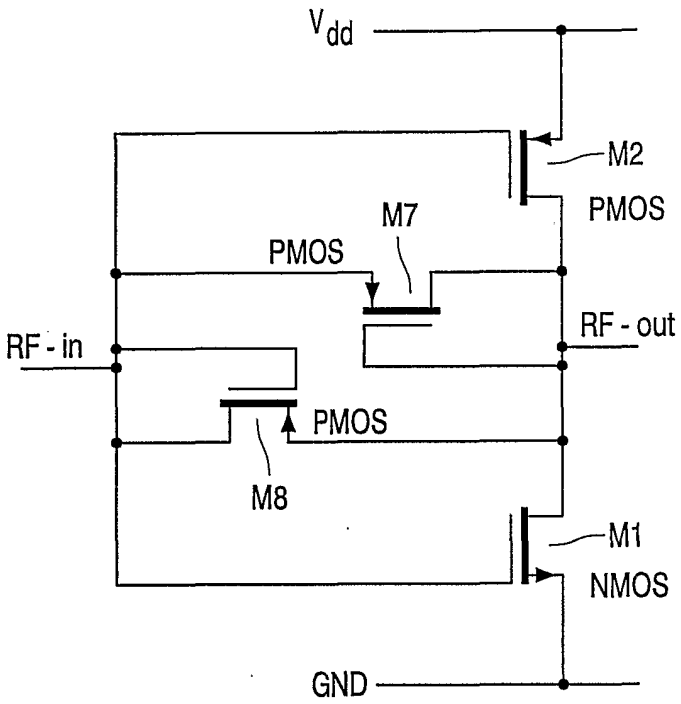

Vdd
M2
PMOS
M7
PMOS
RF - out
RF - in
PMOS
M8
M1
NMOS
GND

FIG. 3

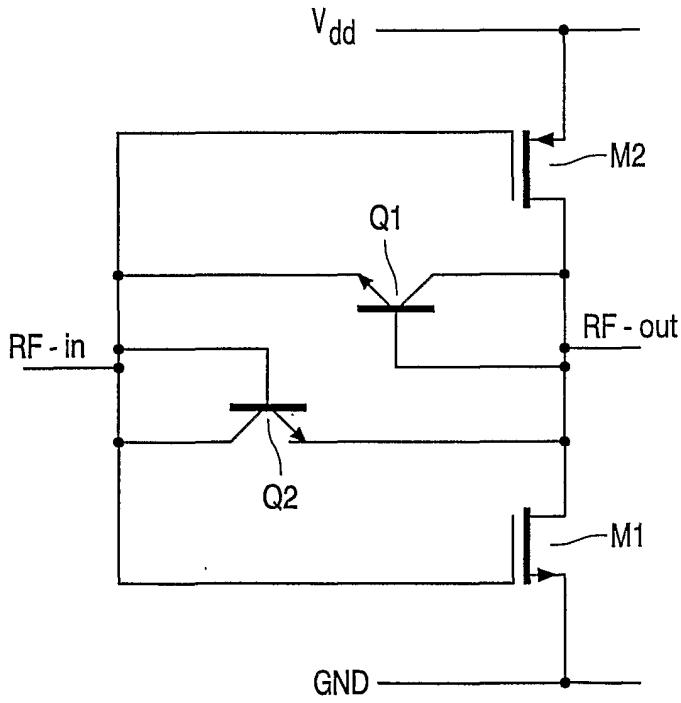

Vdd
M2
Q1
RF - out
RF - in
Q2
M1
GND

FIG. 4

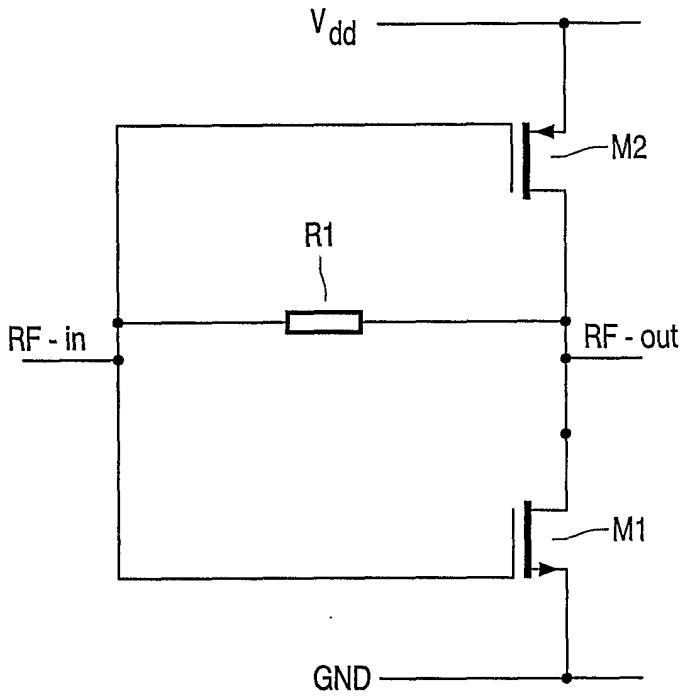


FIG. 5

INTERNATIONAL SEARCH REPORT

PCT/IB 02/05024

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/30 H03F3/193

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H03K H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 313 659 B1 (CRUZ JOSE M ET AL) 6 November 2001 (2001-11-06) column 2, line 41 - line 48 column 6, line 46 -column 8, line 30; figures 5-8	1-6
X	GB 2 351 195 A (ERICSSON TELEFON AB L M) 20 December 2000 (2000-12-20) page 3, line 16 -page 5, line 7; figures 3,11 page 9, line 4 - line 26 page 13, line 7 - line 33	1-4,7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2003	02/04/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Tyberghien, G

INTERNATIONAL SEARCH REPORT

patent family members

PCT/IB 02/05024

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6313659 B1	06-11-2001	NONE	
GB 2351195 A	20-12-2000	AU 4750500 A	02-01-2001
		CN 1369136 T	11-09-2002
		WO 0077931 A1	21-12-2000
		EP 1188238 A1	20-03-2002
		JP 2003502898 T	21-01-2003
		US 2002190784 A1	19-12-2002