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[54] **FOLDING STAGE FOR A FOLDING ANALOG-TO-DIGITAL CONVERTER**

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[51] **Int. Cl.**^{6} **H03M 1/00**

[52] **U.S. Cl.** **341/155**; 341/133

[58] **Field of Search** 341/155, 156, 341/158, 159, 133, 134, 135, 136

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[57] **ABSTRACT**

A folding stage for a folding analog-to-digital converter comprising a plurality of consecutive reference terminals for providing ascending different reference voltages; a first summing node, a second summing node and a first output node. A plurality of differentially coupled transistor pairs with each one of the pairs comprising a first transistor having a main current path and a control electrode which is coupled to an input terminal for receiving an input voltage to be folded and a second transistor having a main current path and a control electrode which is coupled to a respective one of the consecutive reference terminals. The main current path of the first transistor of consecutive transistor pairs is coupled alternately to the first summing node and the second summing node, and the main current path of the associated second transistor is coupled alternately to the second summing node and the first summing node. A dummy structure comprising a first current source, a first dummy transistor having a control electrode coupled to the input terminal, a first main electrode connected to the first current source and a second main electrode coupled to one of the first and second summing nodes, a second current source, and a second dummy transistor having a control electrode coupled to a bias voltage terminal, a first main electrode connected to the second current source and a second main electrode coupled to the other of the first and second summing nodes. The dummy structure reduces capacitive error currents in the differential output current which flows in the summing nodes of the folding stage by providing cancelling currents to the summing nodes.

15 Claims, 4 Drawing Sheets