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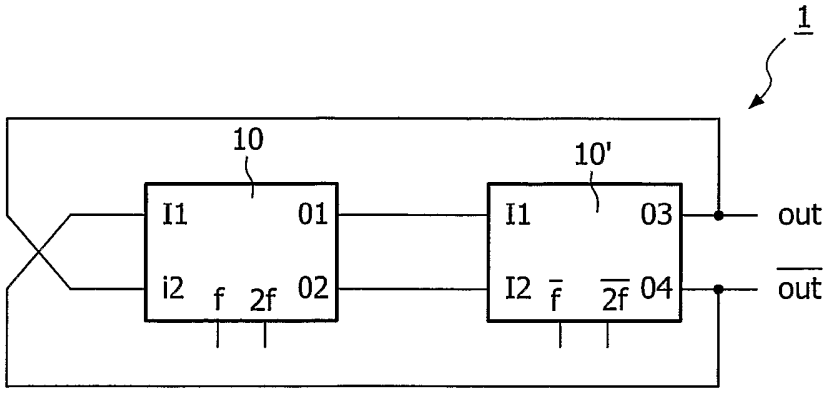
(54) **Title:** FREQUENCY DIVIDER



(57) **Abstract:** A frequency divider comprising, a first latch circuit (10) and a second latch circuit (10'), the second latch circuit (10') being crossed-coupled to the first latch circuit (10). Each latch (10; 10') comprises a respective sense amplifier coupled to a respective latch (11). The sense amplifiers comprise a first clock input for receiving a first clock signal (f, f) and 5 respective complementary first clock signal having a first frequency. The latches (11) comprise a second clock input (2f; 2f) for receiving a second clock signal and respective complementary second clock signal having a second frequency, the second frequency being substantially double the first frequency.

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Frequency divider

The invention refers to a frequency divider.

Frequency dividers are widely used in modern communication devices for dividing a clock signal having a frequency and obtaining another signal having a lower frequency than the frequency of the clock signal. Usually, frequency dividers are implemented using flip-flops or latch circuits. Because clock signals are binary signals i.e. having a HIGH value level and a LOW level, frequency division factors, which are powers of 2 are relatively easier to be implemented.

In modern communication circuits, differential signals are often used and, as a direct consequence frequency dividers adapted to differential signals were necessary.

US-A-6,166,571 describes a frequency divider circuit for producing output signals of half the frequency of an input clock signal, which comprises two identical circuit sections, each producing an output signal and its complement. The circuit sections are connected to each other so that the output signals of one circuit section serve as input signals to the other circuit section. Each circuit section contains a load transistor, which is controlled by one of the clock signal and the clock signal complement, and a switch transistor, which is controlled by the other of the clock signal and the clock signal complement. The circuit exhibits a reduced RC time constant for each circuit section and an increased output signal swing between the output signals and their respective complements. It is observed that the frequency divider comprises two identical sections that are both clocked by the clock signal. The higher the frequency the lower the output signal swing between the output signal and their respective complements. There is therefore a need to have a frequency divider, which is operable at relatively high frequencies and providing relatively large voltage swing.

The invention is defined in the independent claim. The dependent claims defineadvantageous embodiments. The invention provides a frequency divider comprising:

- a first latch circuit and a second latch circuit, the second latch circuit being crossed-coupled to the first latch circuit, each latch comprising a respective sense amplifier coupled to a respective latch,

- the sense amplifiers comprising a first clock input for receiving a first clock signal and respective complementary first clock signal having a first frequency,
- the latches comprising a second clock input for receiving a second clock signal and respective complementary second clock signal having a second frequency, the second frequency being substantially double the first frequency. Throughout the present application it is considered that a complementary signal of a signal is the inverted signal.

During a time interval T/4-T/2 of the first clock signal, since the latch is active the gain of the respective sensing stage increases due to positive feedback applied by the latch. This result in a higher output swing compared to prior-art circuits.

In an embodiment of the invention, the first latch circuit is substantially identical to the second latch circuit. Each sense amplifier may comprise a differential pair of transistors including a first pair of transistors comprising a first transistor coupled to second transistor and a second pair of transistors comprising third transistor coupled to a fourth transistor. Each transistor has a drain, a source and a gate. It should be pointed out here that the invention is not limited to MOS transistors implementation and in a bipolar implementation each transistor has a collector, an emitter and a base corresponding to the drains, source and gate, respectively. A drain of the first transistor and a drain of the third transistor are coupled to a source of the second transistor and to a source of the fourth transistor, respectively. Gates of the second transistor and fourth transistor receive a signal generated by the other latch. Gates of the first transistor and the third transistor are coupled to the first clock input for receiving the first clock signal. It is observed that the role of the sense amplifier is to determine if an input signal is in a HIGH state or in a LOW state and to transmit the signals when the first clock signal is asserted.

In another embodiment of the invention, the latch comprises a pair of cross-coupled transistors, comprising a fifth transistor and a sixth transistor, each transistor having a drain, a gate and a source. The drain of the fifth transistor and the drain of the sixth transistor are coupled to the drain of the second transistor and to the drain of the fourth transistor, respectively. The source of the fifth transistor and the source of the sixth transistor are coupled to the drain of the of seventh transistor and to the drain of an eighth transistor, respectively. A gate of the seventh transistor and a gate of the eighth transistor receive the second clock signal. The crossed coupled transistors implements a negative resistance. The negative resistance is necessary for obtaining the latching property of the circuits and for having the necessary gain in the latches. Usually, the negative resistance is obtained using a crossed coupled pair of transistors.

The above and other features and advantages of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a block level schematic of a frequency divider, according to an embodiment of the invention,

Fig. 2 depicts a transistor level implementation of a sense amplifier, according to an embodiment of the invention,

Fig. 3 depicts a transistor level implementation of a latch, according to an embodiment of the invention,

Fig. 4 depicts a time diagram of a semi-period of the first clock signal, according to an embodiment of the invention, and

Fig. 5 depicts an amplitude versus frequency diagram for the output signals, according to an embodiment of the invention.

Fig. 1 depicts a block level schematic of a frequency divider, according to an embodiment of the invention.

The frequency divider comprises a first latch circuit 10 and a second latch circuit 10', the second latch circuit 10' being crossed-coupled to the first latch circuit 10. The first latch circuit 10 comprises a first input I1 and a first complementary input I2 and a first output O1 and a first complementary output O2.

The second latch 10' comprises a second input I3 and a second complementary input I4 and a second output O3 and a second complementary output O4. The outputs of the first latch 10 are coupled to the corresponding inputs of the second latch 10' i.e. O1 to I3 and O2 to I4. The outputs of the second latch 10' are coupled to the complementary inputs of the first latch 10 i.e. O3 to I2 and O4 to I1 i.e. the first latch 10 and the second latch are crossed-coupled. Each latch circuit comprises a respective sense amplifier coupled to a respective latch (11). The sense amplifiers comprising a first clock input for receiving a first clock signal f; $\overline{f}$ and respective complementary first clock signal having a first frequency. The latches 11 comprise a second clock input 2f; $\overline{2f}$ for receiving a second clock signal and respective complementary second clock signal having a second frequency, the second frequency being substantially double the first frequency.

During a time interval T/4-T/2 of the first clock signal, since the latch is active the gain of the respective sensing stage increases due to positive feedback applied by the latch as shown in Fig. 4. This result in a higher output swing compared to prior-art circuits as shown in Fig. 5. It is remarked that when the circuit uses relatively high frequency signals e.g. in GHz range the shape of the signals are no longer rectangular.

Fig. 2 depicts a transistor level implementation of a sense amplifier, according to an embodiment of the invention. The sense amplifier comprises a differential pair of transistors M1, M3; M2, M4 including a first pair of transistors comprising a first transistor M1 coupled to second transistor M3 and a second pair of transistors comprising third transistor M2 coupled to a fourth transistor M4. Each transistor has a drain, a source and a gate. A drain of the first transistor M1 and a drain of the third transistor M2 are coupled to a source of the second transistor M3 and to a source of the fourth transistor M4 respectively. Gates of the second transistor M3 and fourth transistor M4 receive a signal generated by the other latch. Gates of the first transistor M1 and the third transistor M2 are coupled to the first clock input f for receiving the first clock signal. The drain of the second transistor M3 and the drain of the fourth transistor M4 are coupled to the latch 11. A possible implementation of the latch 11 is shown in Fig. 3.

Fig. 3 depicts a transistor level implementation of a latch, according to an embodiment of the invention. The latch comprises a pair of cross-coupled transistors M5, M6, comprising a fifth transistor M5 and a sixth transistor M6, each transistor having a drain, a gate and a source. A drain of the fifth transistor M5 and a drain of the sixth transistor M6 are coupled to the drain of the second transistor M3 and to the drain of the fourth transistor M4, respectively. A source of the fifth transistor M5 and a source of the sixth transistor M6 are coupled to the drain of the of seventh transistor M7 and to a drain of an eighth transistor M8, respectively. A gate of the seventh transistor M7 and a gate of the eighth transistor M8 receive the second clock signal 2f. The crossed coupled transistors implements a negative resistance. The negative resistance is necessary for obtaining the latching property of the circuits and for having the necessary gain in the latches. Usually, the negative resistance is obtained using a crossed coupled pair of transistors.

It is observed that in the embodiments, only N-MOS transistors are presented. It is understood that a skilled person in the art could apply the teachings of the invention using P-MOS, CMOS, BiCMOS or other type of transistors implemented in a different technology. It is further pointed out here that in a bipolar implementation each transistor has a collector, an emitter and a base corresponding to the drain, source and gate, respectively,

and that the scope of a claim reciting a drain, source or gate is not so limited as to exclude bipolar implementations.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A frequency divider comprising:

- a first latch circuit (10) and a second latch circuit (10'), the second latch circuit (10') being crossed-coupled to the first latch circuit (10), each latch (10; 10') comprising a respective sense amplifier coupled to a respective latch (11),
- the sense amplifiers comprising a first clock input for receiving a first clock signal (f; $\overline{f}$) and respective complementary first clock signal having a first frequency,
- the latches (11) comprising a second clock input (2f; $\overline{2f}$) for receiving a second clock signal and respective complementary second clock signal having a second frequency, the second frequency being substantially double the first frequency.

2. A frequency divider as claimed in claim 5, wherein the first latch circuit(10) is substantially identical to the second latch circuit (10').

3. A frequency divider as claimed in claims 1 or 2, wherein each sense amplifier comprises a differential pair of transistors (M1, M3; M2, M4) including:

- a first pair of transistors comprising a first transistor (M1) coupled to second transistor (M3),
- second pair of transistors comprising third transistor (M2) coupled to a fourth transistor (M4),
- each transistor having a drain, a source and a gate,
- a drain of the first transistor (M1) and a drain of the third transistor (M2)being coupled to a source of the second transistor (M3) and to a source of the fourth transistor (M4), respectively,
- gates of the second transistor (M3) and fourth transistor (M4) receiving a signal generated by the other latch,
- gates of the first transistor (M1) and the third transistor (M2) being coupled to the first clock input (f) for receiving the first clock signal.

4. A frequency divider as claimed in claim any of the preceding claims,wherein the latch (11) comprises:

- a pair of cross-coupled transistors (M5, M6), comprising a fifth transistor (M5) and a sixth transistor (M6), each transistor having a drain, a gate and a source,
- a drain of the fifth transistor (M5) and a drain of the sixth transistor (M6) being coupled to a drain of the of the second transistor (M3) and to a drain of the fourth transistor (M4), respectively,
- a source of the fifth transistor (M5) and a source of the sixth transistor (M6) being coupled to a drain of the of seventh transistor (M7) and to a drain of an eighth transistor (M8), respectively,
- a gate of the seventh transistor (M7) and a gate of the eighth transistor (M8) receiving the second clock signal (2f).

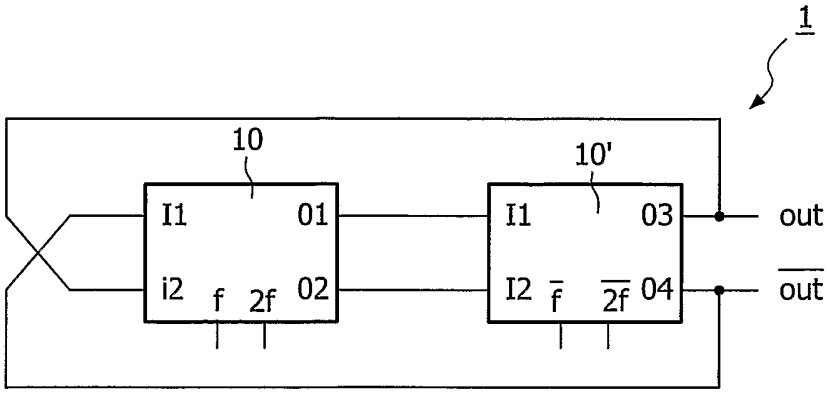

FIG. 1

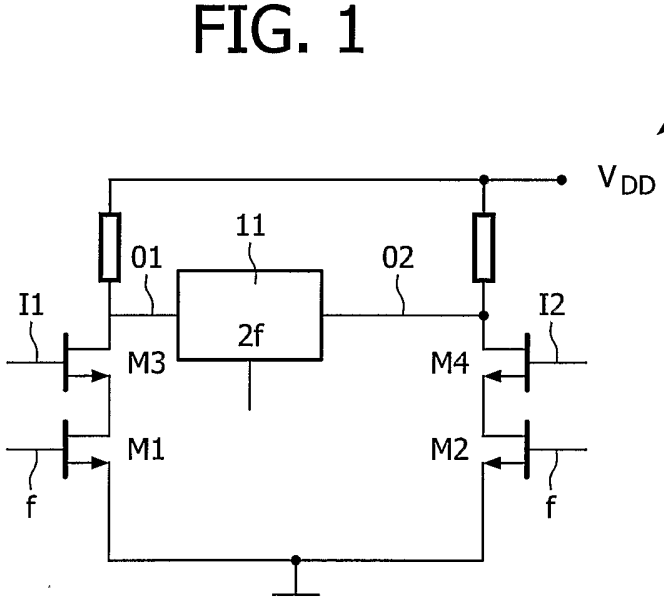

FIG. 2

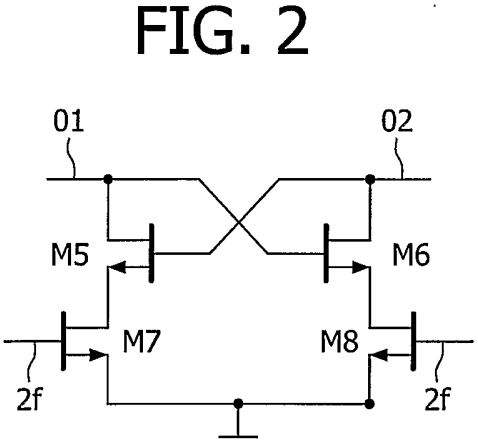

FIG. 3

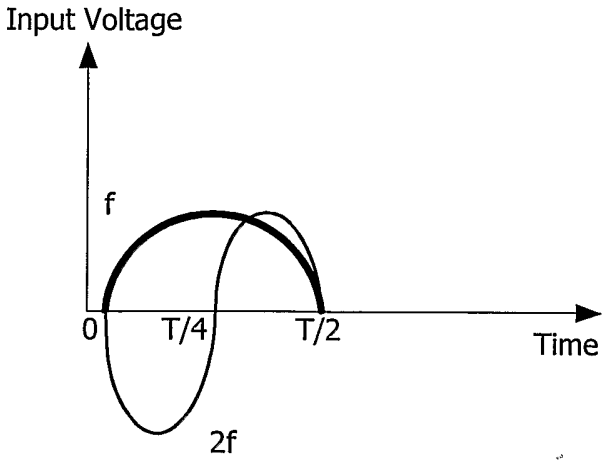
Input Voltage
f
0
T/4
T/2
Time
2f

FIG. 4

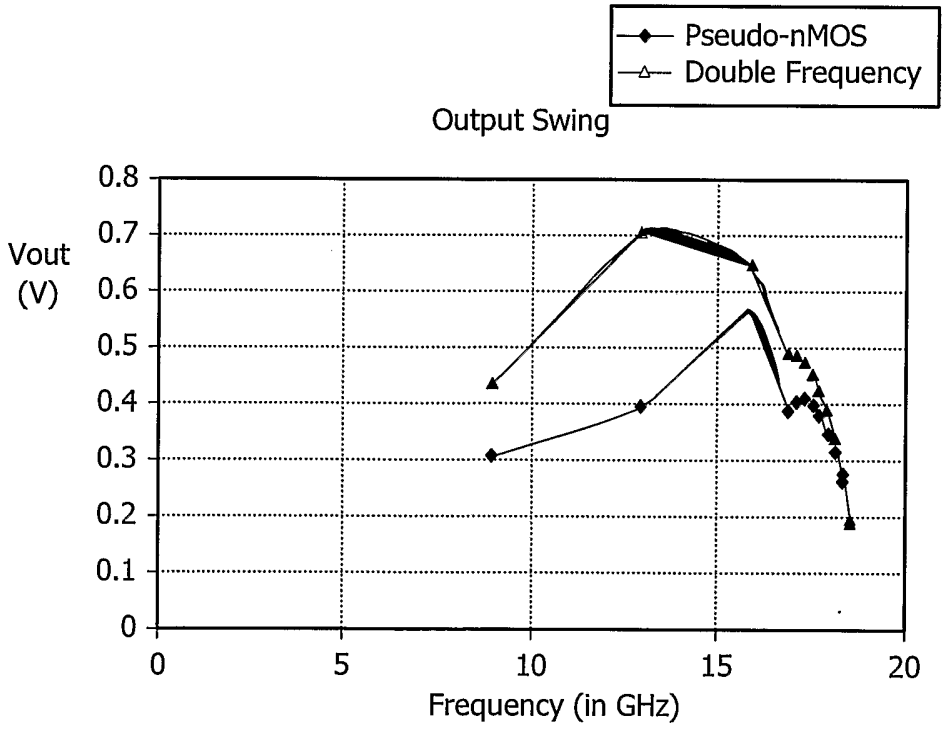
Pseudo-nMOS
Double Frequency
Output Swing
Vout (V)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
5
10
15
20
Frequency (in GHz)

FIG. 5

INTERNATIONAL SEARCH REPORT

ational Application No
/IB2005/052534

A. CLASSIFICATION OF SUBJECT MATTER
H03K23/54 H03K3/356

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 216 295 A (HOANG ET AL) 1 June 1993 (1993-06-01) figures 3a,3b,4,5 column 6, line 13 - column 6, line 57	1-4
A	US 2003/189449 A1 (ZHANG MINGHAO ET AL) 9 October 2003 (2003-10-09) figure 4	
A	NO AUTHOR NAME SUPPLIED IN SOURCE DATA: "Low Power Flip-Flop Circuit" IP.COM JOURNAL, IP.COM INC., WEST HENRIETTA, NY, US, 20 June 2003 (2003-06-20), XP013009421 ISSN: 1533-0001 the whole document	

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 December 2005	28/12/2005

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 004, no. 141 (E-028), 4 October 1980 (1980-10-04) & JP 55 092022 A (NEC CORP), 12 July 1980 (1980-07-12) abstract	
A	US 2004/012416 A1 (CHEUNG SIN-LUEN ET AL) 22 January 2004 (2004-01-22) the whole document	

INTERNATIONAL SEARCH REPORT

Information on patent family members

ıational Application No
'/IB2005/052534

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5216295 A	01-06-1993	NONE	
US 2003189449 A1	09-10-2003	NONE	
JP 55092022 A	12-07-1980	NONE	
US 2004012416 A1	22-01-2004	NONE	