HIGH-VOLTAGE CLASS-D POWER AMPLIFIERS: DESIGN AND OPTIMIZATION

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DISSERTATION

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To My Family

ABSTRACT

Nowadays transducers are ubiquitous as interfaces between the increasingly digital world and the real physical world. The same holds for the power amplifiers driving them. This thesis focuses on the design and optimization of high-voltage class-D amplifiers, which are used for driving capacitive piezoelectric actuator loads in active vibration/noise control applications. The main objective is to further enhance class-D power efficiency compared to existing class-D designs.

To gain insight in class D power efficiency, a detailed analysis of high-voltage class-D dissipation sources is performed and a dissipation model including all the major dissipation sources is developed. The analysis shows that switching loss is a potential dominating dissipation source in high-voltage applications, while its contribution can be minimized by fast switching to eliminate V-I overlap losses. Moreover, it is shown that when varying the class-D switching frequency, a minimum total dissipation exists, with the optimal switching frequency depending on the output power. Furthermore, idle loss reduction by increasing the switching frequency and inserting a dead time to the power stage is backed by the analysis.

Following the analysis, a fast-switching power stage is designed to aim for switching loss minimization. This output stage design features immunity to the on-chip supply bounce, realized by internally regulated floating supplies, variable driving strength for the gate driver, and an efficient 2-step level shifter design. Fast switching transitions and low switching loss are achieved with 94% peak efficiency for the complete class-D power stage in the realized chip. In addition, gate driver sizing procedures for the class-D output stage are discussed, showing that the variable gate driving strength can greatly improve efficiency when on-chip supply bounce is the limiting factor.

Also based on the dissipation analysis, this thesis describes the design of an efficiency-improved high-voltage class-D power amplifier. The amplifier adaptively regulates its

switching frequency for optimal power efficiency across the full output power range. This is based on detecting the switching output node voltage level at the turn-on transition of the power switches. For the final chip prototype, the amplifier achieves 93% efficiency at 45W output power, >80% power efficiency down to 4.5W output power and >49% efficiency down to 0.45W output power.

Finally, for the aim of idle loss reduction, the linearity degradation of dead time insertion and switching frequency increase is discussed in this thesis. To cope with this linearity degradation, both open-loop and closed-loop error correction techniques are explored and it is further shown that a higher-order loop filter combined with uniform sampling once per switching cycle is potentially a suitable choice for closed-loop fixed-carrier class-D implementations.

SAMENVATTING

In moderne elektronica zijn sensoren en actuatoren allom vertegenwoordigd als interface tussen het toenemend digitale domein en de fysieke wereld. Hetzelfde geldt voor de vermogensversterkers om die actuatoren aan te sturen. Dit proefschrift richt zich op het ontwerp en de optimalisatie van klasse D versterkers die gebruikt worden om capacitieve piezoelektrische belastingen aan te sturen in toepassingen op het gebied van trillings- en geluidsreductie. Het voornaamste doel is het vermogensrendement van klasse D versterkers te verbeteren ten opzichte van bestaande ontwerpen.

Om meer inzicht te krijgen in het rendement van klasse D versterkers, is een model gemaakt dat de bijdrages van de verschillende dissipatiemechnismen beschrijft. Deze analyse laat zien dat schakelverliezen potentieel de belangrijkste bijdrage aan de dissipatie kunnen leveren, en dat snel schakelen deze bijdrage kan verminderen door overlap van spanning en stroom in de vermogenstransistoren te voorkomen. Verder blijkt dat als de schakelfrequentie gevariëerd wordt, er een minimum is in de totale dissipatie dat afhangt van het momentane uitgangsvermogen van de versterker. Ook blijkt dat de rustverliezen kunnen worden verminderd door een dode tijd te introduceren en de schakelfrequentie te verhogen.

Deze analyse volgend, is een snel schakelende uitgangstrap ontworpen met het doel de schakelverliezen te beperken. Deze uitgangstrap is ongevoelig voor schakeleffecten op de interne voeding door het gebruik van intern gereguleerde voedingsspanningen, een gate aansturing met variabele sterkte en een efficiënte 2-traps level shifter. Hierdoor worden snelle schakeltransisties bereikt met weinig verliezen waardoor de gerealiseerde chip met de uitgangstrap een vermogensrendement bereikt van 94%. Ook wordt een methode beschreven om de sterkte van de gate aansturing te dimensioneren, waaruit blijkt dat de gate aansturing met variabele sterkte het rendement sterk kan verbeteren als schakeleffecten op de interne voeding de limiterende factor zijn.

Ook gebaseerd op de dissipatie-analyse wordt een klasse D versterker met verbeterd rendement ontworpen en gerealiseerd. De versterker reguleert zijn schakelfrequentie op zo'n manier dat over het gehele vermogensbereik minimale dissipatie wordt bereikt. Deze techniek is gebaseerd op het waarnemen van de spanning op de schakeluitgang op het moment dat de vermogenstransistoren aanschakelen. Een prototype chip is gerealiseerd en bereikt 93% rendement op 45W uitgangsvermogen, > 80% op 4.5W en > 49% op 0.45W.

Tenslotte wordt, met het doel de rustverliezen te beperken, het effect van dode tijd en een hoge schakelfrequentie op de lineariteit van de versterker verkend. Om vermindering van de lineariteit te voorkomen worden open- en gesloten lus foutcorrectie mechanismen verkend. Aangetoond wordt dat een hogere-orde lusfilter in combinatie met uniforme bemonstering van één maal per schakelperiode een geschikte keus is voor klasse D versterkers met een vaste schakelfrequentie.

List of Abbreviations

ESR	Equivalent Series Resistance
HSw	Hard Switching
LED	Light Emitting Diode
NSPWM	Natural Sampling Pulse Width Modulation
PA	Power Amplifier
PD	Pull Down
PU	Pull Up
PWM	Pulse Width Modulation
SSw	Soft Switching
THD	Total Harmonic Distortion
UGB	Unity Gain Bandwidth
UPWM	Uniform Pulse Width Modulation

CONTENTS

CHAPTER ONE

1. Introduction

1.1 Power Amplifiers and Drivers

The continuous evolution of modern electronics and information technology has transformed increasingly more aspects of our daily life into the digital realm. Yet to interface with the real physical world, transducers [1] are ubiquitous, and the same holds for the power amplifiers (PAs) and drivers for driving them. Fig. 1.1 shows just two of many possible examples of such transducer applications, i.e. a loudspeaker and a Light Emitting Diode (LED). Fig. 1.1(a) illustrates the case in which the loudspeaker transforms electrical power into sound. In Fig. 1.1(b), the LED turns electrical power into light. In both cases, power drivers are required to provide the power for the transducers to function.

This thesis will focus on the design and optimization of high-voltage power amplifiers tailored for driving capacitive piezoelectric actuator loads. Fig. 1.2 illustrates such an application scenario where a power amplifier serves as a piezo-actuator driver in an active vibration and noise control system [2], [3], [4]. As shown in Fig. 1.2, first the vibration or noise generated through the panel structure is sensed by a sensor (e.g. an accelerometer). Then through dedicated control systems, the piezoelectric actuator, which is driven by a piezo driver, generates an anti-phase vibration to cancel or attenuate the existing vibration or noise. In these applications, the piezo driver needs to provide tens to hundreds of volts actuation voltage for the piezoelectric actuator. Besides, the signal frequency is in the range of several tens to hundreds of Hz and the piezoelectric actuator can electrically be treated as a capacitive load. With typically several tens of Watt reactive power being processed and the compactness requirement mandating the usage of small or even no heat sinks, the power amplifier for driving the piezo actuators needs to have very high efficiency. This is the main motivation

and the starting point for the research described in this thesis. For the next subsection we will review some classical power amplifier topologies and discuss their corresponding power efficiency.

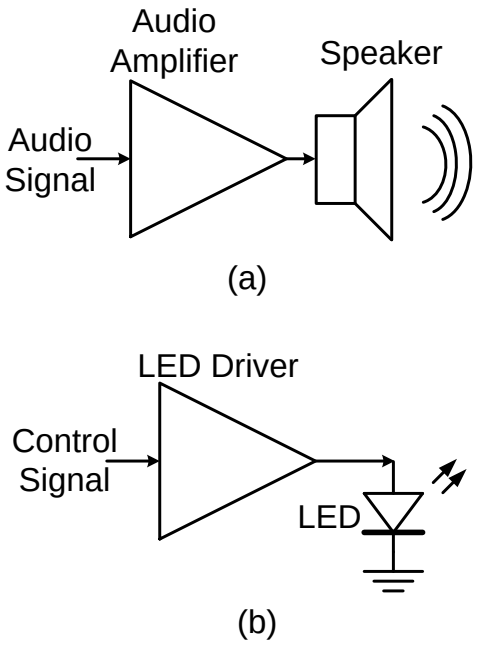


Fig. 1.1. Typical examples of transducers and their corresponding power drivers (a) speakers where electrical power is transformed into sound (b) light emiting diodes where electrical power is transformed into light

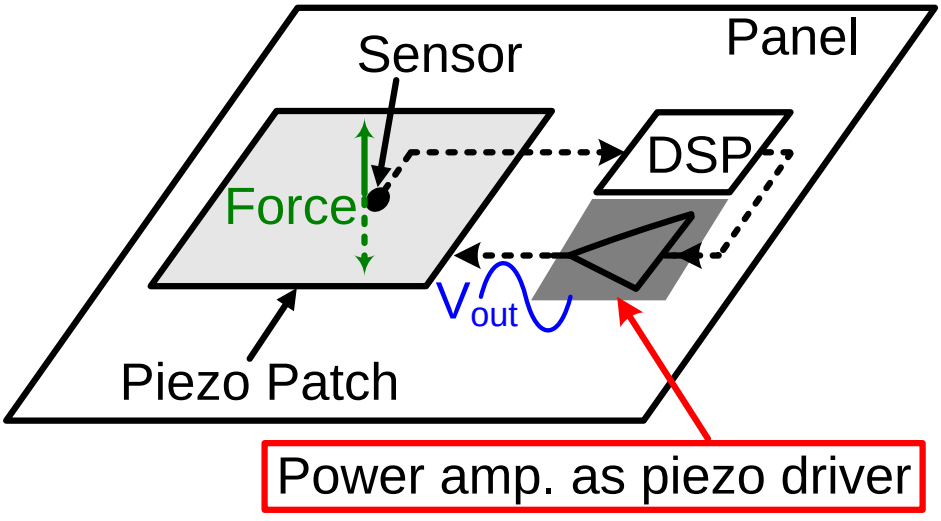


Fig. 1.2. Illustration of an active vibration and noise control system where a PA is adopted as an piezo driver

1.2 Overview of Power Amplifier Types

1.2.1 Linear Class-B Amplifiers

A typical push-pull output stage for class-B amplifiers [5] is shown in Fig. 1.3. The two output power transistors conduct alternately to avoid quiescent current draw from the power supplies. However, during their respective conducting phase, the output transistors have continuous V-I overlap loss, as shown in Fig. 1.4, where V_{Mn} represents the voltage across M_n during the phase that it is conducting. Consequently class-B amplifiers can only have a theoretical maximum power efficiency of 78.6% [5] for a full swing sinusoidal output voltage. For lower output powers and signals with a larger peak-to-average ratio than sinewaves, efficiency is easily an order of magnitude lower [6].

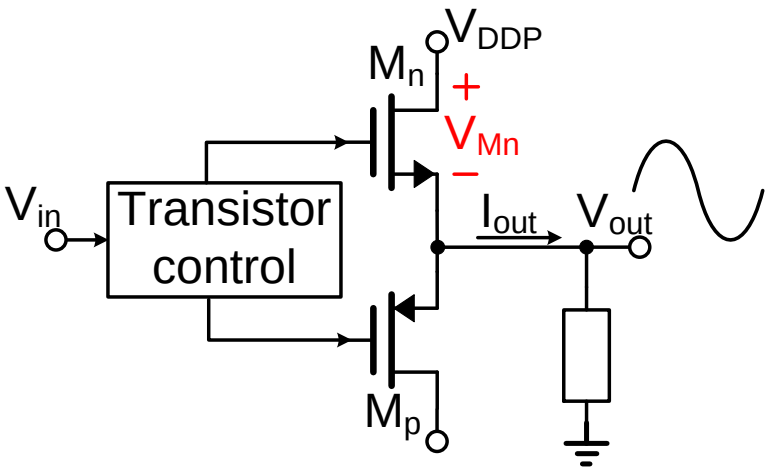


Fig. 1.3. Basic push-pull output stage for a class-B amplifier

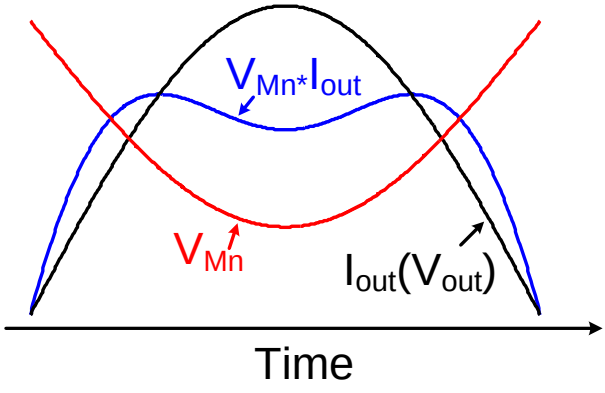


Fig. 1.4. Illustration of continuous V-I overlap loss on a class-B output transistor

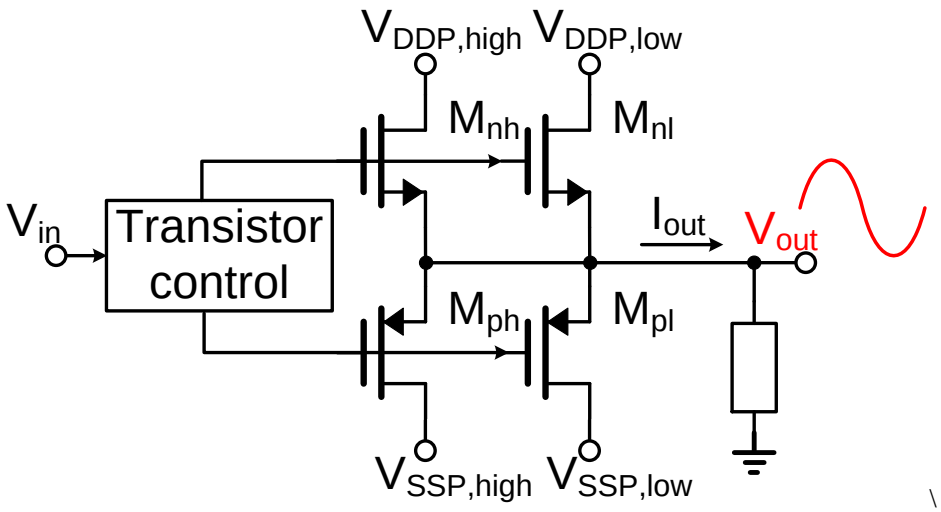


Fig. 1.5. Illustration of a class-G output stage, with two separate supply voltage sets

An improvement to the basic class-B output stage can be made by adding multiple supplies to the power stage, i.e. a class-G amplifier [7]. For the class-G topology, the amplifier switches between low- and high-voltage supplies based on the instantaneous signal amplitude. This way the V-I overlap loss can be significantly reduced, especially for low signal levels, and the efficiency is improved compared to class-B designs. Yet the continuous conduction nature of the output stage is not changed and the theoretical maximum efficiency is still limited.

1.2.2 Switching Class-D Amplifiers

In comparison to linear amplifiers, class-D switching amplifiers (Fig. 1.6) can offer a much higher maximum power efficiency [8]- [23]. Their superior efficiency can be attributed to the switching nature of the output stage, where the continuous V-I overlap loss in the output transistors is eliminated. Fig. 1.6 shows the working principle of a class-D amplifier. An input voltage signal is converted into two control signals for controlling the output switches. The switching output node V_{pwm} is pulse-width modulated (PWM) with its duty cycle proportional to the input voltage. The output low-pass filter then filters out the high-frequency content of the V_{pwm} signal and the final V_{out} is an amplified version of the low-frequency V_{in}.

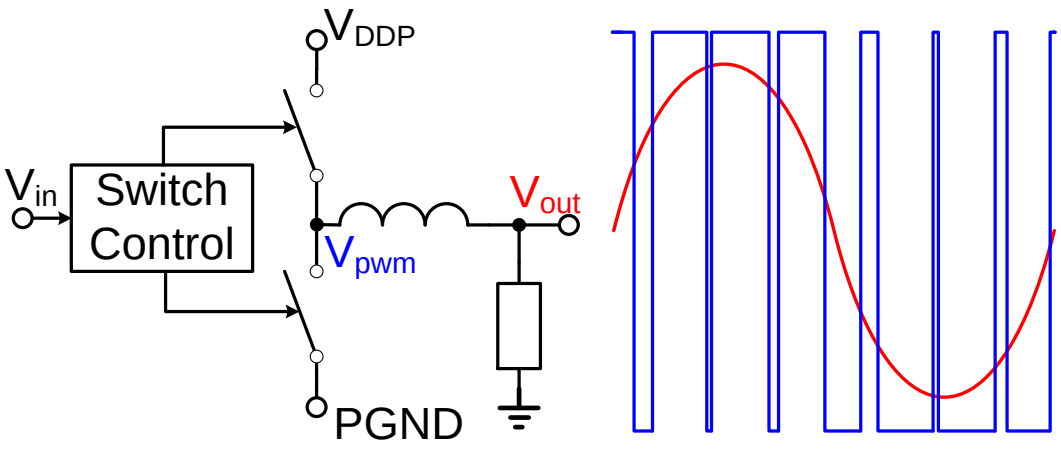


Fig. 1.6. Working principal of a class-D amplifier

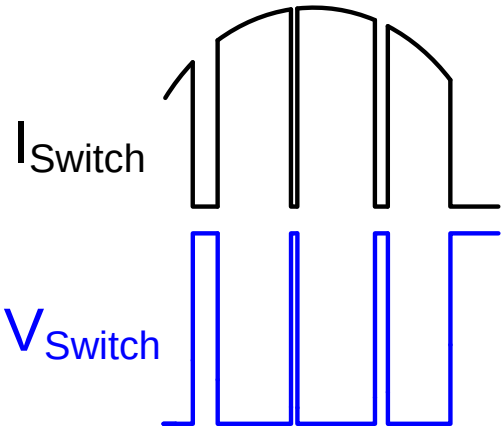


Fig. 1.7. Illustration of voltage and current waveforms in the output switches

Assuming that the output switches are ideal and the switching transitions are infinitely fast, no simultaneous voltage drop and current conduction will occur in the switches. This is shown in Fig. 1.7, where I_{switch} denotes the current flowing through the switch and V_{switch} is the voltage across the switch. Thus ideally class-D output stages have no dissipation and their power efficiency is 100%. For this reason, class-D amplifiers have gained popularity and are widely adopted for audio power amplification, both for high-power [8]- [14] and low-power [15]-[23] applications.

1.2.3 Combination of Linear and Switching Amplifiers

In literature the combination of linear and switching techniques has also been explored, with either series- [24] or parallel-connected [25] linear/switching topologies. The advantage of such techniques is that the switching-induced output voltage ripple can to a large extend be eliminated. Also, the bandwidth of the amplifier can be improved. All of these are achieved without resorting to a power-consuming high switching frequency of the class-D amplifier, because the linear amplifier assists the improvements. For this reason, parallel-connected linear and switching amplifiers can be adopted in many high signal bandwidth applications where low output voltage ripple is also required [26]-[28], with better efficiency compared to the use of only switching techniques. Yet for audio-frequency applications, the addition of an extra linear or switching amplifier is not so attractive from a power efficiency point of view, since a low switching frequency is already adequate for the low signal bandwidth. The extra linear amplifier will only add extra power consumption.

1.2.4 Discussion

Considering the efficiency performance of various types of linear and switching power amplifiers, this thesis will focus on the design and optimization of high-voltage class-D amplifiers, since they can offer the highest power efficiency in the kHz signal frequency range. This is especially motivated by the application discussed in this thesis. The piezoelectric load is capacitive in the signal frequency and mainly reactive output power is being processed with hardly any real power delivered to the load. Consequently the efficiency of the piezo driver [29]-[33] should be maximized. An overview of state of the art class-D designs will be given in the next subsection.

1.3 Design Aspects of Class-D Amplifiers

Power efficiency and linearity are two major performance criteria used for class-D designs [8]- [23] and will be discussed next. Besides these two performance criteria, other features like incorporating the output filter in the feedback network, electro-magnetic interference minimization and robustness are also important for a class-D design and will also be discussed.

1.3.1 Power Efficiency

Various dissipation sources lead class-D PA efficiency away from the ideal 100% and typical peak power efficiency is around 90%. The dissipation sources have been summarized and modeled with various level of accuracy [34]-[38]. In [34], conduction loss due to the output power switch on resistance and switching loss resulting from V-I overlap during switching are considered to be the main loss mechanisms. It is also shown that proper sizing of the power switch W/L ratio can optimize the total dissipation. Yet the modeling of the switching loss in [34] is rather simplified. Detailed modeling of the switching loss can be found in [35]-[38]. The distinction between lossless and lossy switching transitions is important, as the optimization procedure can be rather different with contributing dissipation sources varying.

Passive component losses can also contribute significantly to the total loss of the class-D output stage. These include the losses from both the output power inductors and the filtering capacitors [39]-[42]. Regarding the loss mechanisms, there exists conduction loss due to the equivalent series resistance (ESR) of these passive components. Moreover, hysteretic core loss of the output power inductors is also an important contributor [41],[42]. This loss mechanism can be attributed to the unrecoverable part of the energy required for the changing magnetization of the core material.

Moreover, efficiency optimization should also be done for low output powers and for signals with high peak-to-average ratio. Light load efficiency improvement can be realized by identifying the dominating dissipation source for light load condition and find methods to minimize it [22], [43]-[46]. In this respect, adaptive techniques are usually being used. In [22] changing the power transistor size according to output power level is used while in [44] and [46] switching frequency is adaptively changed.

1.3.2 Linearity

Class-D power stage non-idealities introduce distortion to the amplifier's output signal [47],[48]. Feedback loop gain can suppress these error and various high-order feedback loops with sufficient loop gain are implemented for this reason [49]-[51]. Yet it has been shown that higher-order loop filters does not necessarily mean better linearity performance due to the extra error introduced by the PWM-based feedback loop itself [52]-[54]. This error is

related to the PWM residual ripple voltage not being completely attenuated by the loop filter. For getting minimum aliasing error, in [52] a minimum aliasing error loop filter is adopted to suppress the ripple-induced error. In [55] sampling after the loop filter is used to significantly reduce this ripple voltage.

1.3.3 Full Output Filter Control

Conventional class-D feedback networks are connected to the switching output node of the power stage instead of the actual output node of the amplifier [8]-[23]. This is considering the two additional poles introduced by the second-order low-pass filter between the switching output node and the actual output. To get high loop gain for error suppression, low frequency poles, which is at frequencies much lower than the poles' frequency of the second-order low-pass filter, have to be introduced to the feedback loops. Thus additional zeros should be introduced for frequency compensation when the output filter is included in the feedback loop. This has been done for both self-oscillating [56],[57] and fixed-carrier [58],[59] class-D topologies, by properly compensating the phase lag resulting from the output filter. The most significant advantage of incorporating the output filter in the feedback loop is that the non-linearity of the power inductor is no longer important, since its error can also be corrected. Low-cost and compact size power inductors are then feasible for the output filter [59].

1.3.4 Electro-Magnetic Interference (EMI) Issues

Compared to linear amplifiers, the switching nature of class-D amplifiers causes them to have potential EMI issues, because of the high frequency harmonics generated through the switching actions. From a system design point of view [60], proper shielding and grounding of the amplifier is necessary. Besides, the PCB design should avoid long traces and loops interfacing with external and on-chip components. From a circuit design point of view, proper switching sequences [61] as well as slow switching transitions [62],[63] can help reducing EMI. Moreover, similar to switched-mode power supply designs [64]-[68], spread spectrum techniques can be applied to class-D designs for EMI reduction [69].

1.3.5 Protection Circuitry

Robustness is another important requirement for power amplifiers and thus various protection circuits for the power stage are required. These include over current protection, over temperature protection etc. Especially for high-voltage designs, the over current protection circuit design is not straightforward since the switching output node has a voltage swing higher than any maximum gate source voltage allowable. Proper isolation and accurate over current detection circuits can be found in [9] and [70]. In addition, for speaker protection in audio applications, accurately sensing the load current in the switching output stage is also challenging and has been addressed in [19] and [23].

1.4 Motivation and Thesis Outline

1.4.1 Motivation – Power Effieincy

As discussed previously, class-D PAs can offer the highest power efficiency in the kHz signal frequency range among the various PA types. Yet how to achieve this high efficiency and whether further optimization is possible is rarely being addressed in a systematic way in literature [8]-[23]. In this thesis the main research motivations/questions are listed as follows,

1) What are the main dissipation sources in an integrated high voltage class-D amplifier?

2) How can we further improve its efficiency performance?

3) In circuit design how can we implement these improvements?

1.4.2 Thesis Outline

The remainder of the thesis is organized as follows:

With efficiency improvement being the primary motivation for this work, chapter 2 starts with a detailed analysis on class-D dissipation sources. A dissipation model is established that can accurately predict the class-D dissipation across different load conditions as well as different switching scenarios. This dissipation analysis serves as the guideline for the following chapters, with three feasible power efficiency optimization methods given for further exploration in the following chapters. The three optimization directions aim for

minimizing the switching loss, extending the high-efficiency output power range as well as improving efficiency at idle/low output power, respectively.

Chapter 3 focuses on minimizing switching loss in an integrated high-voltage class-D power stage realization. It is shown that fast switching is required to minimize the switching loss associated with V-I overlap. But with parasitic inductances between the on-chip power stage and the external power supplies present, fast switching causes large di/dt and in turn significant on-chip supply bounce. On-chip floating supply regulators and in-cycle variable gate driver strength are introduced to minimize the influence of on-chip supply bounce and realize fast switching transitions. In addition, the design of robust level shifter circuits for logic signal communication between different supply domains are also discussed in this chapter.

Chapter 4 presents an optimal-efficiency-tracking switching frequency regulation technique for extending the high-efficiency output power range. It is analyzed here that the inductor ripple loss is the dominant dissipation source at low output power levels, as long as the switching transitions on the switching output node is lossless soft switching. A regulation loop is designed that can always ensure that switching transitions are at the boundary between lossless soft switching and hard switching, thus simultaneously minimizing switching loss and inductor ripple loss. The realized amplifier can maintain high efficiency over orders of magnitude output power variation.

Chapter 5 discusses methods for further improving efficiency at idle/low output power. This is by inserting dead time in the output stage as well as operating the power stage with higher switching frequency. However, this will make the linearity performance worse. Methods for optimizing the linearity are discussed, both for open-loop and closed-loop situations.

Finally chapter 6 gives conclusions and recommendations for future work.

CHAPTER TWO

2. Class-D Dissipation: Modeling and Optimization

(Section 2.2 to section 2.3 are taken from part of the author's paper accepted to IEEE Journal of Solid-State Circuits in 2015 [88].)

2.1 Introduction

This chapter will focus on analyzing and developing a dissipation model for high-voltage class-D power stages. The main purpose for developing such a model is to identify the dominating dissipation sources in class-D power stages with high supply voltage (in the range of 100V). Subsequently with all the dominating dissipation mechanisms identified, various methods for improving the power stage efficiency can be developed. These efficiency improvement methods will serve as design guidelines for the following chapters in this thesis.

In literature, switching power stage dissipation has been modeled with various levels of accuracy [34]-[38]. However, with the switching stage operating conditions (switching frequency, supply voltage) varying by orders of magnitude over operating conditions, the dominating dissipation sources are different for each case. No dissipation models clarifying the dominating loss mechanisms of a high-voltage class-D power stage are available, especially when considering that dominating dissipation sources can vary for different output power levels. For this reason, it is necessary to develop a comprehensive model with all the dissipation sources that can contribute significantly to the high-voltage case included. Subsequently, with the developed model it can be clearly seen what the dominating dissipation sources are and how they can be optimized.

This chapter is organized as follows: section 2.2 shows all the contributing dissipation sources for a class-D power stage. With the switching loss being an important dissipation source, section 2.3 analyzed this loss mechanism in detail. The developed dissipation model is verified against transistor-level simulation results in section 2.4. Finally, section 2.5 draws conclusions and discusses efficiency improvements that are investigated in the subsequent chapters.

2.2 Class-D Power Stage Dissipation Sources

For class-D dissipation analysis, a basic class-D power stage topology is shown in Fig. 2.1. Two N-type DMOSFETs are used as power switches (Fig. 2.2) and their on/off state is controlled by two gate driver circuits. Typically the maximum V_{ds} of the DMOSFETs is much higher than their V_{gs}, therefore the gate driver supply V_{DD} is much lower than the output stage supply V_{DDP}. The current I_L flowing through the power inductor L_{out} can be divided into two parts: the average load current within one switching cycle with value I_{out} and the inductor ripple current with amplitude I_{rip} expressed as [71]:

$$I_{rip}=\frac{V_{DDP}D(1-D)}{2f_{sw}L_{out}} \tag{2.1}$$

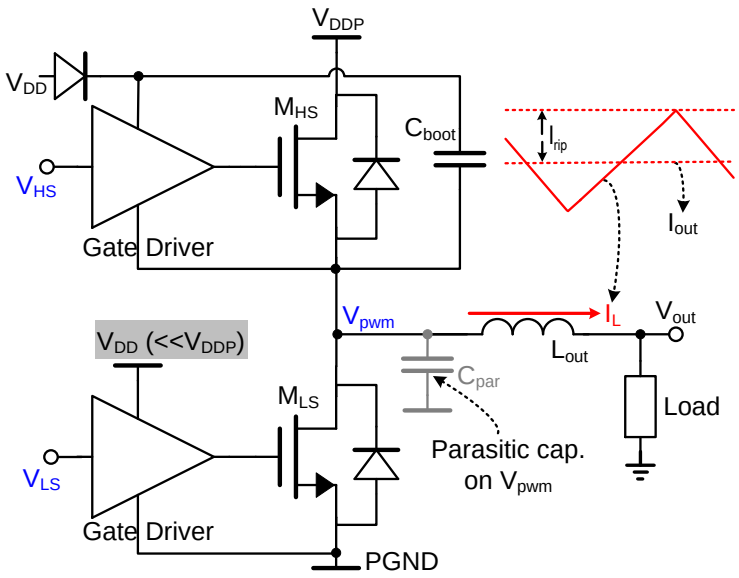


Fig. 2.1. Basic topology of a high-voltage class-D power stage

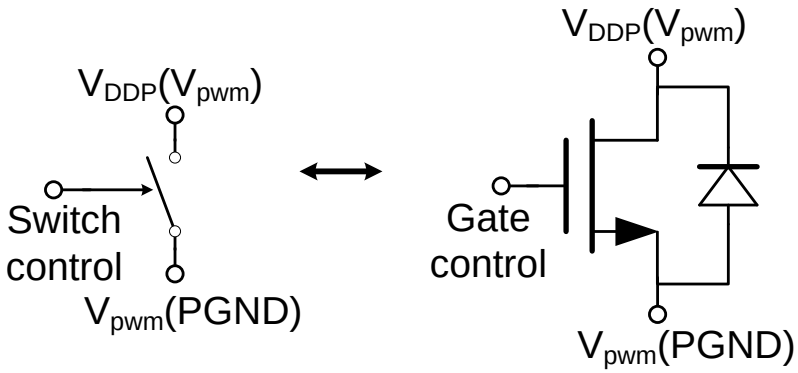


Fig. 2.2. N-type DMOS FET devices as both high-side and low-side power switches for high-voltage class-D amplifier implementation.

where f_{sw} is the class-D switching frequency and D is the V_{pwm} duty cycle. As we can see from (2.1), I_{rip} is influenced by numerous circuit operating parameters. This makes the ratio between I_{out} and I_{rip} also dependent on these parameters. Yet the I_{out}-I_{rip} ratio is important for identifying the different dissipation contributions at changing output power levels, as will be discussed in the following.

The main dissipation sources in a class-D power stage are listed in TABLE I. Among them, conduction loss P_{con} is due to I_{out} flowing through the on resistance of the power transistors (r_{on}) and the equivalent series resistance of L_{out} (r_{esr}),

$$P_{con}=I_{out}^2(r_{on}+r_{esr}) \tag{2.2}$$

Ripple loss P_{Irip} is caused by the I_{rip} conduction in r_{on} and r_{esr}, as well as the magnetic core loss in L_{out}. Assuming I_{out} is constant during one switching cycle with the triangle I_{rip} superimposed on it, the conduction loss contribution of I_{rip} can be expressed as,

$$P_{Irip,cond}=\frac{1}{3}I_{rip}^2(r_{on}+r_{esr}) \tag{2.3}$$

There is also magnetic core loss, related to the hysteresis of the B-H loop of the inductor core material. This loss is the unrecoverable part of the energy required for the changing magnetization of the core material and is expressed as [41],

$$P_{Irip,core}=K(Vol)(f_{sw})^x(\Delta B)^y \tag{2.4}$$

where K is a constant for core material, Vol is the core volume, x is the power factor for switching frequency f_{sw} and y is a power factor for the changing magnetic flux density with amplitude ΔB. The changing magnetic field ΔH, which varies together with ΔB following the B-H curve, is directly proportional to $I_{rip.}$ Thus by adopting x=1 and y=2 as a simplified power factor [72], (2.4) can be rewritten using I_{rip} as.

$$P_{Irip,core}=\frac{1}{3}I_{rip}^2 r_{eq} \tag{2.5}$$

with $r_{eq}= 3K(Vol)f_{sw}$ being the equivalent resistance for the core loss contribution. Further combining the I_{rip}-induced conduction loss (2.3) and magnetic core loss (2.5),

$$P_{Irip}=\frac{1}{3}I_{rip}^2(r_{on}+r_{esr}+r_{eq}) \tag{2.6}$$

Gate driver loss P_g results from charging/discharging the gate capacitance of M_{HS}/M_{LS} when turning M_{HS}/M_{LS} on/off, P_g for M_{HS} and M_{LS} combined can be expressed as:,

$$P_g=Q_g V_{DD} f_{sw} \tag{2.7}$$

where $Q_g=\int_{PGND}^{V_{DD}} C_g(V)dV$ with C_g the total gate capacitance of M_{HS} and M_{LS}. Total gate charge instead of the gate capacitance is adopted here for easier and more precise power loss calculation because the parasitic capacitances of a power MOSFET show large variations over different bias conditions [36].

TABLE I. LIST OF MAIN DISSIPATION SOURCES IN A CLASS-D POWER STAGE

Dissipation Type	Source	Analytical Expression
Conduction loss P_{con}	I_{out} conduction	(2.2)
Ripple loss P_{Irip}	I_{rip} conduction	(2.6)
Gate driver loss P_g	Charging/discharging the gate capacitance of M_{HS}/M_{LS}	(2.7)
Capacitive loss P_{cap}	Charging/discharging C_{par} on V_{pwm} by M_{HS}/M_{LS}	(2.13)
Switching loss P_{sw}	During hard switching, V-(I_L+I_{rr}) overlap dissipated in the power switches	

Both the capacitive loss P_{cap} and the switching loss P_{sw} are induced by the switching at the pulse-width-modulated (PWM) output node V_{pwm}. With a high-voltage V_{DDP}, $P_{sw}+P_{cap}$ can be significant. Yet whether these two dissipation sources exist, depends on the V_{pwm} switching

waveforms and consequently on the I_{out}-I_{rip} amplitude, as will be discussed in detail in the following.

2.3 V_{pwm}-Switching-Induced Power Loss Analysis

Depending on the inductor current direction and amplitude at the moment of switching, three V_{pwm} switching types can be identified as follows (using V_{pwm} low-to-high transitions for illustration):

1) Hard switching (HSw). As shown in Fig. 2.3, the inductor current I_L is flowing out of the power stage as M_{Ls} is turned off at t_0. During the dead time t_d, when both power transistors are kept off, I_L has nowhere to go but through the body diode of M_{LS}. As a result V_{pwm} will stay near the PGND level. This remains until M_{HS} is turned on at t_1 when the dead time t_d is finished. The switching transition begins when the current I_{HS} in M_{HS} is large enough to provide the current for charging C_{par} (I_{cap}), the reverse-recovery current [11] of the body-diode of M_{LS} (I_{rr}), and the inductor current I_L, as illustrated in Fig. 2.4. Among these three types of current that contribute to M_{HS} dissipation, the I_{cap} contribution can be expressed as:

$$P_{cap,HSw}=\frac{1}{2}Q_o V_{DDP} f_{sw} \tag{2.8}$$

where $Q_o=\int_{PGND}^{V_{DDP}} C_{par}(V)dV$ when M_{HS} is on while M_{LS} is off. The Q_o expression is also for more precise calculation of P_{cap} considering the nonlinear C_{par}.

As for the contribution of I_{rr} and I_L, the transition time from t_1 to t_2 is determined by the gate driver pull-up strength [29] [35] and thus the V-I overlap part contributed by I_L will be dependent on the gate driver design. To simplify the modeling of P_{sw}, we assume that the gate driver pull-up strength is large enough to make the transition very fast and to satisfy $I_L*(t_2-t_1) << Q_{rr}$ (the reverse recovery charge). Then we get

$$P_{sw,HSw}=\frac{1}{2}Q_{rr} V_{DDP} f_{sw} \tag{2.9}$$

$P_{cap,HSw}+P_{sw,HSw}$ then will be the total M_{HS} dissipation during the hard switching transition.

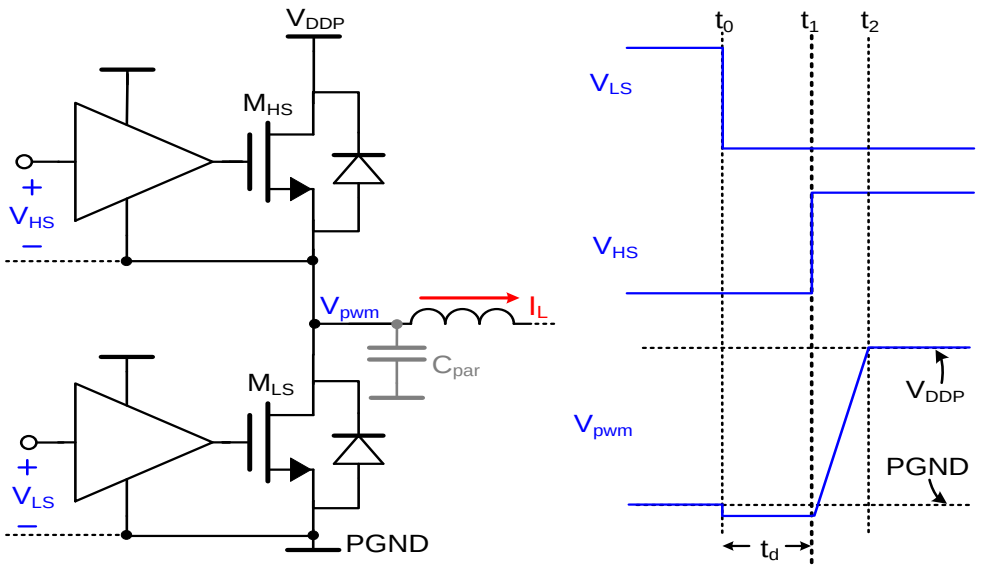


Fig. 2.3. Illustration of a V_{pwm} hard switching transition, where M_{HS} has to complete the transition with V-I overlap. In this case switching-induced loss results in M_{HS}.

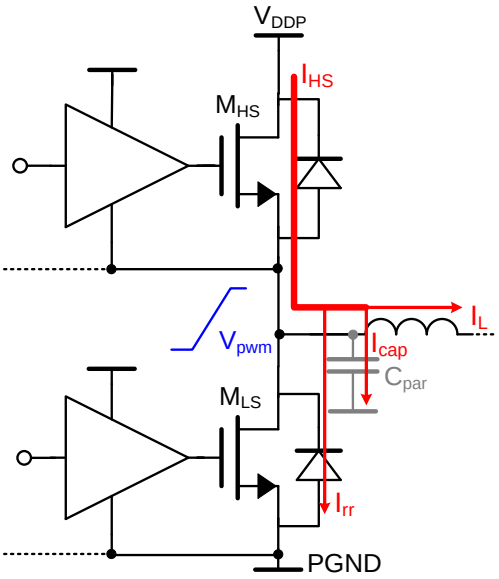


Fig. 2.4. Active power switches (M_{HS} in this example) has to provide current for a hard switching transition, resulting in V_{pwm} switching-induced loss.

2) Soft switching (SSw). The switching dynamic changes when the inductor current I_L is flowing into the power stage at the transition time, as shown in Fig. 2.5. In this case when M_{LS} is turned off at t_o, I_L will immediately begin to charge C_{par} and V_{pwm} begins to rise. If the value of I_L is large enough to satisfy

$$I_L * t_d \geq Q_o' \qquad (2.10)$$

where $Q_o' = \int_{PGND}^{V_{DDP}} C_{par}(V)dV$ when both M_{HS} and M_{LS} are off, the switching transition will finish within the dead time at t_1 before M_{HS} is turned on at t_2. No V-I overlap in the active devices exists in this lossless soft switching transition (Fig. 2.6) and thus $P_{sw,SSw}+P_{cap,SSw}=0$.

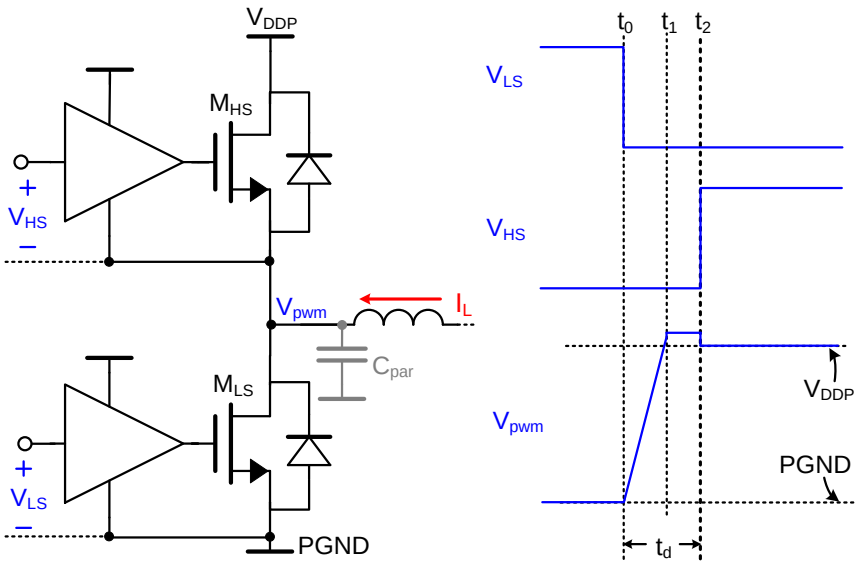


Fig. 2.5. Illustration of a V_{pwm} lossless soft switching transition, where the inductor current can fully charge V_{pwm} to V_{DDP} without resorting to the active devices M_{HS}/M_{LS}.

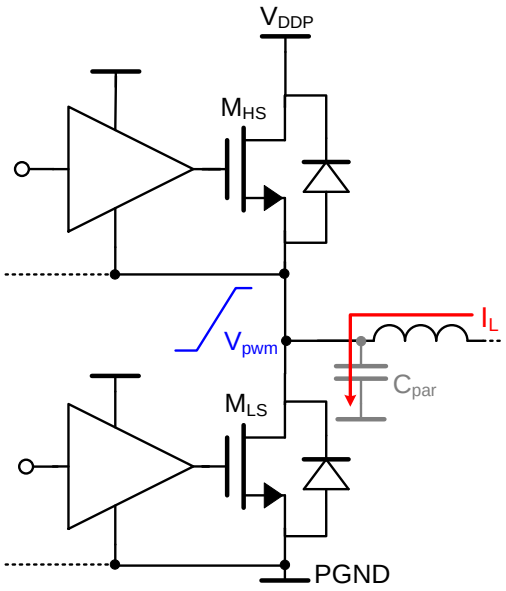


Fig. 2.6. The inductor current itself can accomplish the switching transition in lossless soft switching, without resorting to the active power switches.

3) Partial soft switching (PSSw). Same as in the case of lossless soft switching, I_L is flowing into the power stage at the transition time, as shown in Fig. 2.7. When M_{LS} turns off, I_L also immediately begins to charge C_{par}, thus $P_{sw,PSSw}=0$. However, if the value of I_L is too low to satisfy (2.10), C_{par} cannot be charged to V_{DDP} within the dead time. M_{HS} is turned on to finish the rest of the transition with $P_{cap,PSSw}$ loss expressed as:

$$P_{cap,PSSw}=\frac{1}{2}F^2Q_oV_{DDP}f_{sw} \tag{2.11}$$

where F represents the ratio of the remaining V_{pwm} transition that has to be finished by the active power switches and is approximated here as:

$$F=(Q_o^{'}-I_Lt_d)/Q_o^{'} \tag{2.12}$$

To summarize the combined $P_{sw}+P_{cap}$ for the above three switching transition scenarios, we define the inductor current in the direction of flowing out of the power stage to be positive, then

$$P_{sw}+P_{cap}=\begin{cases}\frac{1}{2}(Q_{rr}+Q_o)V_{DDP}f_{sw} & \text{if } I_{out}-I_{rip}>0\\ 0 & \text{if } I_{out}-I_{rip}\le 0 \text{ and } \left|I_{out}-I_{rip}\right|*t_d\ge Q_o^{'}\\ \frac{1}{2}F^2Q_oV_{DDP}f_{sw} & \text{if } I_{out}-I_{rip}\le 0 \text{ and } \left|I_{out}-I_{rip}\right|*t_d<Q_o^{'}\end{cases} \tag{2.13}$$

As for the V_{pwm} high-to-low transition, I_L now equals $I_{out}+I_{rip}$, which will be always flowing out of the power stage for positive I_{out}. This is a lossless soft switching transition when $(I_{out}+I_{rip})*t_d\ge Q_o^{'}$ is satisfied, which is typically the case.

Considering the complete switching cycle with a positive I_{out} as shown in Fig. 2.8, a higher I_{rip} amplitude than I_{out} results in bidirectional I_L and consequently both switching transitions are soft switching (Fig. 2.8(a)), with partial soft switching for the low-to-high transition still possible. On the other hand, a lower I_{rip} amplitude than I_{out} results in unidirectional I_L, which means the low-to-high transition is hard switching (Fig. 2.8(b)).

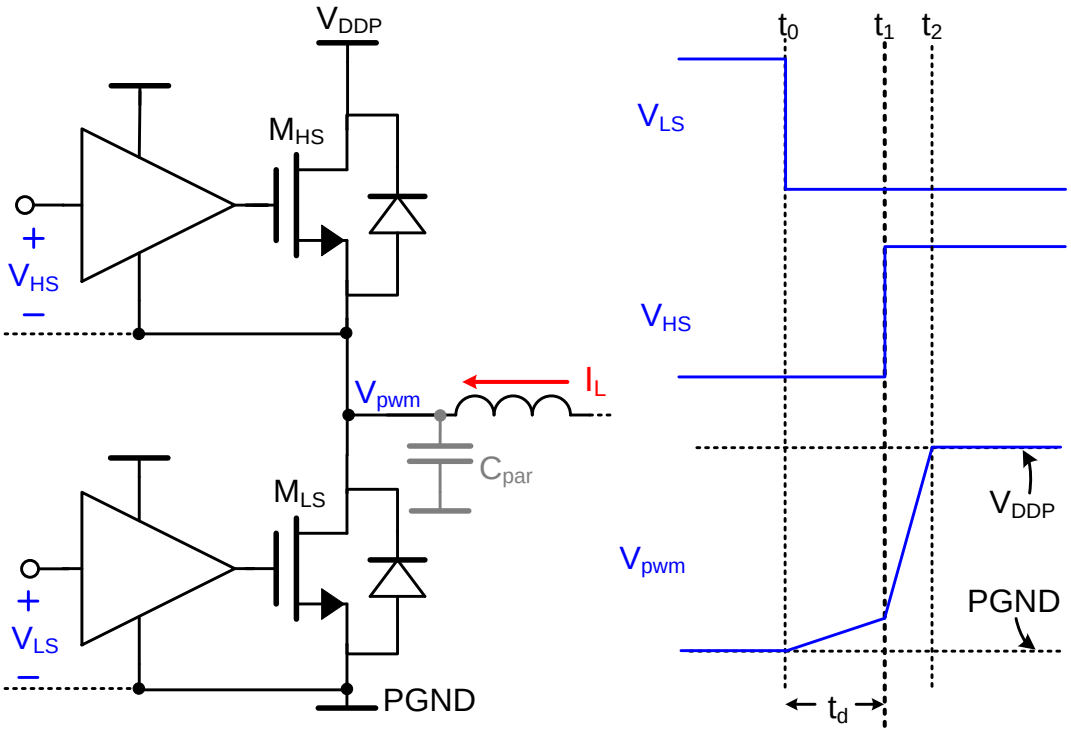


Fig. 2.7. Illustration of a V_{pwm} transition partially completed by M_{HS}, resulting in P_{cap}. In this case the inductor current amplitude is not large enough to fully charge V_{pwm} to V_{DDP} within the dead time.

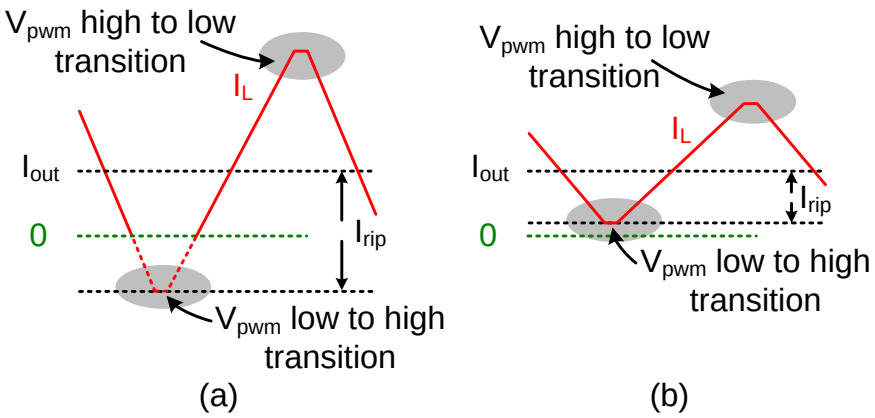


Fig. 2.8. Depending on the relative amplitude of I_{rip} and I_{out}, it can be that both V_{pwm} switching transitions are soft switching or one of the transitions is hard switching. (a) Bidirectional inductor current result in V_{pwm} low to high transition being soft switching. (b) Unidirectional inductor current flowing out of the power stage result in V_{pwm} low to high transition being hard switching

TABLE II. SUMMARY OF THE PARAMETERS USED IN SIMULATION

Parameters	Value
Power Stage Supply V_{DDP}	80V
Gate Driver Supply V_{DD}	3.3V
Output Inductance L_{out}	100µH
V_{pwm} Duty Cycle	0.5
Dead Time t_d	100ns
DMOSFET's size	56000µm/0.75µm

TABLE III. PARAMETERS ASSOCIATED WITH THE POWER DMOSFETS FOR DISSIPATION CALCULATION

Parameters	Values (DMOSFET W/L=56000µm/0.75µm)	Remarks
On resistance r_{on}	560mΩ	On resistance of the DMOSFETs
Gate Charge Q_g	15nC	$2*\int_{PGND}^{V_{DD}} C_g(V)dV$
$Q_o^{'}$	8.5nC	$\int_{PGND}^{V_{DDP}} C_{par}(V)dV$ (Both M_{HS} and M_{LS} are off)
Q_o	28nC	$\int_{PGND}^{V_{DDP}} C_{par}(V)dV$ (M_{HS} is on)
Q_{rr}	$[(I_{out}-I_{rip})/100mA]\cdot 1.5nC$	Reverse recovery charge ($I_{out}>I_{rip}$)

2.4 Verification of Loss Analysis

With analytical expressions for each of the dissipation sources listed in TABLE I as in (2.2), (2.6), (2.7) and (2.13), a comparison can be made between transistor-level power dissipation simulation and the analytical model. For the verification, we only consider the power loss of the transistors, i.e. r_{esr} and r_{eq} of the power inductor will not be considered yet. TABLE II shows a summary of the power stage design parameters [29] which have been used in both simulation and analytical models, while TABLE III lists the main parameters associated with the power DMOSFETs used in the analytical model.

Fig. 2.9 shows the comparison between the transistor-level simulation results and the analytical model, with two different I_{out} settings. The analytical model predicts the dissipation of the power switches well across the three different switching scenarios, with the switching frequency f_{sw} varied for getting to different I_{rip} such that all three scenarios can be covered. The main discrepancy between the analytical model and the simulation lies in the PSSw region. This is due to the nonlinear C_{par}, which makes the remaining voltage and charge ratio F in (2.12) not precise.

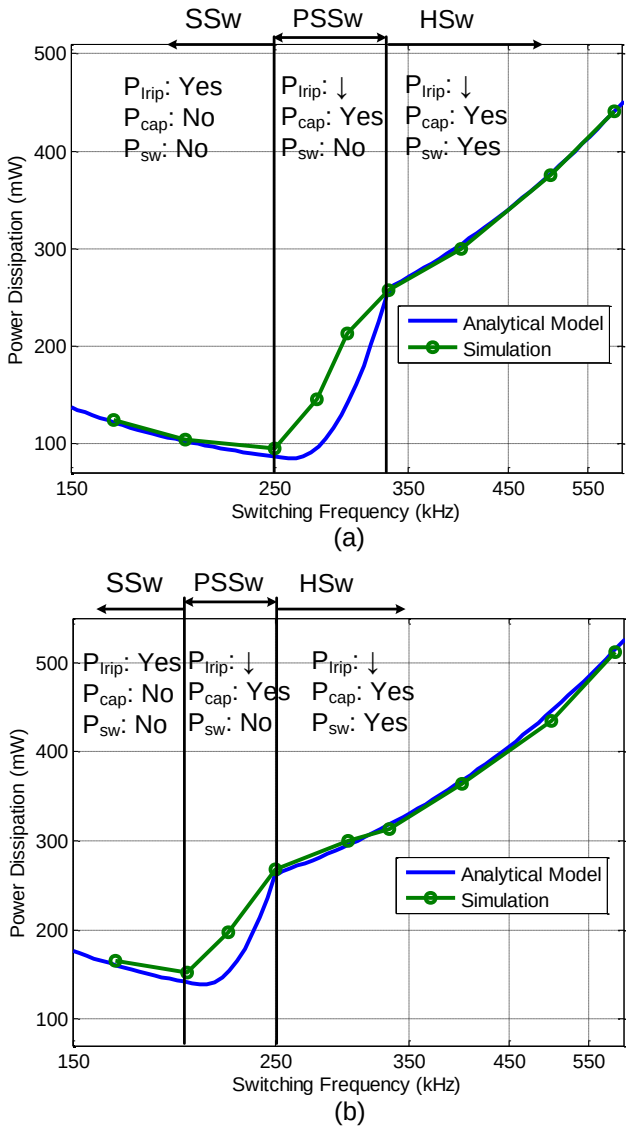


Fig. 2.9. Comparison between analytical model and transistor-level simulation for the dissipation of the output stage. (a) I_{out}=300mA. (b) I_{out}=400mA. Here we use "yes" for the presence of a specific dissipation source and "no" for absence.

2.5 Design Optimizations: Motivation for Research in Chapter 3-5

2.5.1 Reducing switching loss

In the derivation of (2.9), the switching loss during hard switching, we have assumed that the V-I overlap part contributed by I_L (I_L*(t_2-t_1)) is much smaller than the reverse recovery current contribution (Q_{rr}). This requires that the gate driver pull-up strength is large enough

to make the transition time t_2-t_1 very short. The design challenges this brings with respect to supply bounce and the subsequent realization of a fast-switching class-D power stage will be discussed in Chapter 3.

2.5.2 Extending high-efficiency output power range

When comparing Fig. 2.9(a) and Fig. 2.9(b), we can observe that a minimum power dissipation exists for each I_{out} case, each with a different optimal switching frequency. This motivates us to investigate on when the switching frequency is optimal and how to get to it. Then by varying f_{sw} in the desirable way we can extend the high-efficiency output power range, as will be discussed in Chapter 4.

2.5.3 Improving efficiency at idle/low output power

Fig. 2.10 shows the simulation result using the analytical model of the class-D power stage dissipation at two different dead time t_d settings (50ns and 200ns respectively with 200mA I_{out}). With the larger t_d setting, the output stage can achieve a lower total dissipation. The reason is that the larger t_d allows lossless SSw with less I_{rip} and thus higher f_{sw}, where I_{rip} induced loss P_{Irip} is less. This fact can be exploited to further optimize the efficiency at idle/low output power. However, inserting a larger t_d to the output stage for efficiency improvement will compromise the distortion performance [72],[73]. The simultaneous optimization of low-power efficiency and linearity performance will be further discussed in Chapter 5.

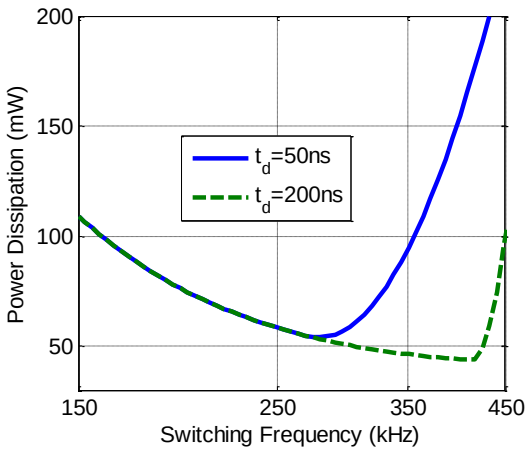


Fig. 2.10. Analytical model simulation of the class-D power stage dissipation at I_{out}=200mA, with a dead time of 50nS and 200ns respectively.

2.6 Conclusions

In this chapter, a detailed analytical modeling of the main class-D power stage dissipation sources is established. Further more, the analytical loss model is verified by comparing to transistor-level simulation results of across all load conditions and switching scenarios. Based on the power loss analysis, directions for further optimizing the power stage efficiency are given, which serve as motivations for the works done in chapter 3-5.

CHAPTER THREE

3. Switching Loss Reduction – Fast-Switching Power Stage Design

(Section 3.2 to section 3.6 are taken from the author's paper published in IEEE Journal of Solid-State Circuits in 2014 [29].)

3.1 Introduction

As discussed in section 2.5.1, fast switching transitions are crucial in a class-D power stage, since the V-I overlap loss dissipated in the power switches during a hard switching transition is directly proportional to the V_{pwm} transition time. Yet one significant design problem associated with a fast switching power stage is the on-chip supply bounce [8],[29]. Consequently switching speed is typically limited as to limit the on-chip supply bounce. This section will discuss the design of a power-efficient high-voltage power stage, where fast switching and the capability to handle the significant on-chip supply bounce are achieved simultaneously.

The output current switching between the high-side and low-side power switches causes a large di/dt, leading to on-chip supply bounce caused by parasitic inductances. For high-voltage DMOS output devices, the maximum allowed gate-source voltage (V_{gs}) is the same as for normal MOS devices in the same process node and is much lower than their maximum drain-source voltage (V_{ds}). The integration of complex signal processing functions and features on the same chip as the power blocks necessitates the power stage design in deep-submicron process nodes. However, the supply bouncing magnitude of several volts, while

not yet a problem in [8]-[14], makes the design in these smaller process nodes prone to performance degradation or even malfunction.

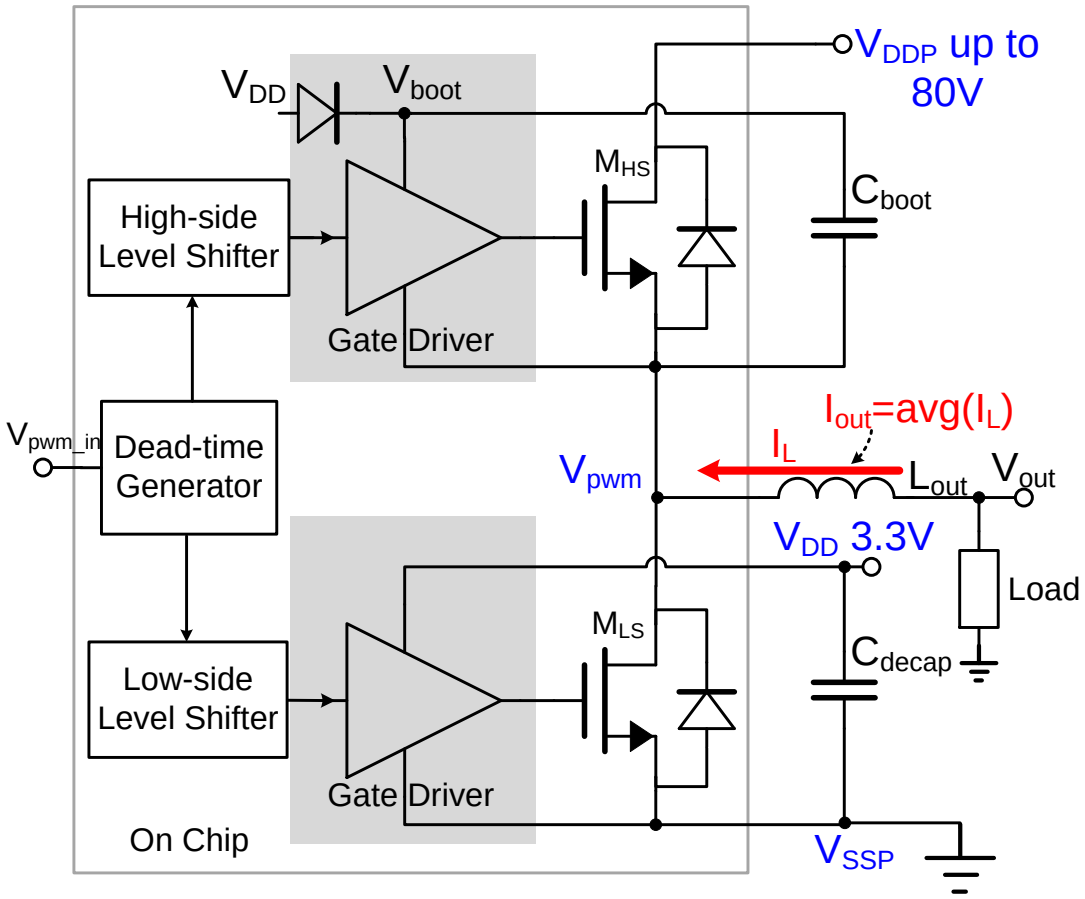


Fig. 3.1. Topology of a typical class-D power stage

In [14], parallel-connected power switches with weighted size are configured to perform staged turn-on/off for preventing inductive flyback to the supply rails. This way supply bounce can be reduced, with some tradeoff on efficiency because the turn-on of the HS and LS power switches has to be overlapped. Active clamp circuits [74] [76] can also be used as an effective way to reduce the voltage stress across the power switches and prevent damage to circuits. Yet the clamping can only mitigate power supply overshoot, while undershoot associated with the supply bounce is not clamped. In this chapter we describe a gate driver topology that overcomes the supply bouncing issue and enables a high-voltage, high-power class-D power stage design in a deep-submicron process node [29]. This is achieved by using gate drivers with on-chip regulated floating supplies, with the low-voltage driver and control circuits fully shielded from all the supply bounce. Moreover, simultaneous supply bounce

minimization and efficient switching transitions are realized by adopting an in-cycle variable gate-driving strength.

This chapter is organized as follows: in section 3.2 we show a detailed analysis of the gate driver sizing considering the on-chip supply bounce and its associated power efficiency degradation issues. The proposed floating gate driver and in-cycle variable gate-driving strength techniques for realizing efficient switching transitions are described in section 3.3. In Section 3.4 the requirement overview and circuit topology of the level shifter circuit for the class-D power stage are analyzed. Section 3.5 discusses the measurement results and in section 3.6 the conclusions of this chapter are drawn.

3.2 Gate driver sizing issues

A typical class-D power stage for high-voltage high-power applications consists of two identical NDMOS devices as High Side (HS) and Low Side (LS) switches as shown in Fig. 3.1. Since for DMOS power transistors the maximum V_{gs} is typically much lower than the maximum V_{ds}, the LS gate driver is supplied by a separate low-voltage supply and externally decoupled. For the HS gate driver, an external bootstrapping capacitor can be used as the supply. Here we use the three-line earth symbol for the power ground V_{SSP}, which is the off-chip reference ground. Later in the chapter the single-line ground symbol will be adopted to represent the on-chip grounds as to distinguish them from the off-chip reference ground. The circuit parameters of this power stage used for the simulations in this chapter are summarized in TABLE IV. The switching frequency f_{sw} is chosen at 500kHz as a typical value of class-D f_{sw} in general [8]-[14]. For piezoelectric-actuator applications, a lower f_{sw} can also be used if the signal bandwidth is lower. The output DC current I_{out} is the average inductor current I_L within one switching cycle. It is set at 1A with the output V_{pwm} duty cycle being 0.5. This represents the scenario of the instant when the output stage is discharging the capacitive piezoelectric load from mid-supply. Nevertheless, the analysis itself is general and also holds for other output current and duty cycle combinations, as well as when the output stage is processing a dynamic output signal.

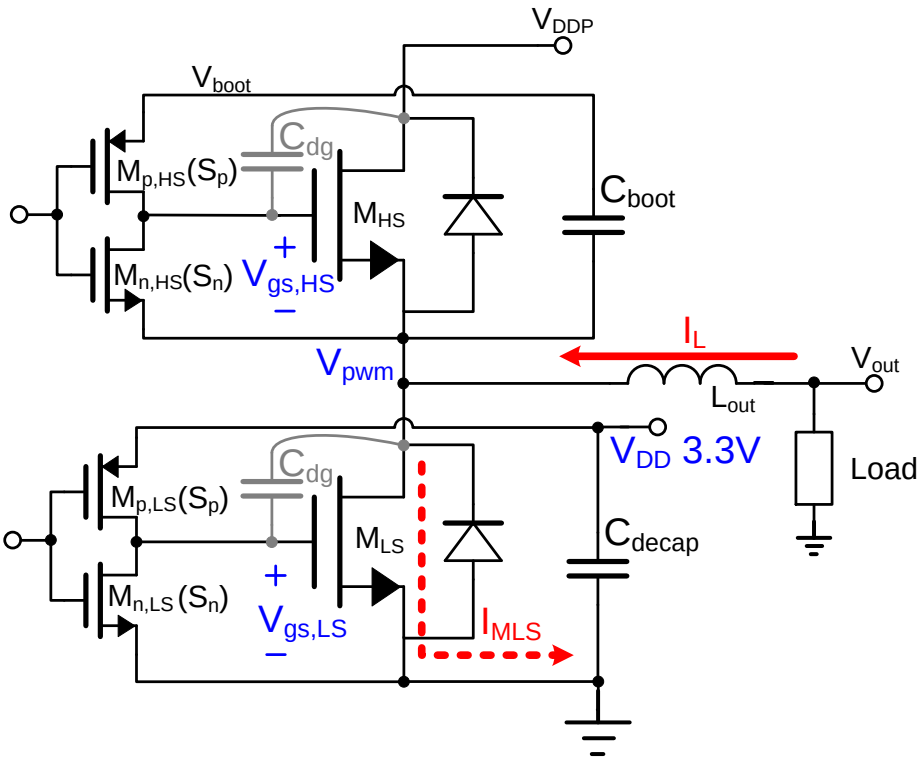


Fig. 3.2. Circuit diagram with combined gate driver and output power switches for analyzing class-D power stage switching dynamics

TABLE IV. SUMMARY OF THE PARAMETERS USED IN THE POWER STAGE SIMULATION

Parameters	Value
Power Stage Supply V_{DDP}	80V
DMOSFET's Maximum V_{gs}	3.3V
Output Inductance L_{out}	100µH
Switching Frequency f_{sw}	500kHz
Output DC Current I_{out}	1A
V_{pwm} Duty Cycle	0.5
Dead Time t_d	100ns

3.2.1 Power Transistor Dissipation

To emphasize on evaluating the gate driver sizing influence on the switching loss, we categorize the dominating power loss in the power MOSFETs of a high-voltage Class-D output stage into three types of losses for simplicity [34]: 1) P_{cond}: conduction loss (both from I_{out} and I_{rip}, so $P_{cond} = P_{con} + P_{Irip}$ in TABLE I on page 14) caused by the power MOSFETs' r_{on}. 2) P_{cap}: capacitive loss caused by charging and discharging parasitic capacitances on V_{pwm},

and 3) P_{sw} : switching losses caused by V-I overlap in the switches during switching transitions. Compared to the analysis made in Chapter 2, the gate driver loss P_g is neglected here as at most output powers it is much smaller than the three listed above. Among the three dissipation sources, P_{cond} is inversely proportional to the power transistor size S while P_{cap} is proportional to the power transistor size S. As for P_{sw}, in the optimal case (very fast switching) its dominant contribution is the intrinsic reverse-recovery current [11] and this is also proportional to the power transistor size S. The total dissipation can then be optimized by choosing the correct transistor size to balance the three power dissipation sources [34]. Under the circuit operating conditions in TABLE IV, an optimized DMOS power transistor size is derived as 56000μm/0.75μm, with TABLE V listing each dissipation source and their respective contributing ratio. This optimization is considered in the ideal case, i.e. with no power supply parasitic inductances included.

Because our first attempt here is to examine what the dissipation sources should be and how they contribute to the total dissipation in the optimal case, the driver stage (Fig. 3.2) for driving the two power switches should also be designed to behave as close to ideal drivers as possible in this optimization. This has two implications 1) the drivers should turn on the power switches very fast such that the main contribution to V-I overlap is caused by the reverse-recovery current. Since we do not consider power supply parasitic inductances in this phase, the driver pull-up transistor can be increased as much as necessary to reach this minimum P_{sw}. The minimized P_{sw} is then proportional to the reverse-recovery charge in the body diode and thus proportional to the power transistor size S. 2) The driver should turn off the power switches very fast and then be able to completely keep the power switches off when required. Similarly since power supply parasitic inductances are not considered yet, the driver pull-down transistor is sized to be much larger than the pull-up transistor as to avoid cross conduction [77].

TABLE V. LIST OF EACH DISSIPATION SOURCE WITH AN OPTIMIZED POWER TRANSISTOR SIZE S OF 56000μm/0.75μm

Dissipation Source	Power Loss Type	Power Loss	Ratio	
Total Output DMOSFETs' Loss	Balanced	1.2W	100%	
P_{cond}	$\propto 1/S$	570mW	48%	
P_{cap}	$\propto S$	120mW	10%	52%
P_{sw}	$\propto S$	510mW	42%	

However, although switching can be arbitrarily fast in this optimization procedure, in reality it will cause large di/dt, and consequently supply bounce which affects the circuit operation. In the following subsection we will show how the gate drivers influence the supply bounce (di/dt) for different switching scenarios and how efficiency deteriorates if supply bounce has to be limited by proper gate driver sizing.

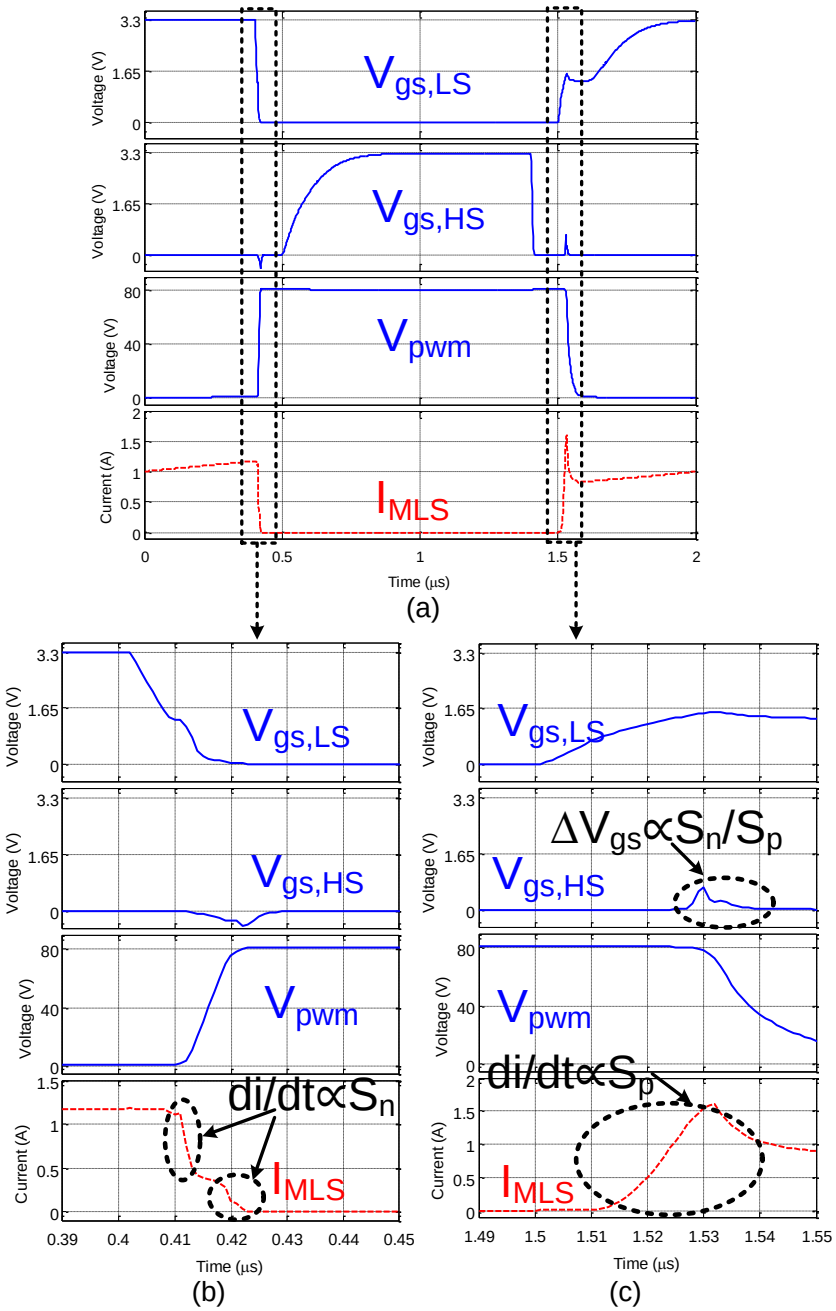


Fig. 3.3. Simulation waveforms with both V_{pwm} soft switching and hard switching transitions. (a) One complete switching cycle (b) Soft switching transition (c) Hard switching transition

3.2.2 Supply Bounce Analysis and Gate Driver Sizing

The switching behavior of a class-D output stage can be categorized into two types of switching transitions: soft switching, where I_L (dis)charges the parasitic output capacitance of the switch transistors and hard switching, where the transistors (dis)charge these parasitics [74]. Depending on the relative amplitude of the inductor ripple current and the load current, I_L can either be bidirectional with both switching transitions being soft switching or unidirectional, where one transition is soft switching and the other is hard switching. The power stage circuit diagram in Fig. 3.2 is used to illustrate the two switching transitions. The load current I_L is flowing into the power stage and keeps flowing in this direction during the full switching cycle. Fig. 3.3(a) shows the simulation waveforms in one complete switching cycle, consisting of soft and hard switching transitions while Fig. 3.3(b) and Fig. 3.3(c) shows the two edges in detail.

In Fig. 3.3(b) for the soft switching transition edge, the V_{pwm} low-to-high transition starts when M_{LS} is turning off, and I_L provides the current to charge V_{pwm} to V_{DDP} without resorting to the active devices. From the driver sizing point of view, when we look at the current flowing in M_{LS} (I_{MLS}), first, I_{MLS} is decreased such that I_L can provide for the current necessary to charge the M_{LS} parasitic capacitances and to discharge the M_{HS} parasitic capacitances. Then there comes a period where V_{pwm} is slewing and I_{MLS} keeps nearly constant. When the slewing is over, I_{MLS} is further decreased to be conducted by the HS body diode within the dead time. During both times when I_{MLS} is decreasing, the di/dt is proportional to how fast M_{LS} is being turned off, and thus is proportional to the gate driver pull-down (PD) transistor $M_{n,ls}$ size S_n.

For the hard switching transition as shown in Fig. 3.3(c), first M_{HS} is turned off, and the current flows through the M_{HS} back-gate diode. V_{pwm} remains high until M_{LS} has been turned on and has taken over all the load current as well as the current for discharging the V_{pwm} node. The rate at which I_{MLS} is increasing during this time is proportional to the driver pull-up (PU) transistor $M_{p,LS}$ size S_p. After that, V_{pwm} starts slewing with a rate determined by $C_{dg,LS}$ and the on resistance of $M_{p,LS}$ (with size S_p). This slewing will also cause the M_{HS} gate-source voltage to rise through $C_{dg,HS}$ and the on resistance of $M_{n,HS}$ (with size S_n), so the driver PD transistor $M_{n,HS}$ should be sized with a much lower on resistance than PU transistor $M_{p,LS}$ to avoid cross conduction.

Because the HS and LS drivers and power switches are identical, the driver size versus di/dt analysis made above also holds for the case that the V_{pwm} high-to-low transition is soft switching while the V_{pwm} low-to-high is hard switching. The difference is that, since the HS gate driver supply is referred to V_{pwm}, the di/dt of the current flowing in M_{HS} and the subsequent supply bounce on V_{DDP} will not influence the HS gate driver supply. This will only be the case for class-D output stage topologies employing complementary output power transistors [9].

In conclusion, regarding the relationship between the gate driver sizing and the switching dynamics, 1) S_n is limited by the permissible di/dt in soft switching 2) S_p is limited by the permissible di/dt in hard switching, and 3) $S_p/S_n << 1$ to prevent cross conduction during hard switching. From 1)-3) we further conclude that S_n in soft switching is the major concern when it comes to supply bounce.

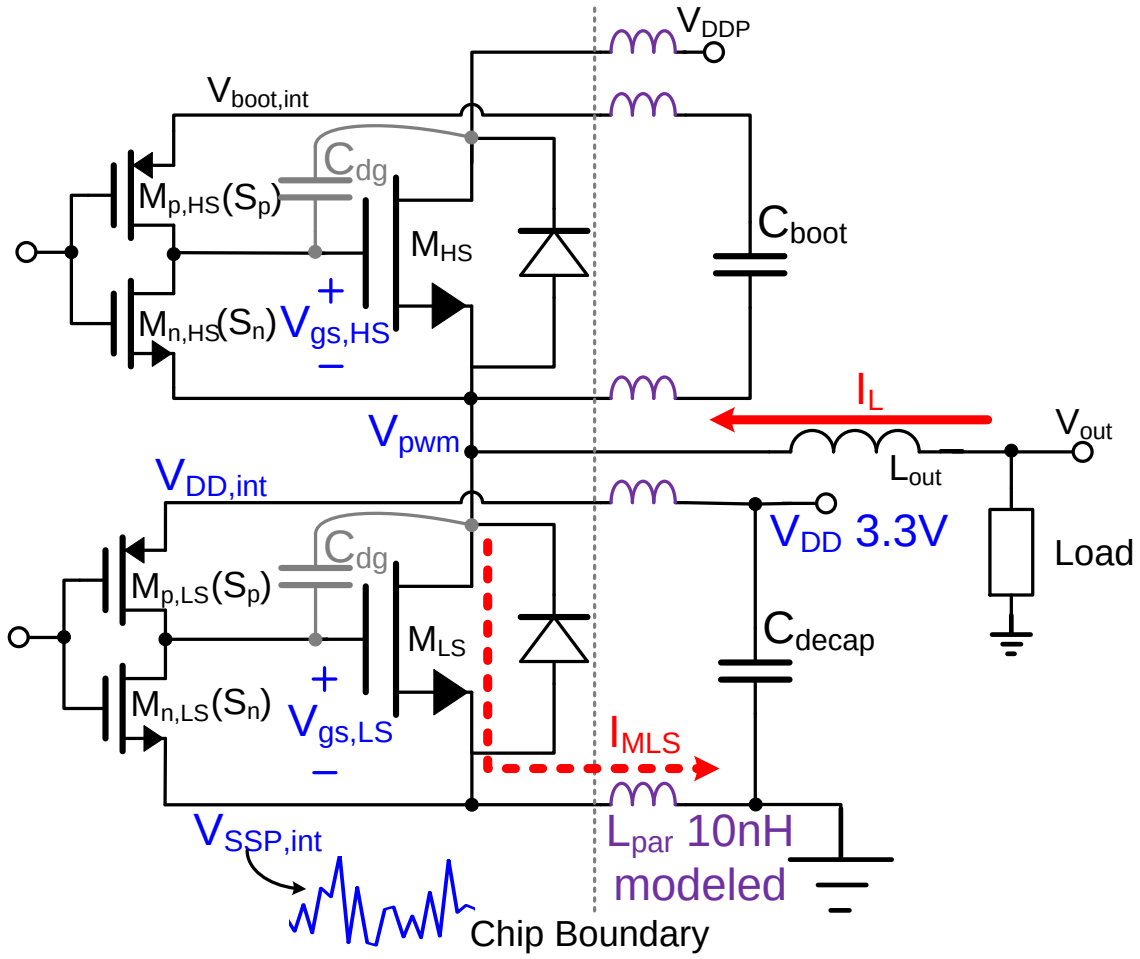


Fig. 3.4. Class-D power stage with power supply parasitic inductance included

For relating the analyzed di/dt to the on-chip supply bounce, the class-D power stage with parasitic inductances of power supply and decoupling capacitor included is shown in Fig. 3.4. The parasitic inductances consist of bond wires, lead fingers, and PCB traces between the on-chip power supply pads and the decoupling capacitors of the external power supplies, which can easily add up to tens of nano-Henrys [8]. With a modeled parasitic inductance L_{par} of 10nH, Fig. 3.5 illustrates the influence of the bounce on the power stage switching transitions with 3.3V gate driver supply. Even though in this simulation 500pF on-chip V_{DD} decoupling was added between $V_{DD,int}$ and $V_{SSP,int}$, and furthermore extremely slow switching was adapted to ensure that oscillatory switching transitions [83] are overcome, 60% variation on the gate driver supply is evident with the modeled L_{par} of 10nH. The main concerns here include the robustness considerations for the low-voltage circuit blocks as well as the suboptimal switching loss P_{sw} performance. To gain insight into how efficiency gets deteriorated, the gate driver sizing procedure with constrained on-chip supply bounce is derived as follows,

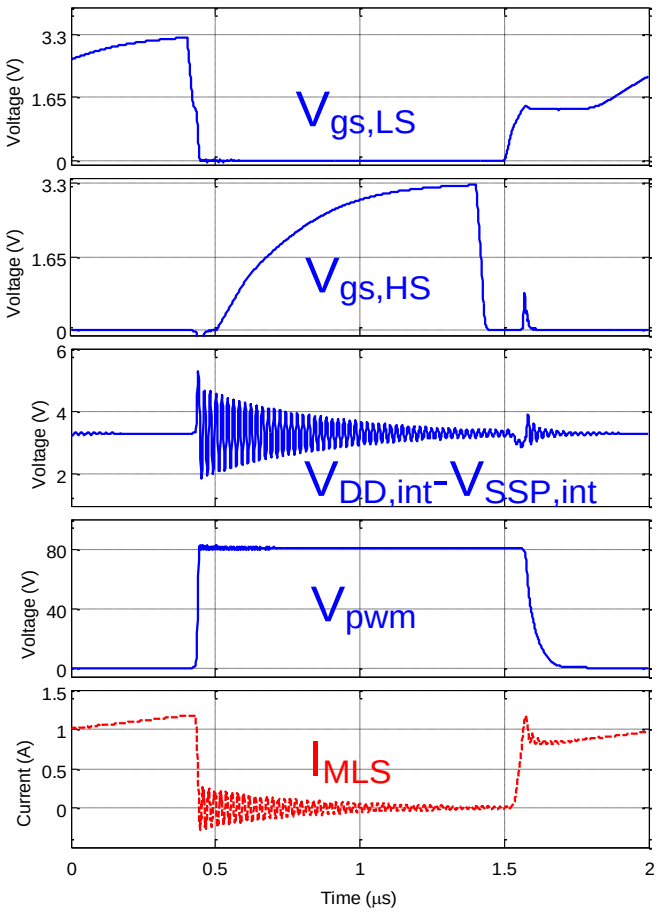


Fig. 3.5. Simulation waveforms illustrating the influence of supply bouncing, V_{pwm} high-to-low transition has to be extremely slow and results in high switching loss.

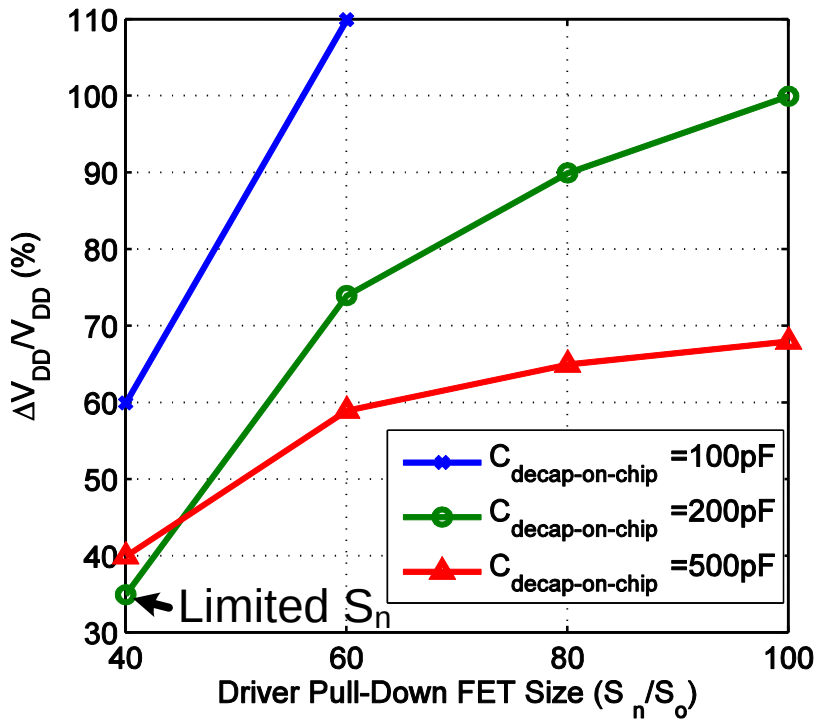
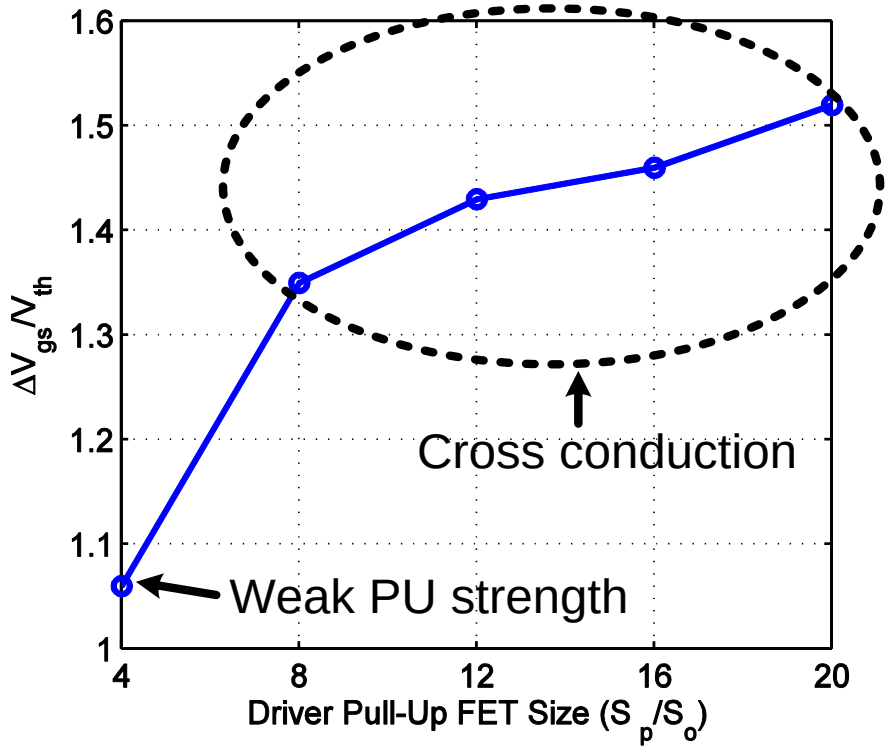


Fig. 3.6. Simulation result of different driver pull-down transistor size and the corresponding on-chip supply bouncing, under different on-chip decoupling capacitor values, S_n value is normalized to a S_o of 3.2μm/0.32μm.

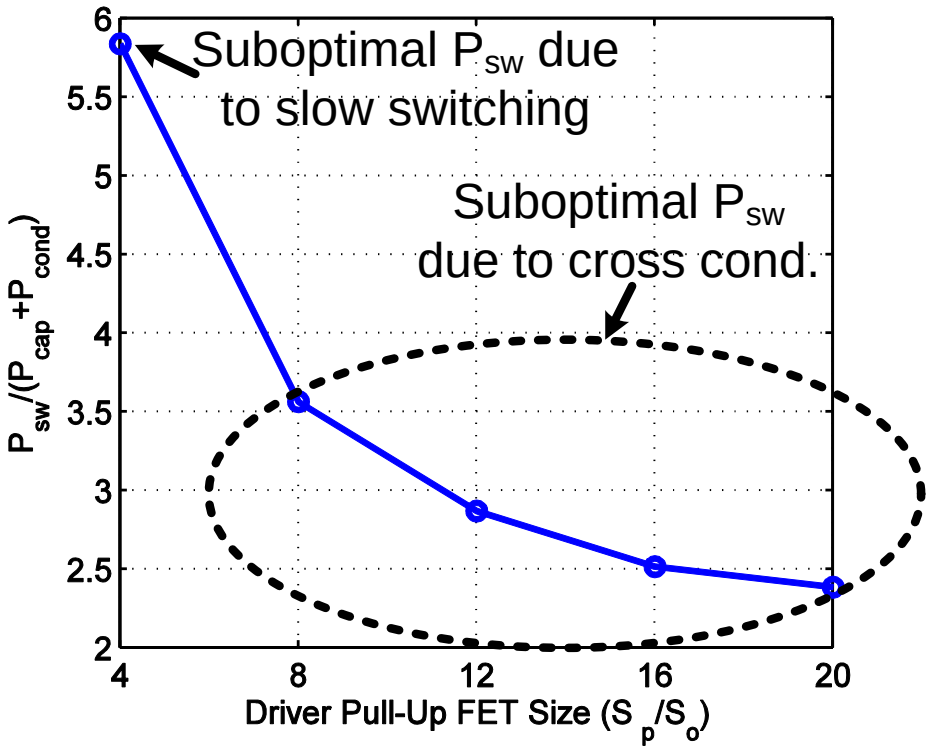
(1) Determine the driver pull-down transistor size S_n, based on the tolerable maximum gate driver supply bounce limited by soft switching transition.

Fig. 3.6 shows the simulation result of different driver pull-down transistor size and the corresponding on-chip supply bouncing, for different on-chip V_{DD} decoupling capacitor values. We see that the on-chip V_{DD} bounce increases with the driver pull-down transistor size. Also, adding more on-chip decoupling capacitor will help to decrease the bounce, but with limits. As also shown in Fig. 3.6, for a $S_n/S_o = 40$ to limit the bounce, adding on-chip decoupling capacitor from 200pF to 500pF will not decrease the on-chip bounce anymore, primarily because the L_{par}-$C_{decap\text{-}on\text{-}chip}$ bandwidth limits the effectiveness of bounce suppression.

(2) Determine the driver pull-up transistor size S_p, limited with respect to the pull-down transistor S_n for avoiding cross conduction of the two output power DMOS switches.



(a)



(b)

Fig. 3.7. Driver pull-up transistor sizing with S_n/S_o chosen at 40. S_n and S_p values are normalized to an S_o of 3.2µm/0.32µm. (a) S_p limited for avoiding cross conduction (b) Suboptimal switching loss performance

Considering the already limited S_n for suppressing the on-chip supply bounce, S_p is further limited by the requirement to avoid cross conduction. This means that hard switching transitions have to be either extremely slow or cause cross conduction, with both cases causing suboptimal switching loss. Fig. 3.7(a) shows the S_p sizing when S_n/S_o has been chosen at 40. The efficiency degradation caused by this limitation is evident in Fig. 3.7(b).

An increase of S_p/S_o from 8 to 20 results in faster switching, which lowers $P_{sw.}$ However, a larger S_p also results in cross conduction, adding to P_{sw}, so P_{sw} is not reduced to the optimal value compared to the other losses $P_{cond} + P_{cap}$ (optimum ratio should be 0.72 as in TABLE V).

Since the main factor that determines the power supply bouncing during switching transitions is the driver-size-related di/dt, the analysis made above is not limited by the power transistor size chosen in TABLE V. If a different power transistor size is chosen, the driver size will have to be scaled accordingly to meet the same requirement on di/dt as well as on avoiding cross conduction. Consequently the design trade-offs for limiting the di/dt in soft switching and aiming for fast transitions in hard switching are the same. Regarding the effect of process and temperature variation on the on-chip supply bounce magnitude, the analysis of the relationship between the driver transistor size and the bounce magnitude also holds. A decrease in temperature or a fast process corner has the same effect as an increase in transistor size, which will cause more bounce. Additionally, in designs where a larger L_{par} than the modelled 10nH exists through longer decoupling loops, e.g. larger packages than required or decoupling capacitors placed far away from the supply pins, the supply bounce magnitude will also increase.

3.3 Floating gate driver design

3.3.1 Floating Gate Driver with Regulated Supply

To overcome the on-chip driver supply bouncing issue without sacrificing efficiency during switching transitions, we propose a gate driver topology with on-chip regulated floating supply. As shown in Fig. 3.8(a), two on-chip voltage regulators are used to provide stable on-chip supply voltages to the gate driver circuits. The two regulators track the two reference nodes $V_{SSP,int}$ and V_{pwm} respectively, so the on-chip bouncing will not be seen by

the driver circuits. The unregulated input supply voltage for the regulators are chosen based on the estimated maximum bouncing magnitude plus the minimum operation voltage of the regulator circuits (12V unregulated V_{DD} is used here). The detailed gate driver circuit is shown in Fig. 3.8(b). The pull-up current has been divided into two parts. The main I_{pu} is supplied by the unregulated V_{DD} while an auxiliary I_{pu} is used to turn the output power transistor fully on. By this configuration the regulators are not required to supply the hundreds of milliamps for I_{pu} and their design can be simplified. For the pull-down current path, an in-cycle variable gate driving strength is implemented and will be explained next.

3.3.2 In-Cycle Variable Gate-Driving Strength

As explained in the previous section, the main reason for excessive switching loss during hard switching is because the driver PU transistor has to be much weaker than the PD transistor, other than limited by on-chip bounce considerations. To circumvent this limitation of the driver PU strength, we propose to a use an in-cycle variable gate-driving strength [11]. As shown in Fig. 3.9(a), when the driver input and output status have both been detected as already off, the combined strength of M_{n1} and M_{n2} will be used to keep the power transistor off when the other driver is turning on based on the S_p/S_n driver ratio requirement. However, when the driver is in the process of turning its output off and hasn't yet reached the level determined by the Schmitt trigger, only the weaker M_{n1} will provide the pull-down current to turn off the output power transistor slowly in order to keep di/dt low (Fig. 3.9(b)). This way we have the design freedom to both choose the correct S_p/S_n ratio to avoid cross conduction, and limit the on-chip supply bounce. Simulation waveforms for comparing the effectiveness with and without the adaptive driver turn-off strength are shown in Fig. 3.10, with the modeled L_{par} of 10nH in the simulation. Fig. 3.10(a) shows that the same effect for keeping the power transistor off is obtained while Fig. 3.10(b) illustrates that the supply bouncing is significantly reduced when a weaker PD strength can be applied for turning the power transistor off. Fig. 3.10(a) and Fig. 3.10(b) are enlarged simulation waveforms within one switching period.

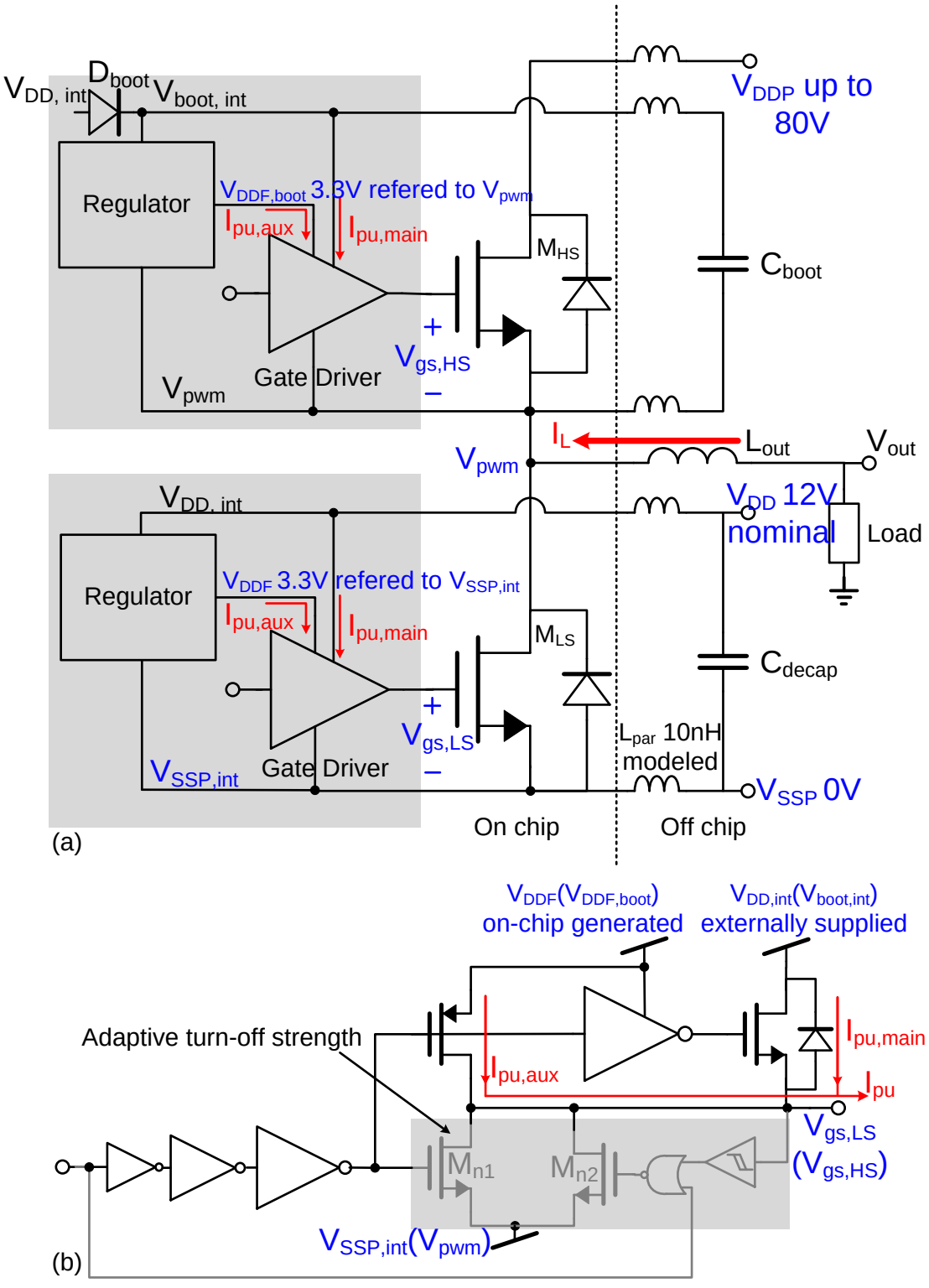


Fig. 3.8. Proposed power stage topology (a) supply bouncing influence on the functionality of the gate driver is eliminated by the on-chip regulated gate-driver supply (b) Detailed gate driver structure.

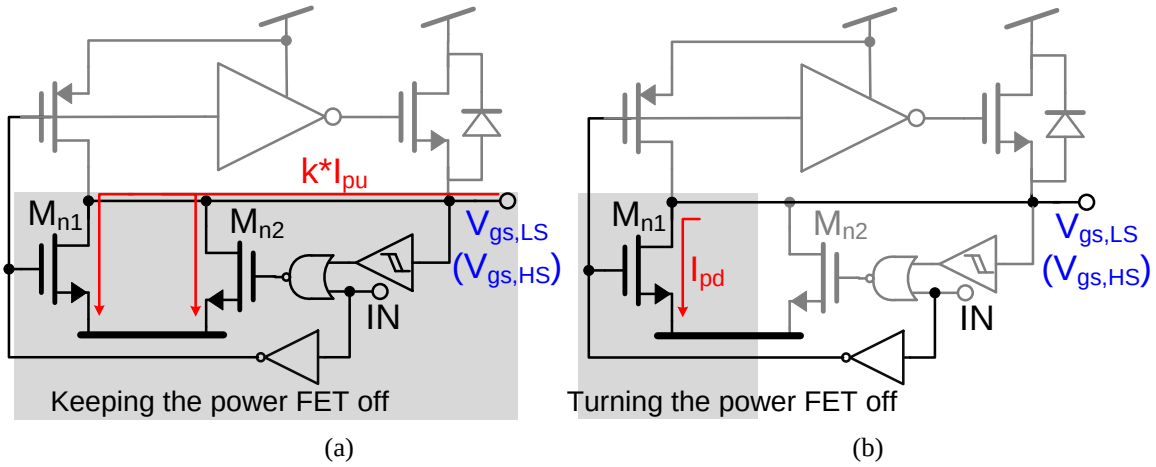


Fig. 3.9. Gate driver with adaptive turn-off strength (a) Stronger pull-down transistors for keeping the power transistor off (b) Weaker pull-down transistors for turning the power transistor off

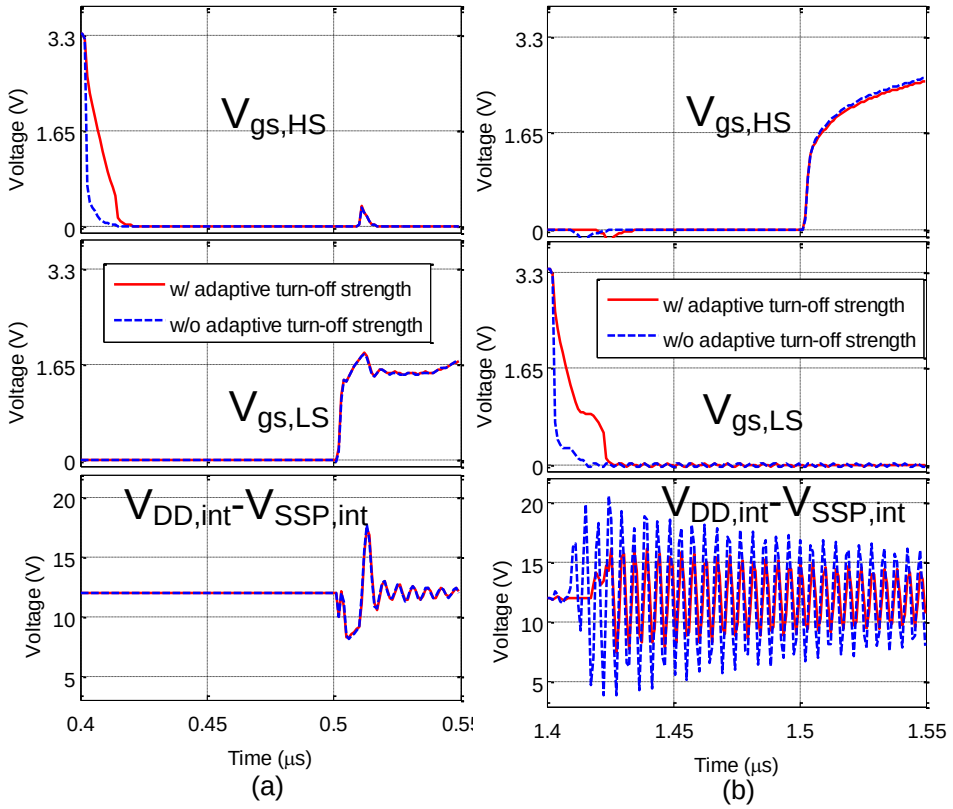


Fig. 3.10. Simulation waveforms for the on-chip supply bouncing with and without the adaptive turn-off strength within one switching cycle (a) When one power transistor turns on, the other power transistor can be kept off (b) On-chip supply bouncing can be significantly reduced.

3.3.3 Sizing of the Floating Gate Drivers

Compared with the sizing of the gate driver with externally decoupled low-voltage gate driver supply, the sizing of the floating gate driver combined with the variable gate-driving strength can now have the following advantages:

(1) The gate driver PD transistor can be sized larger, since the floating gate drivers can sustain a much higher on-chip supply bouncing amplitude and the floating regulated driver supplies will not be directly influenced.

As can be seen in Fig. 3.11, although the off-chip decoupled 12V supply still has large variations during switching, the on-chip floating supply varies only 10% with the adopted floating regulator circuit discussed in section 3.3.4. This variation is mainly due to the load regulation of the regulator for providing the PU current. Also, this clean gate driver supply is achieved without using area-consuming on-chip decoupling capacitors in the hundred pF range.

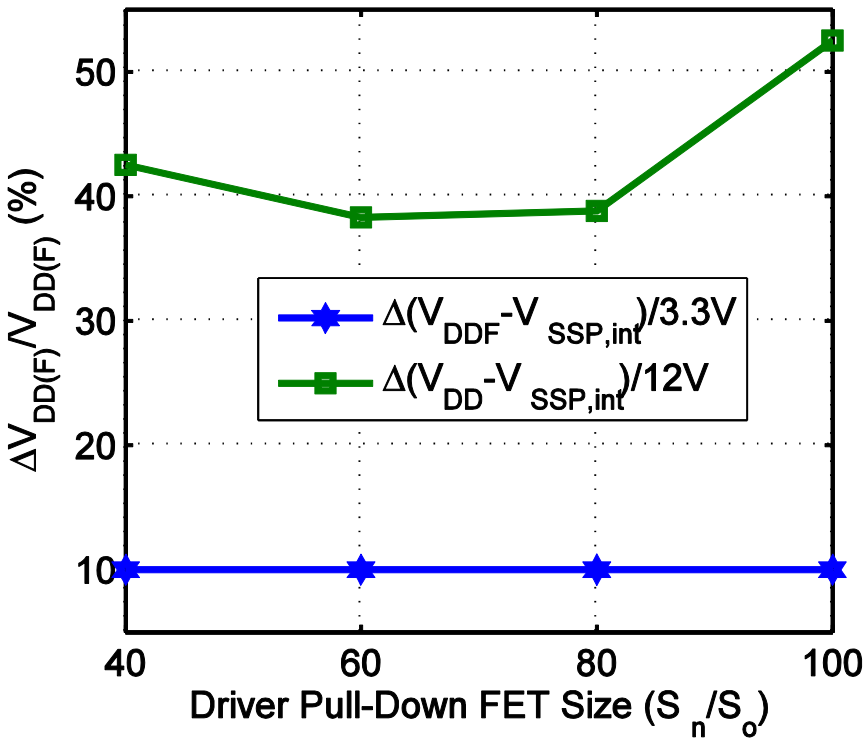
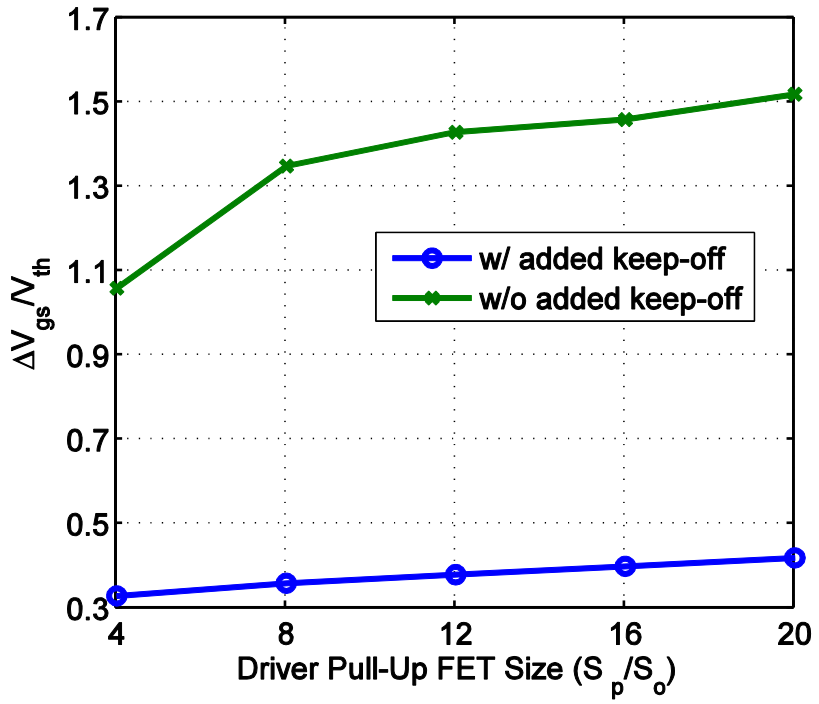
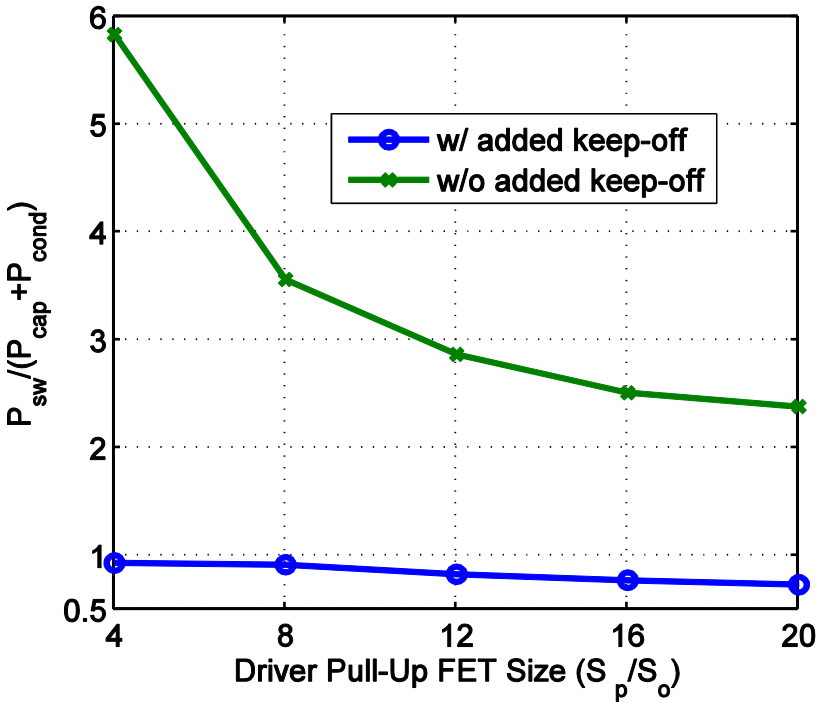


Fig. 3.11. Simulation result of the on-chip floating gate driver supply variation with respect to different gate PD strengths. S_n value is normalized to a S_o of 3.2µm/0.32µm.



(a)



(b)

Fig. 3.12. Simulation result of using different driver PU strengths, with S_n/S_o chosen at 40. S_n and S_p values are normalized to a S_o of 3.2µm/0.32µm. (a) Cross conduction is prevented by adding additional keep-off strength of $4xS_n$. (b) Fast hard switching transitions are realized with much smaller switching loss compared with the case using off-chip decoupled 3.3V gate driver supply

(2) The PU transistor can be sized larger to improve efficiency without getting limited by the maximum S_p/S_n ratio. Cross condition is avoided by the additional keep-off strength.

In Fig. 3.12(a) we see the effect of added keep-off strength to the PU transistor sizing. With the same S_n/S_o=40 as used in section 3.2 for limited bounce, 4x added keep-off strength can ensure that ΔV_{gs} is far below V_{th} when choosing S_p/S_o up to 20. Fig. 3.12(b) shows that efficient hard switching transitions can be realized since now larger PU transistor size can be adopted. With S_p/S_o set to 20, the $P_{sw}/(P_{con}+P_{cap})$ ratio is now 0.73, close to the minimized $P_{sw}/(P_{con}+P_{cap})$ ratio of 0.72 in TABLE V.

3.3.4 On-chip Floating Voltage Regulator

The on-chip floating regulator circuit for both HS and LS is shown in Fig. 3.13. For fast response and low output voltage ripple, the output $V_{DDF}/V_{DDF,boot}$ has been excluded from the feedback loop [87]. The drawback on precision is not critical here since the regulator supplies mainly digital blocks. The output devices of the regulator are also DMOS devices to sustain the higher 12V unregulated V_{DD} as well as the bouncing superimposed on it.

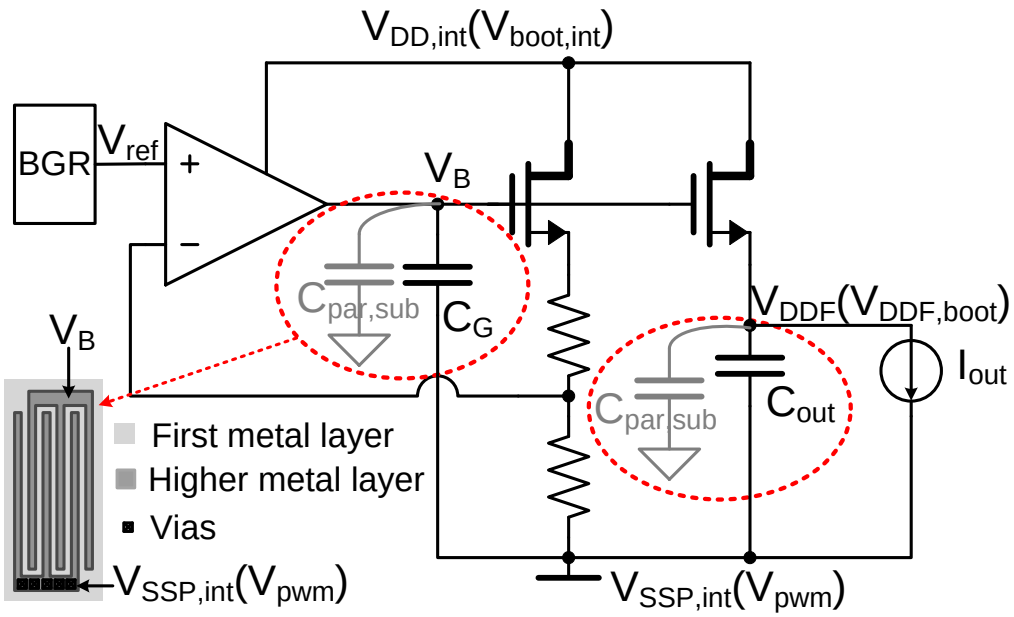


Fig. 3.13. On-chip regulator and its decoupling capacitor C_G implementation

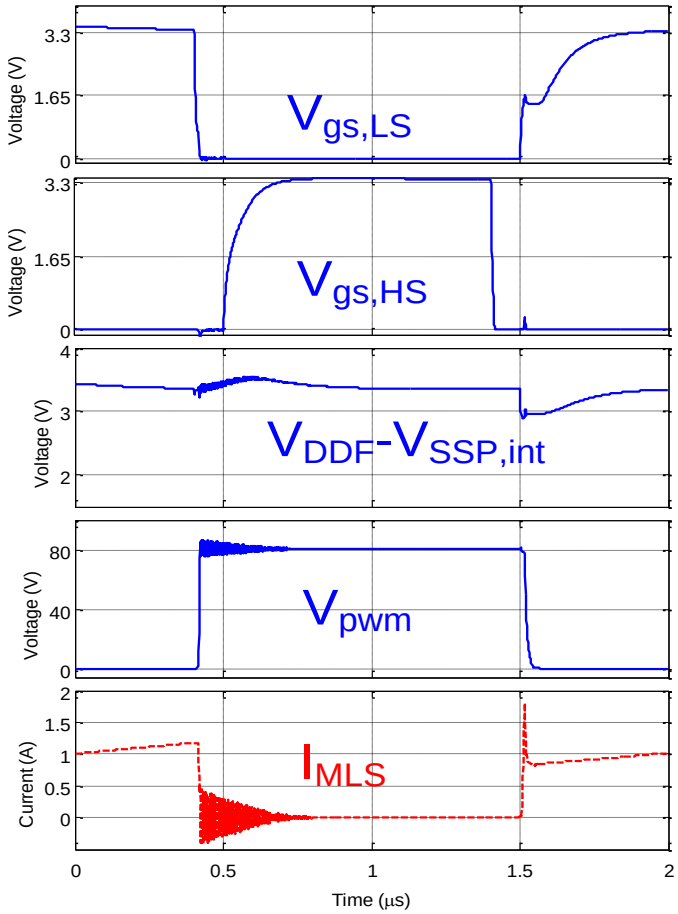


Fig. 3.14. Simulation waveforms of the power stage in Fig. 3.8, V_{pwm} high-to-low transition is fast, without disturbing the on-chip floating driver supply.

On-chip decoupling capacitor C_G is important for power supply ripple rejection. It is vital to minimize its parasitic capacitance $C_{par,sub}$ to the substrate as any disturbance from the $V_{SSP,int}/V_{pwm}$ node will be coupled to V_B by a ratio $C_{par,sub}/(C_G+C_{par,sub})$. As an example, the output voltage V_{PWM} slews 80V in a few nanoseconds; even with 1% parasitic capacitance 0.8V will be coupled to the 3.3V output, which is an unacceptable 25% variation. Consequently it is rather important that these decoupling capacitors are fully shielded from the substrate as shown in Fig. 3.13. Here for the metal fringe capacitor the whole first metal plate is connected to the $V_{SSP,int}/V_{pwm}$ node such that V_B is fully shielded. The output decoupling capacitor C_{out} has a value of 20pF, which is much more area efficient than the decoupling capacitor of an unregulated gate-driver supply (Fig. 3.6).

Efficient switching transitions as shown in Fig. 3.14 are achieved by this gate driver topology. The on-chip floating regulators provide a reliable 3.3V supply to the gate driver circuit during both soft- and hard-switching transients. Also, thanks to the in-cycle variable

gate-driving strength, the high-to-low hard switching here is performed fast, simultaneously avoiding cross conduction and excessive bounce on the off-chip decoupled 12V supply (Fig. 3.10).

3.4 Power-Efficient 2-step level shifter

Another important circuit block for the class-D power stage is the level shifter circuit [79]-[82]. It is used for communication between signals referred to the digital ground V_{SSD} and those referred to the power ground $V_{SSP,int}$ or the floating HS V_{pwm}, as shown in Fig. 3.15. With a 3.3V supply for both the low-voltage control blocks and the gate drivers, the on-chip supply bouncing magnitude higher than the 3.3V supply itself presents a challenge for reliable level shifting. As shown in Fig. 3.15, the >3.3V bounce causes the voltage potential between V_{DDF} and V_{SSD} to be very uncertain. This makes conventional level shifting by building a direct interface circuit using V_{DDF} and V_{SSD} as power and ground [8], [79], [80] not feasible. For reliable level shifting, a two-step approach has been adopted here, where the voltage level is first referred to the higher 12V $V_{DD,int}$ and then to $V_{SSP,int}$.

In addition, compared to level shifters used for transferring to voltage levels referred to fixed supply rails [9], [81], [82], level shifting to the slewing V_{pwm} is associated with disturbance that could corrupt the transferred signal. We consider the SR latch referred to the V_{pwm} voltage domain as shown in Fig. 3.16. The supply rail referred to V_{pwm} has the same high slew rate as V_{pwm} (up to 10kV/μs in this design). If there exist parasitic capacitances e.g. to the substrate at the input of the latch, and the stage preceding the latch has a resistive load, this directly translates to a common-mode disturbance for the latch and a possible logic output error can occur.

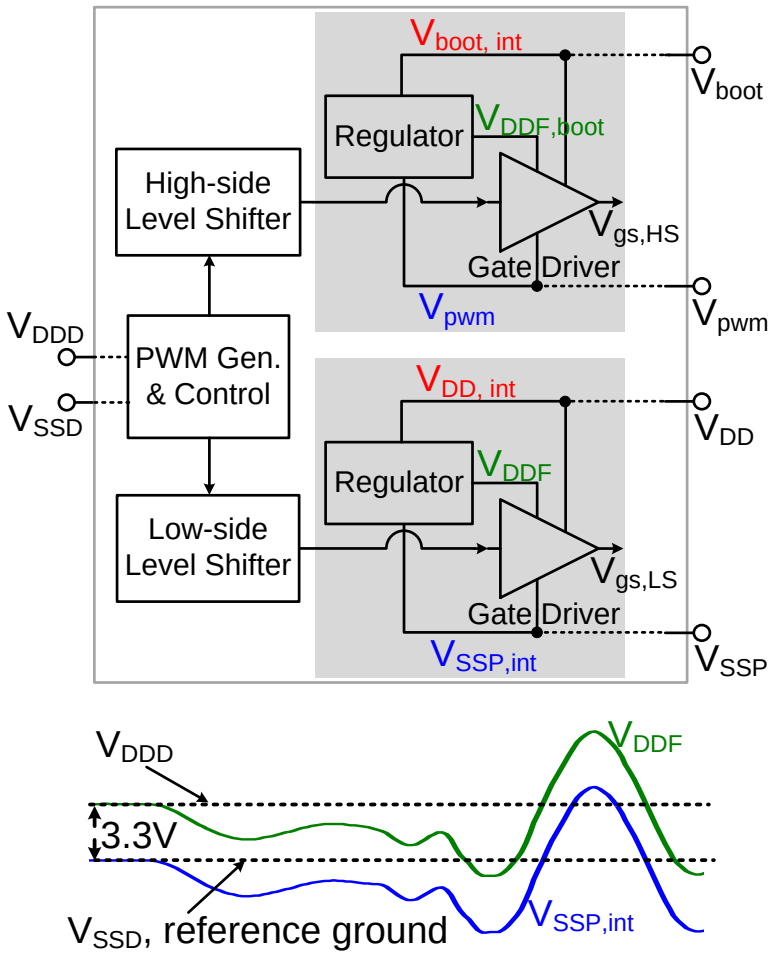


Fig. 3.15. Illustration of the communication between different voltage domains by the level shifter

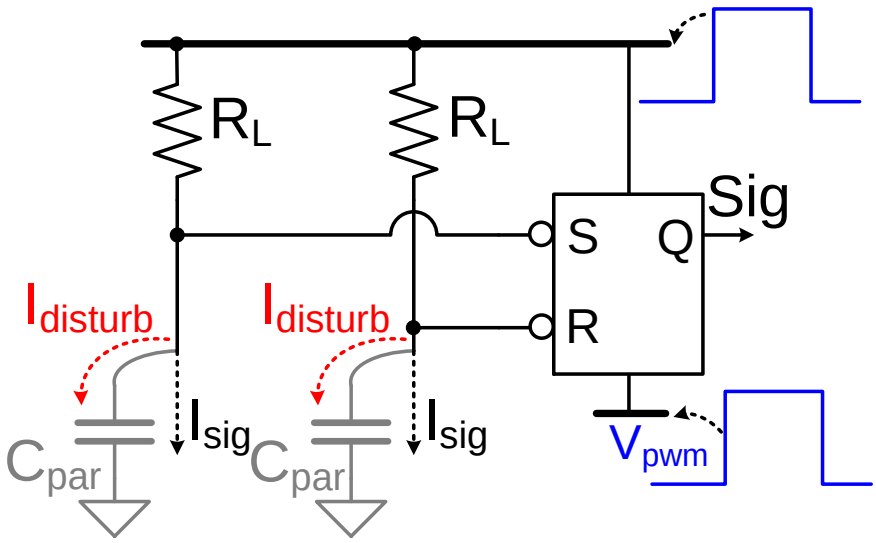


Fig. 3.16. Slewing for the voltage levels referred to V_{pwm} can cause error output of the level shifter

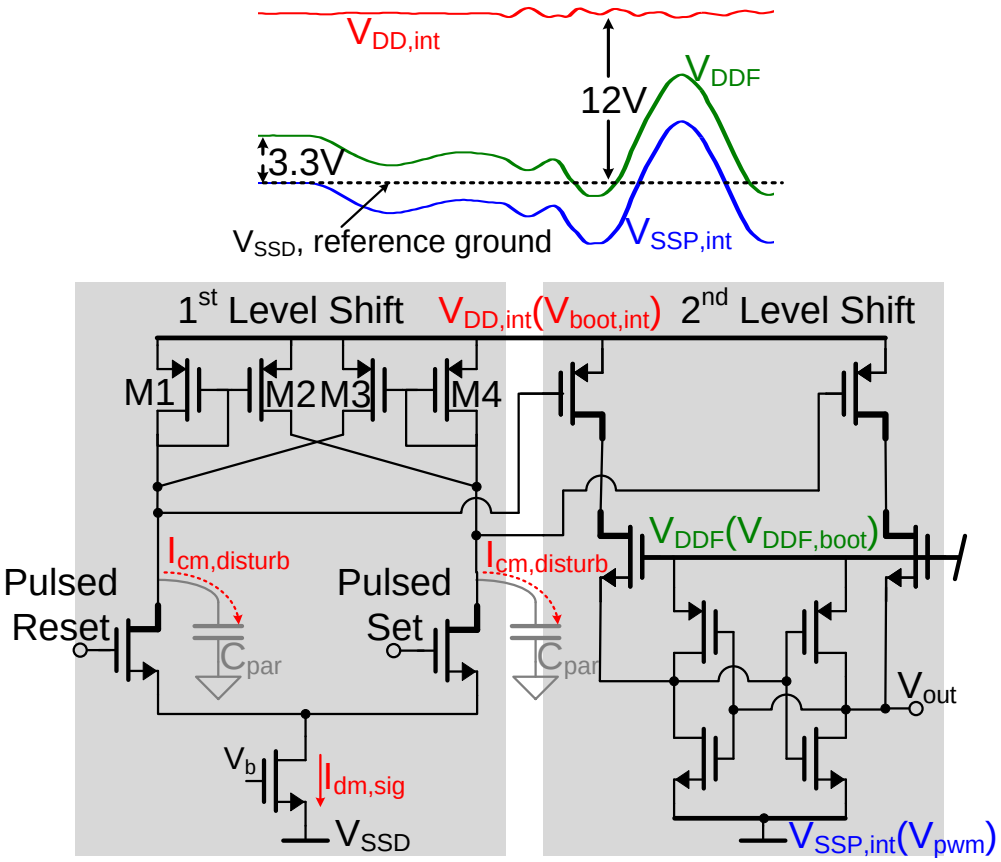


Fig. 3.17. Level shifter circuit and illustration of the on-chip supply/ground waveforms which necessitates a 2-step approach for the level shifting

To cope with the >3.3V supply bounce, the two-step level shifting approach is shown in the circuit schematic in Fig. 3.17, where the voltage level is first referred to the higher 12V $V_{DD,int}$ and then to $V_{SSP,int}$. As shown in Fig. 3.17, the already available 12V $V_{DD,int}$ referred to V_{SSD} is not influenced too much by the bounce and thus establishing a reliable interface circuit across $V_{DD,int}$ and V_{SSD} as the 1st level shifting step. Subsequently the 2nd level shifting transfers the signal to the one referred to $V_{SSP,int}$, tolerating the supply voltage variation between $V_{DD,int}$ and $V_{SSP,int}$.

For the HS level shifter circuit, the power dissipation could be significant because the current for transferring the signal has to flow between the maximum 92V $V_{boot,int}$ and ground. Two approaches have been implemented in the level shifter circuit of Fig. 3.17 to minimize its power dissipation and make it power efficient for HS usage. Firstly, pulsed set and reset input are applied such that only pulsed current are bridging most of the 92V [80]. Additionally, we introduce an active load (transistors M1-M4) with partial positive feedback characterized by a lower impedance for common-mode disturbances like $V_{DD,int}$ or V_{pwm}, and

a higher impedance for the differential-mode signal pulses. The diode-connected M1 and M4 are configured with slightly larger W/L ratio compared with the cross-coupled M2 and M3. From a large-signal perspective, approximately 2x larger (M1+M2) and (M3+M4) are used for conducting the common-mode disturbance current $I_{cm,disturb}$ while only M1 or M4 are used for conducting the signal current $I_{dm,sig}$. This way, compared to using a simple active load [79], significantly lower current pulses can be applied in the first level shifting while maintaining its common-mode noise immunity. Concluding, with the introduction of a two-step level shifting, pulsed set/reset signaling as well as an active load with partial positive feedback, the level shifter circuit shown in Fig. 17 can deal with the design challenges for both HS and LS and thus identical circuits are used for both HS and LS level shifting.

3.5 Measurement results

The 80V power output stage has been fabricated in a 0.14µm SOI-based BCD process and the chip photograph is shown in Fig. 3.18. For the layout of the power stage, two bondpads are used for each of the V_{DDP}, V_{SSP} and V_{pwm} pins to ensure enough current handling capability. The top-metal layer connected to these power supply bondpads is triangular (as is evident in the chip photograph in Fig. 3.18) to realize a uniform current density, resulting in minimal metal resistance in the power transistors.

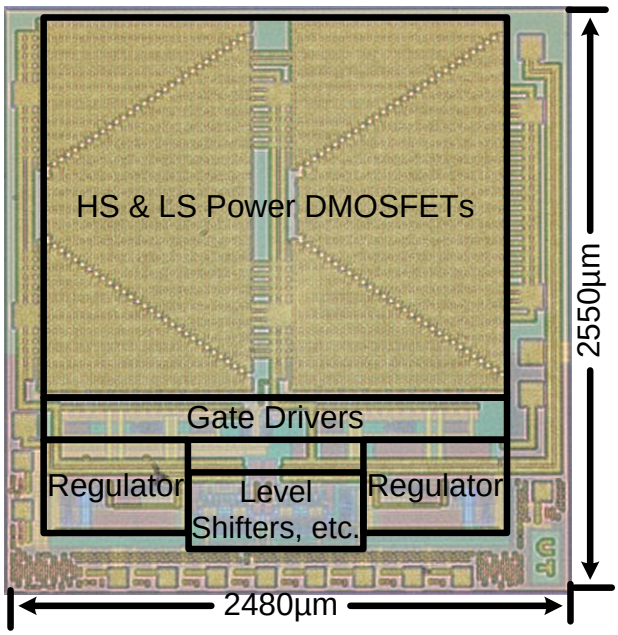


Fig. 3.18. Chip photograph of the 80V class-D power stage

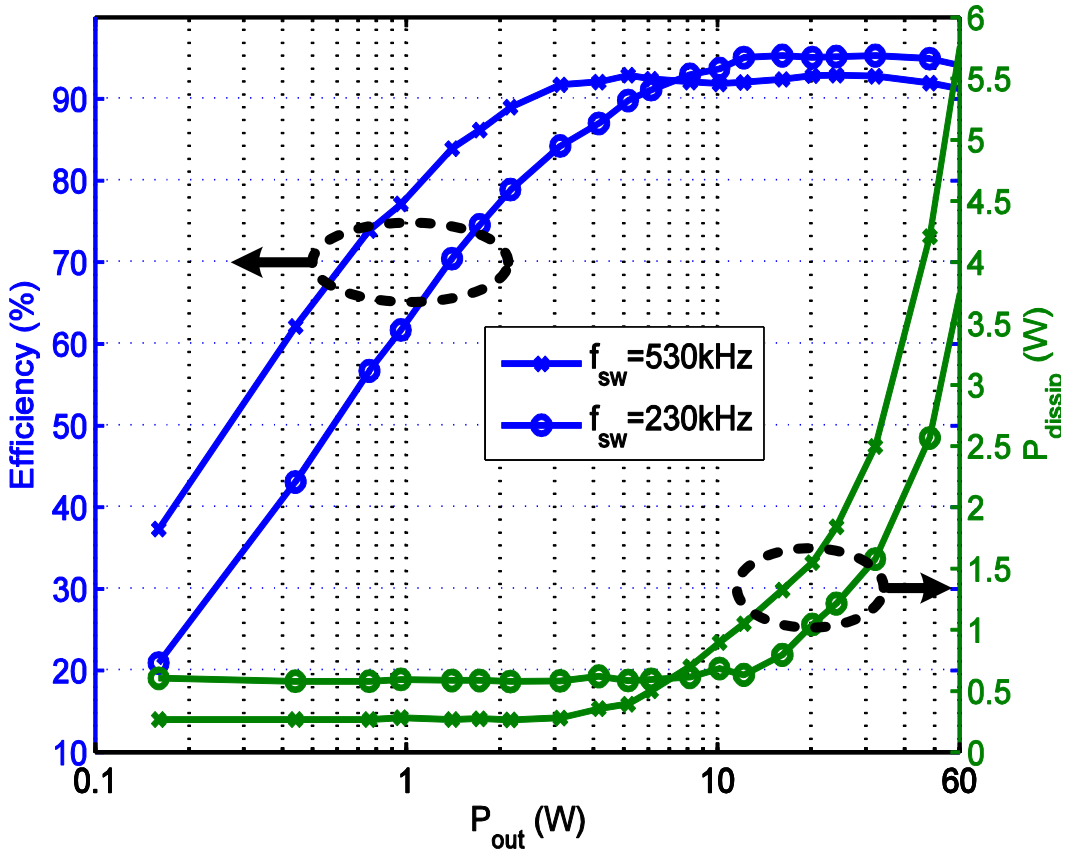


Fig. 3.19. Power efficiency and dissipation measurement results for 230kHz and 530kHz switching frequency, the measurement is with a DC electronic load for delivering real output power.

Packaged chips are used for all the measurements that follow, with external heat sinks attached to the package for thermal stability considerations. Off-chip decoupling capacitors are required for the decoupling of the following critical voltage domains: high-voltage power supply V_{DDP}/V_{SSP}, LS gate driver supply V_{DD}/V_{SSP}, HS gate driver bootstrapped supply V_{boot}/V_{pwm}. Minimum current loops [8] should be ensured in the PCB design for these decoupling loops as to minimize L_{par}. Two power supplies are required: the 12V gate-driver supply as well as the 80V high-voltage power supply.

For measuring efficiency, first a current-source load instead of the capacitive piezoelectric load is used to make the power stage delivering active output power. When the output voltage is fixed, the output power is varied by sweeping the output current value of the current-source load, and the output power is dissipated in this load. For a fixed output voltage of 40V (duty cycle of 0.5) and a switching frequency of 230kHz as well as 530kHz, the efficiency

measurement results are shown in Fig. 3.19. The measured peak efficiency for 230kHz switching frequency is 94%. For power efficiency measurements when driving capacitive piezoelectric load, a series-connected 23μF+1.6Ω is used to model the piezo-actuator [32] and this load is mostly capacitive at the input signal frequency f_{sig} of several tens to hundreds of Hz. Efficiency is defined here as

$$Eff = P_{out,app}/(P_{out,app}+P_d),$$

where $P_{out,app}$ is the apparent output power $V_{out,rms}*I_{out,rms}$ (VA) processed by the amplifier and P_d is the total amplifier dissipation. Even though there will be no real power delivered to the load for the purely capacitive load case, this expression for power efficiency (Eff) can still be used to characterize the power stage efficiency, since it is based on how much will be dissipated (P_d) when processing a certain amount of power ($P_{out,app}$). Fig. 3.20 shows the measurement results with a 500Hz signal applied on the load and maximum $P_{out,rms}$ of 45VA. The peak efficiency is 92% and 89% for switching frequency of 230kHz and 530kHz respectively. The current supplied by both the 12V and 80V supply are taken into account for all of these power efficiency measurements.

For measuring linearity, the power stage is operated within a hysteretic-based feedback loop [83]-[85]. For a 1st-order hysteretic-based loop [85] with the switching frequency set at 230kHz for D=0.5, Fig. 3.21 shows the THD+N performance when driving a series-connected 2.2μF+3Ω load. A THD+N of 0.03% is achieved for f_{sig}=1kHz, which is comparable to [85]. Compared with the case of f_{sig}=1kHz, THD+N level will increase for the f_{sig}=2kHz case. This is mainly because the output power is higher due to the capacitive load, and the loop gain of the feedback loop for suppressing the harmonics of the 2kHz signal is lower than the loop gain in the 1kHz case.

Compared to other power stage designs, this design offers the best possibilities for integration with other mixed-signal functions and especially digital circuitry thanks to the smaller process node being used, 0.14μm versus 0.25–3μm in [8]-[13]. This is permitted by the supply bounce immunity features, enabling its operation with a 3.3V V_{gs} other than 5-12V V_{gs} in [8]-[12] and 18V V_{gs}=V_{ds} in [13]. The >90% peak efficiency compares favorably with [8]-[13]. This is also ensured by the supply-bouncing immunity, as well as by the in-cycle variable gate drive strength.

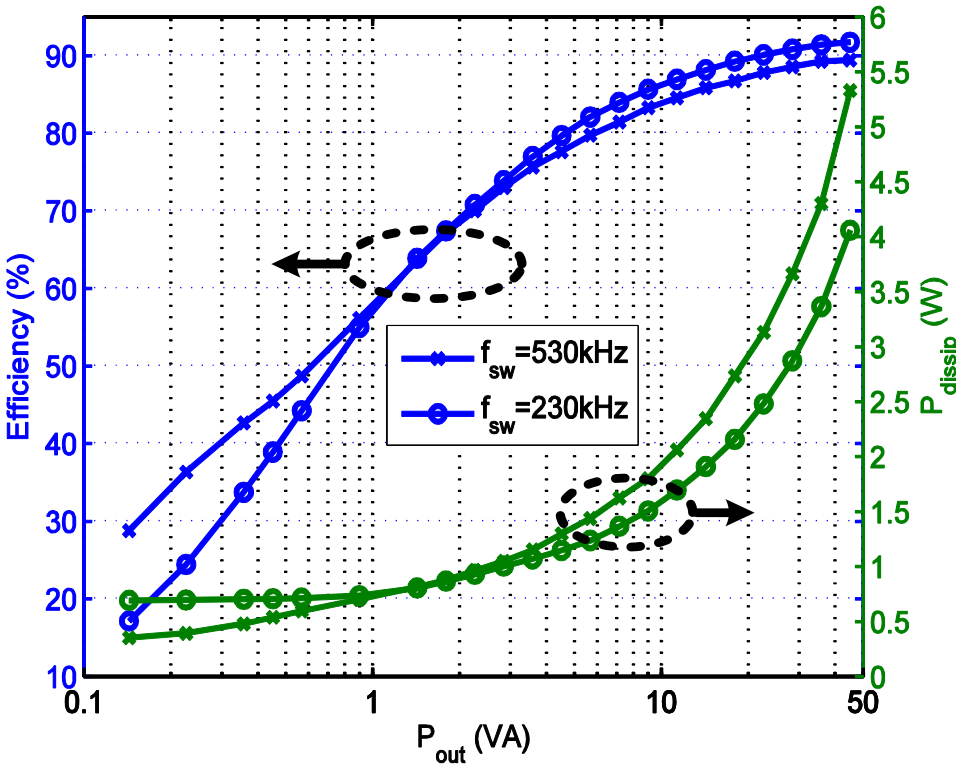


Fig. 3.20. Apparent power efficiency (see text) and dissipation measurement results for 230kHz and 530kHz switching frequency driving a series-connected 23µF capacitor and 1.6Ω resistor.

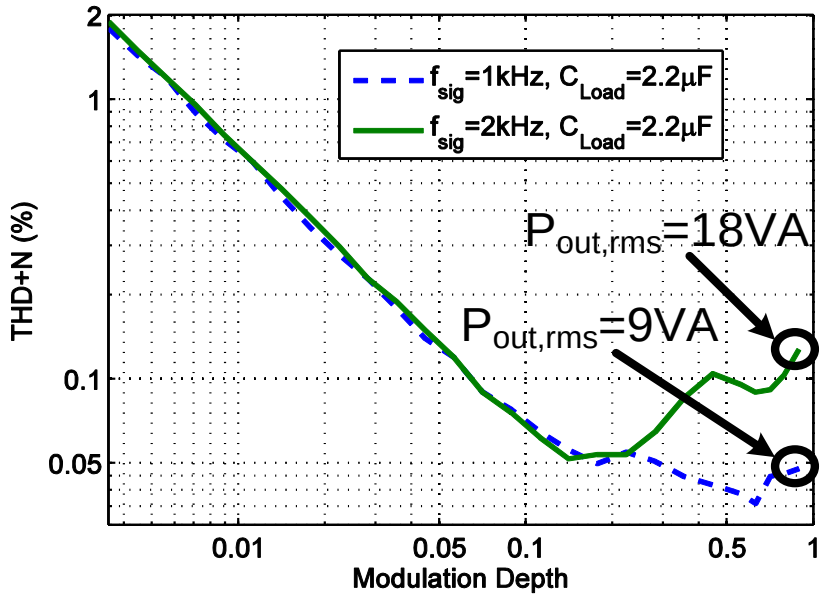


Fig. 3.21. Measured linearity performance of the class-D output stage within a 1st-order hysteretic feedback loop, with a series-connected 2.2µF+3Ω load.

3.6 Conclusions

Fast switching transitions are crucial for minimizing class-D switching losses. In this chapter the gate driver sizing issues considering the on-chip supply bounce are discussed in detail. It is shown that for traditional gate driver circuits both the pull-up and pull-down strength have to be limited to avoid excessive supply bounce and this in turn limits the realization of power-efficient fast switching transitions. The introduction of regulated floating supplies, variable driving strength for the gate driver and a 2-step level shifter ensure fast switching transitions not disturbed by on-chip supply bounce. A high-voltage, high-power class-D power stage with 3.3V V_{gs} is realized and measures with over 94% peak efficiency.

CHAPTER FOUR

4. Extending High-Efficiency Output Power Region – Switching Frequency Regulation

(Section 4.2 to section 4.5 are taken from part of the author's paper accepted to IEEE Journal of Solid-State Circuits in 2015 [88].)

4.1 Introduction

In section 2.5.2 it was observed that when varying the switching frequency, a minimum power dissipation point exists that depends on the output power. (Fig. 2.9(a) and Fig. 2.9(b)). We would like the amplifier to operate at this minimum dissipation point for both high and low power, because considering the relatively high peak-to-average ratio of audio signals [6], the average output power level that the amplifier is typically operating at can be orders of magnitude lower than the maximum output power. Consequently this necessitates the optimization of class-D efficiency across orders of magnitude output power range.

The common approach to optimize power efficiency across a certain output power range, is to choose the output transistor size [34] or the switching frequency, f_{sw} [9] for a tradeoff between low- and high-power efficiency. Fixing the transistor size and the switching frequency results in either the low- or high-power efficiency being suboptimal. Adaptive techniques for changing the power transistor size [22] or the switching frequency [44],[46] have already been proposed for further efficiency enhancement. However, the dynamic

power stage activation in [22] is not suitable for high-voltage applications. This is because the parasitic capacitance at the output node of the power stage is still present for the inactive part of the power stage, resulting in the same high switching loss. Varying the switching frequency according to the output current only [44],[46] is also suboptimal since the actual power dissipation mechanisms are highly dependent on other circuit operating conditions such as the output inductor ripple current, as will be explained in the following section.

In this chapter we propose a switching frequency regulation technique that always maintains minimal power dissipation from idle to maximum output power [83]. This is achieved by detecting the output switching node voltage level at the turn-on transition of the power switches. This information is directly related to the dissipation sources and is inherent for getting to the optimal switching frequency and in turn the minimal dissipation, independent of circuit operating conditions affecting the output inductor ripple current. The proposed switching frequency regulation for efficiency improvement is described in section 4.2. In section 4.3, the overall topology and circuit blocks for the class-D power amplifier are described. Section 4.4 discusses the measurement results and in section 4.5 the conclusions are drawn.

4.2 Efficiency Improvement with Switching Frequency Regulation

4.2.1 Dissipation Sources versus Switching Frequency

In chapter 2 we have already developed a class-D dissipation model that can adequately predict the power stage dissipation crossing different output regions and covering the three major types of switching dynamics (HSw, SSw and PSSw). Following this analytical loss model, the total dissipation P_{total} and each of its contributing sources can be analyzed under different load conditions with varying f_{sw}. This way we can identify the dominating dissipation source for a specific output power level and subsequently find methods for adapting the switching frequency to minimize the contribution of this dominating dissipation source. To form a general analysis of the output stage dissipation, we first exclude the magnetic core loss of the output inductor, i.e. assuming $P_{Irip,core}$ as in (2.5) = 0. The core loss is highly dependent on the type and size of the chosen inductor, and its effect will be added separately in the next section.

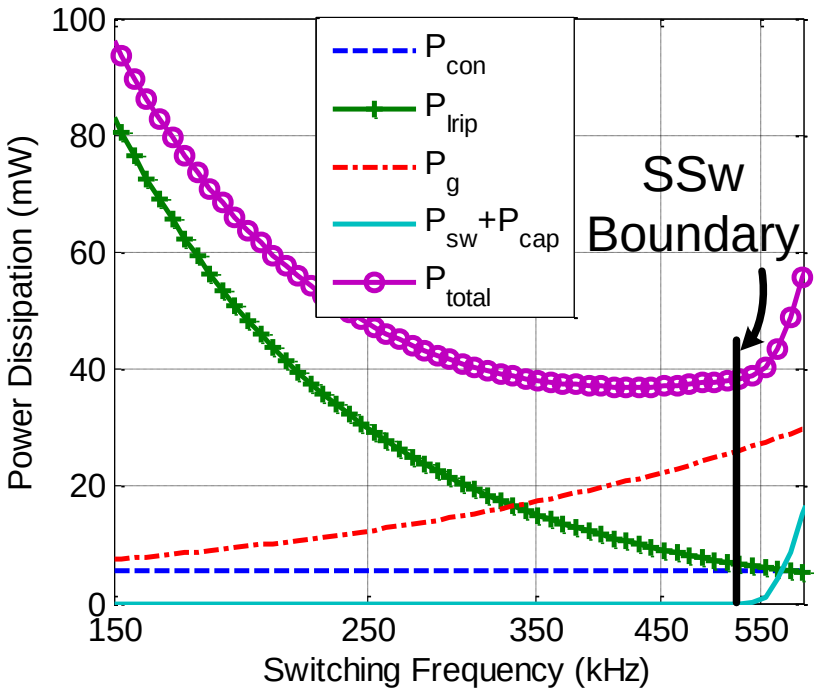


Fig. 4.1. Modeled contribution of each dissipation source with varying switching frequency at low output power. P_{Irip} is the dominating dissipation source at low switching frequency. Its contribution can be minimized by moving to higher f_{sw} where P_g and $P_{sw}+P_{cap}$ are not yet significant (I_{out}=100mA, D=0.5).

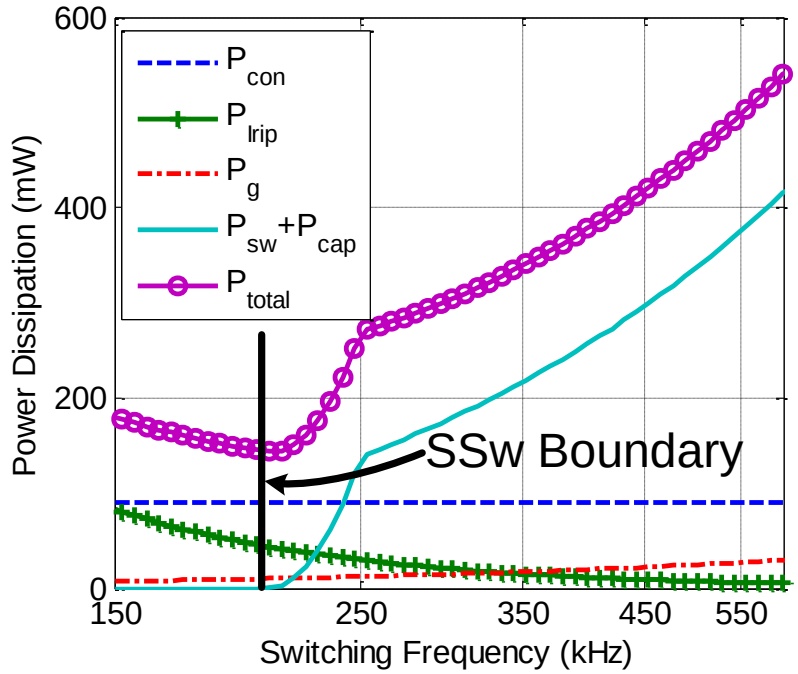


Fig. 4.2. Modeled contribution of each dissipation source with varying switching frequency at medium output power (I_{out}=400mA, D=0.5).

Fig. 4.1 shows the contributing dissipation sources for a low output power level (I_{out}=100mA, D=0.5). As we can see from Fig. 4.1, because P_{Irip} is the dominating loss for the lower f_{sw} region, P_{total} can be significantly decreased with increasing f_{sw}. This trend continues until the gate driver loss P_g becomes comparable with that of P_{Irip} and counteracts the decreasing P_{Irip}. Consequently P_{total} flattens out for higher frequencies.. Further increasing f_{sw} across the SSw boundary causes P_{sw}+P_{cap} to rise significantly due to the high V_{DDP} and thus is not desirable.

With the output power increased to a medium level as shown in Fig. 4.2 (I_{out}=400mA, D=0.5), the same trend can be seen with P_{total} decreasing together with P_{Irip} for increased f_{sw}. The SSw boundary is shifted to a lower f_{sw} here because the necessary I_{rip} to achieve SSw has increased due to the higher I_{out}. Also because of this lower f_{sw} for achieving SSw, P_g is insignificant compared to the other losses and the immediate increase in P_{sw}+P_{cap} becomes the main dissipation source at higher f_{sw}. As can also be seen in Fig. 4.2, minimum P_{total} is at a frequency slightly higher than the SSw boundary. This is because the decrease in P_{Irip} has a stronger effect than the increase in P_{sw}+P_{cap} in the PSSw region. Yet the decrease is insignificant, considering the constant P_{con} that constitutes the larger part of P_{total}.

When the output power further increases as shown in Fig. 4.3 (I_{out}=800mA, D=0.5), SSw cannot be achieved within the f_{sw} range. Also, due to the high V_{DDP}, P_{sw}+P_{cap} increase significantly with increasing f_{sw}. This makes the P_{Irip} contribution not important and thus increasing f_{sw} is not beneficial. In this case the class-D amplifier should operate with the lowest possible f_{sw}, as can be seen in Fig. 4.3.

The analysis made above can be summarized into two points, 1) When soft switching is possible, increasing f_{sw} till the SSw boundary is beneficial to lower P_{Irip} and in turn P_{total}.. Dissipation at that frequency is close to minimal. 2) When SSw cannot be realized, minimum P_{total} is achieved at the lowest f_{sw}, where P_{SW}+P_{cap} is the lowest. Based on these two points, achieving minimum dissipation across the full output power range means the class-D switching transitions should be at the SSw boundary whenever possible. With SSw conditions highly dependent on both I_{out} and I_{rip}, and I_{rip} influenced by numerous factors (e.g. > 5× variation in the 0.05-0.95 duty cycle range), an intelligent way to regulate f_{sw} to the SSw boundary is required.

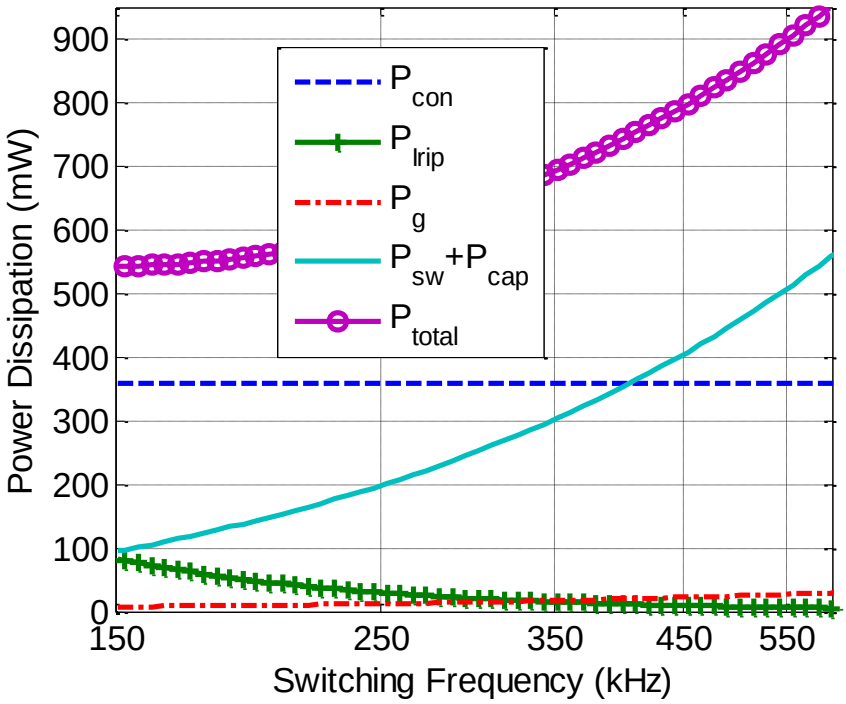


Fig. 4.3. Modeled contribution of each dissipation source with varying switching frequency at high output power(I_{out}=800mA, D=0.5).

4.2.2 Output Inductor Loss Considerations

In the analysis made above, only the power loss from the output power transistors was considered. Yet the magnetic core loss of the output inductor can also be a significant contributor to the total loss, especially when the inductor has to be compact. We take a Coilcraft MSS1278T 100µH power inductor [86] as an example here (It has a saturation current of 3.12A for 10% drop in L value, 12mm*12mm*7.8mm in volume). Based on power loss data from [72], inductor core loss contribution is considered, by adding $r_{eq}=0.9\Omega \cdot f_{sw}/100kHz$ to P_{lrip}. Fig. 4.4 shows the power dissipation versus f_{sw} trend for the same load condition as in Fig. 4.2 (I_{out}=400mA, D=0.5). Compared with Fig. 4.2, P_{lrip} takes up a higher portion of the total loss. Even though total dissipation has practically doubled by including core loss, minimum dissipation is achieved at only a slightly higher f_{sw}. Therefore it can be concluded that by properly choosing output inductors whose core loss are not completely dominating in P_{total}, operation on the SSw boundary leads to dissipation very close to minimum. This is the basis of the proposed frequency regulation technique.

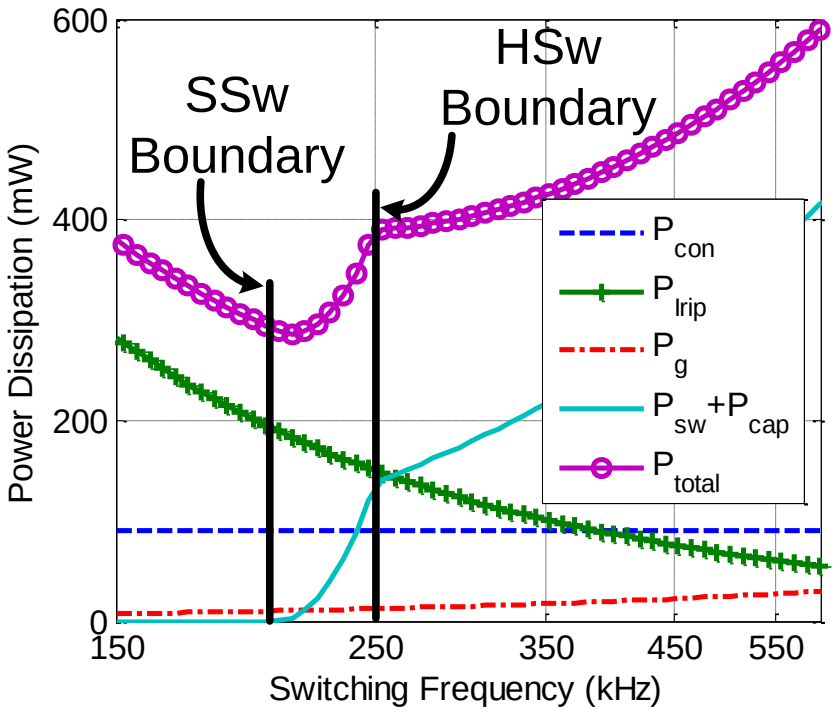


Fig. 4.4. Modeled total power dissipation with varying f_{sw} when output power inductor loss is included (I_{out}=400mA, D=0.5).

4.2.3 Switching Frequency Regulation

To achieve minimum dissipation the amplifier has to be kept at the soft switching boundary, but as explained in section II, this point depends heavily on circuit parameters and operating point. However, the V_{pwm} level at the rising edges of V_{HS}/V_{LS} can be used to indicate if the amplifier is soft switching. The working principle is shown in Fig. 4.5. Fig. 4.5(a) shows the SSw waveforms, with I_{rip} larger than necessary (excessive P_{Irip}) for eliminating $P_{sw}+P_{cap}$. Both V_{pwm} transitions finish within the dead time t_d and are already at the other supply rail when M_{HS}/M_{LS} turns on. This means I_{rip} (and consequently P_{Irip}) could be smaller by increasing f_{sw}. On the other hand, for the PSSw case shown in Fig. 4.5(b), I_L is too small to charge C_{par} during t_d, and the remaining V_{pwm} rising transition is accomplished by M_{HS}. V_{pwm} is not yet at V_{DDP} when M_{HS} turns on, indicating the existence of P_{cap} and f_{sw} should decrease.

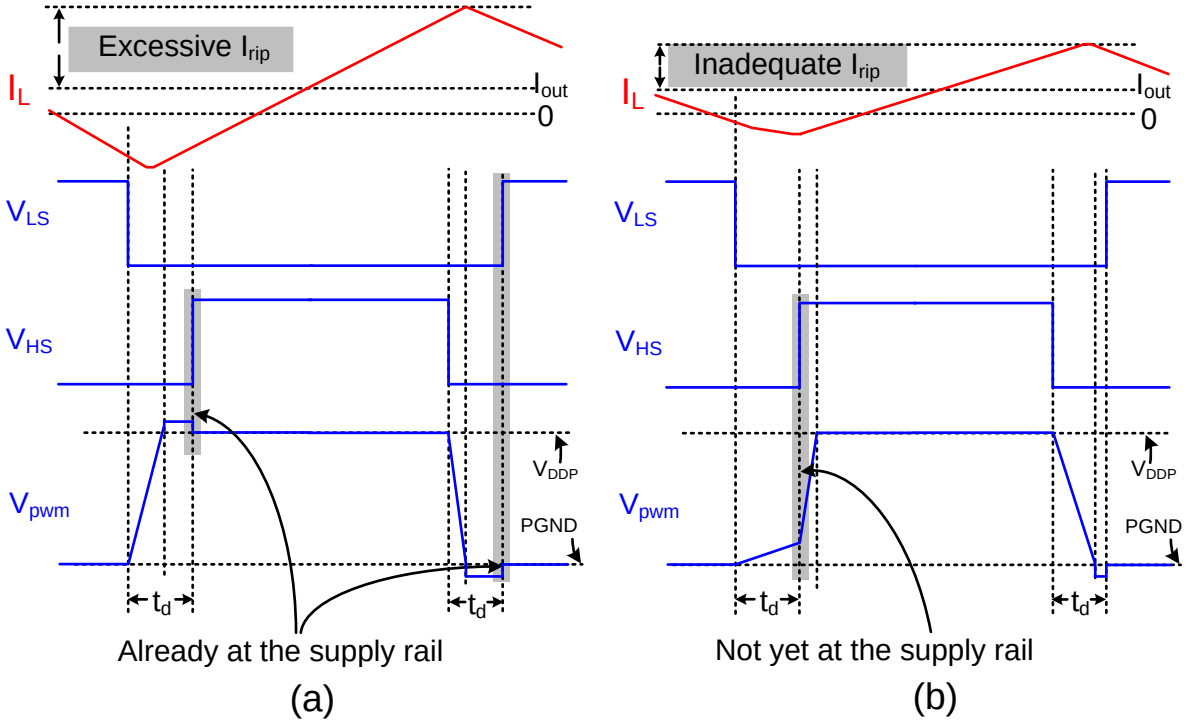


Fig. 4.5. Using V_{pwm} level information at the rising edge of V_{HS}/V_{LS} to indicate whether the switching frequency is at the point for reaching minimum dissipation (a) Excessive P_{Irip}, f_{sw} should be increased (b) P_{cap} exists, f_{sw} should be decreased

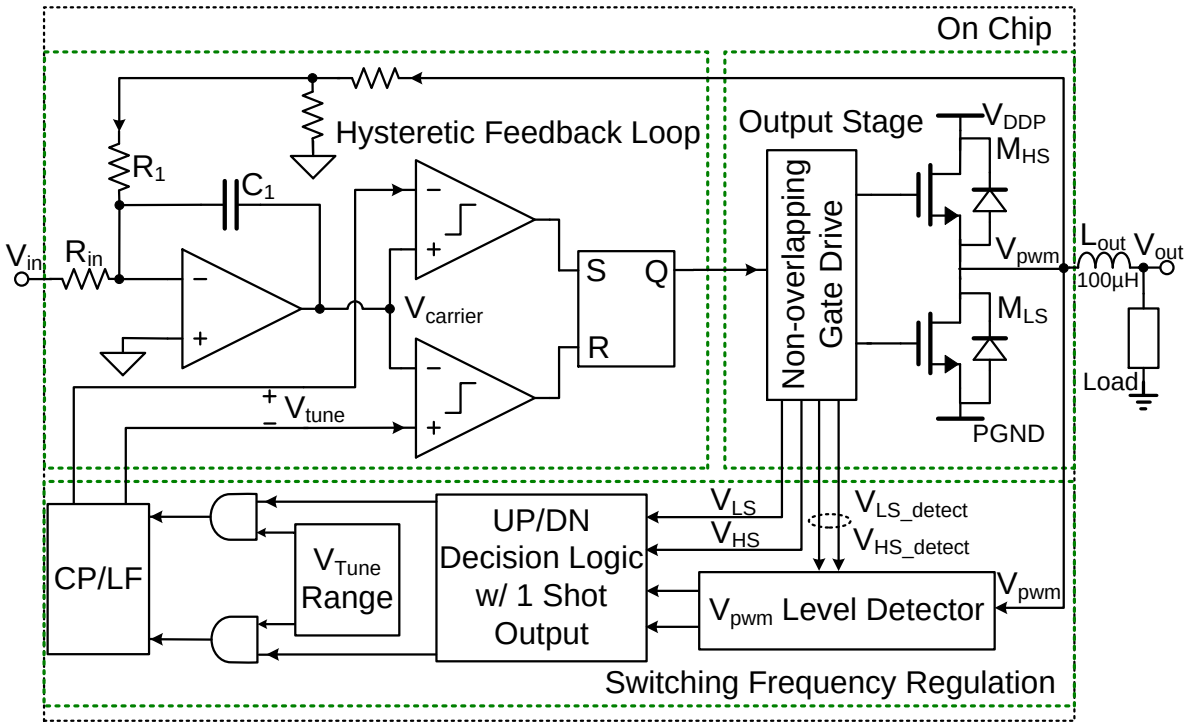


Fig. 4.6. Topology overview of the class-D amplifier with f_{sw} regulation.

Based on this analysis, the optimal-efficiency-tracking f_{sw} adaptation can be based on the following two cases: 1) When during both transitions V_{pwm} reaches the supply rail before the corresponding V_{HS}/V_{LS} rising edge, a higher f_{sw} should be aimed for. 2) When for either transition, V_{HS} or V_{LS} rises before V_{pwm} reaches the supply rail, a lower f_{sw} should be adopted. By adapting f_{sw} such that either one of the V_{pwm} switching is at the SSw boundary while the other is fully lossless, minimization of both $P_{sw}+P_{cap}$ and P_{Irip} is achieved. By further setting a f_{sw} higher limit, the system naturally shifts to hard switching at high output power, with minimized $P_{sw}+P_{cap}$.

4.3 Circuit implementation

4.3.1 Overall topology

The implementation of the amplifier is shown in Fig. 4.6. In this realization, the amplifier is based on a 1st-order hysteretic self-oscillating loop [83], [85]. Alternative implementations can also use carrier-based topologies [1], by changing f_{sw} of the triangle carrier, either continuously or through a frequency plan to control the spectral content. f_{sw} is controlled by the hysteretic window voltage $V_{tune.}$ The power output stage is identical to the one presented in Chapter 3, works with 80V V_{DDP}, an on-chip regulated 3.3V driver supply and has a 2-step level shifter that can handle supply bounce higher than the internal supply [29].

4.3.2 Circuits

Fig. 4.7 shows the V_{pwm} level detection circuit. At the beginning of a transition, when V_{pwm} is far (up to 80V) from the supply rail, M_{LSC}/M_{HSC} shield the clamps M_{LSD}/M_{HSD} from V_{pwm}. When V_{pwm} is close to the supply rail, M_{LSC}/M_{HSC} are in the linear region, such that M_1/M_4 can detect if V_{pwm} is close (less than a V_{TH}) to the supply rail. Control signals $V_{LS\_detect}/V_{HS\_detect}$ are generated in the output stage with their rising edges time shifted compared to V_{LS}/V_{HS} such that they only activate M_{LSC}/M_{HSC} for half the switching cycle to prevent cross current flow from the supply. For proper control of M_{LSC} and M_{HSC}, $V_{LS\_detect}/V_{HS\_detect}$ are referred to PGND and V_{pwm} respectively with additional level shifter circuits. M_4 level shifts to logic levels referred to V_{SSD}. M_1-M_3 level shift in 2 steps to deal with the large (> 3.3V) on-chip PGND bounce.

Fig. 4.8 shows the UP/DN decision logic. The V_{pwm} status is sampled at the rising edge of V_{HS}/V_{LS} for switching noise immunity. The 1 shot for an f_{sw} increase is activated if both V_{pwm} transitions are finished in time while the 1 shot for an f_{sw} decrease is activated if either transition is not.

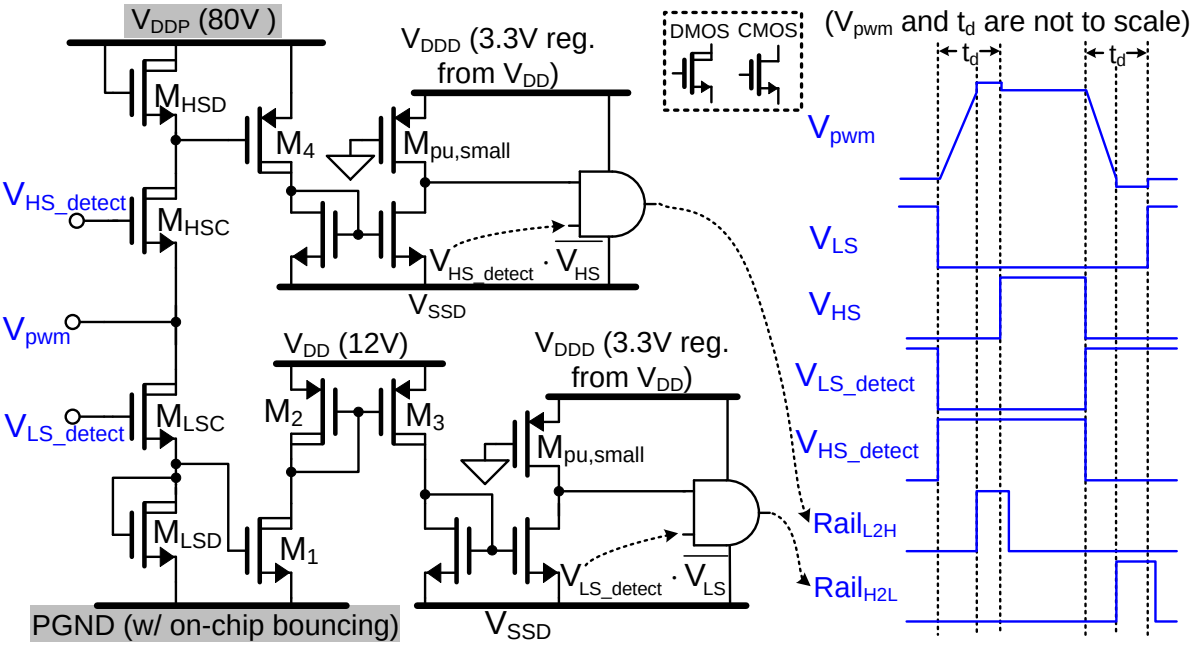


Fig. 4.7. V_{pwm} level detection circuit

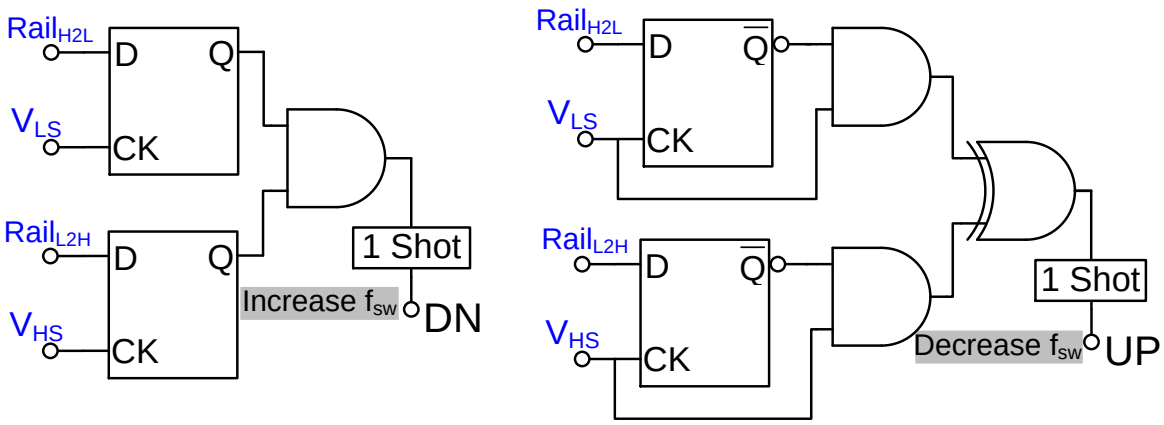


Fig. 4.8. UP/DN decision logic

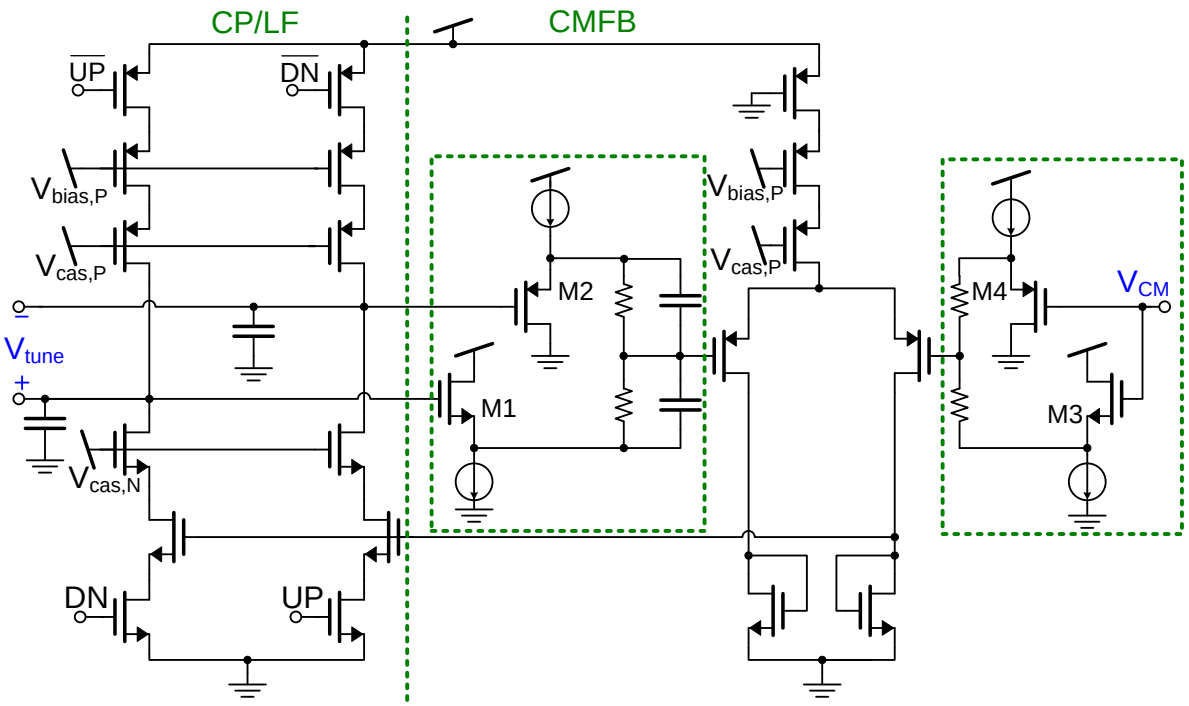


Fig. 4.9. Charge pump/loop filter circuit used for the V_{tune} generation.

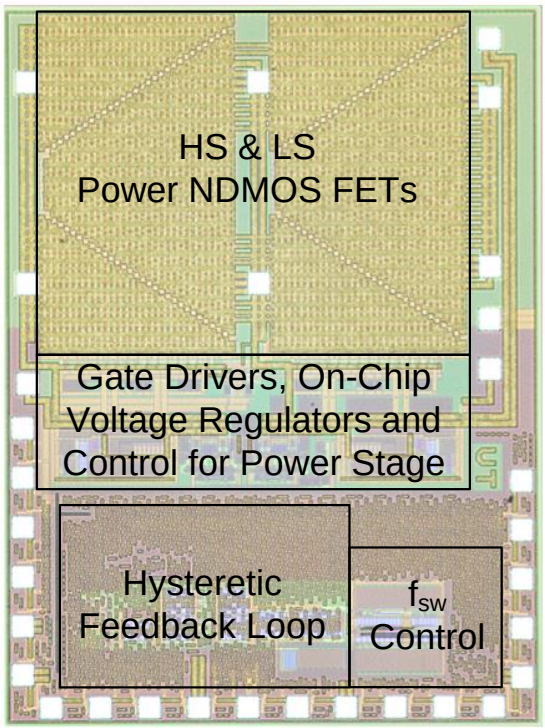


Fig. 4.10. Chip photograph of the class-D amplifier, the die measures 3.4mm×2.5mm.

Fig. 4.9 shows the charge pump/loop filter circuit for the fully-differential V_{tune} generation. Since V_{tune} is at 2× the signal frequency f_{sig} (when I_{out} increases in either direction), V_{tune} generation is fully differential for minimal 2nd-order distortion. For realizing a wide f_{sw} tuning range, V_{tune} is required to be able to operate near the supply rails. To facilitate this, complementary buffers (M1 and M2) are used to measure the common-mode voltage of $V_{tune,p}$ and $V_{tune,n}$. Corresponding replica buffers (M3 and M4) are applied to the common-mode reference voltage V_{CM}.

4.4 Measurement results

The amplifier is implemented in a 0.14µm SOI-based BCD process. The chip photograph is shown in Fig. 4.10, with the die measuring 3.4mm×2.5mm. For the layout of the amplifier, the power stage and the control blocks (f_{sw} control and hysteretic feedback loop) are separated, to avoid the high switching noise associated with the power stage [29] to interfere with the signal path. For chip packaging, the same design considerations apply, with the noisy power stage pins (V_{DDP}, PGND, V_{pwm}, gate driver V_{DD}) placed at one side of the packaged chip and the pins for the control blocks at the other side. For the measurement PCB design, current switching loops [1] are ensured to not overlap with the signal path, as to minimize noise coupling to the signal.

For power efficiency measurements, a series-connected 23µF + 1.6Ω is used to model the piezo-actuator [31]. Because this load is mostly capacitive at f_{sig}, efficiency is defined here as $P_{out}/(P_{out}+P_d)$, where P_{out} is the apparent output power $V_{out,\,rms}$*$I_{out,rms}$ (VA) processed by the amplifier and P_d is the total amplifier dissipation. For the total amplifier dissipation P_d, both the power stage (the power inductor included) and control circuits dissipation are taken into account. Fig. 4.11 shows the measured efficiency of the amplifier for a 500Hz sine wave for three fixed V_{tune} settings and one with f_{sw}-regulation enabled at 80V V_{DDP}. The inductor used for the dissipation measurement is a Murata 1410478C 100µH power inductor with saturation current of 7.8A. The control blocks used an external 12V V_{DD} and the power stage used an external 80V $V_{DDP.}$ Current drawn from both V_{DD} and V_{DDP} supplies are included in the P_d. Fig. 4.11 clearly shows that the amplifier can adjust its f_{sw} for best efficiency across the whole output power range. Idle power consumption is 360mW while for the two lower f_{sw} cases it is 440mW and 690mW, achieving a reduction of 18% and 48%. The peak efficiency of the amplifier is 93% while for the two higher f_{sw} cases it is 91% and 89%, achieving a power loss

reduction of 19% and 31%. In idle, the adaptive f_{sw} is 500kHz while for 45VA output power, the adaptive f_{sw} is from 200kHz at D=0.5 to 100kHz at D=0.05 or 0.95.

THD+N is below 1.3% over the full output power range at 80V V_{DDP} with the series-connected 23µF + 1.6Ω load when adaptive f_{sw} is enabled (Fig. 4.12). However, at 80V V_{DDP}, the substrate starts to act as a back gate for the high side power switch and drivers in this SOI process, influencing the gate drive strength and muddling the THD+N plots. Therefore THD+N is also shown in Fig. 4.13 with 60V V_{DDP} where the trend is much clearer.

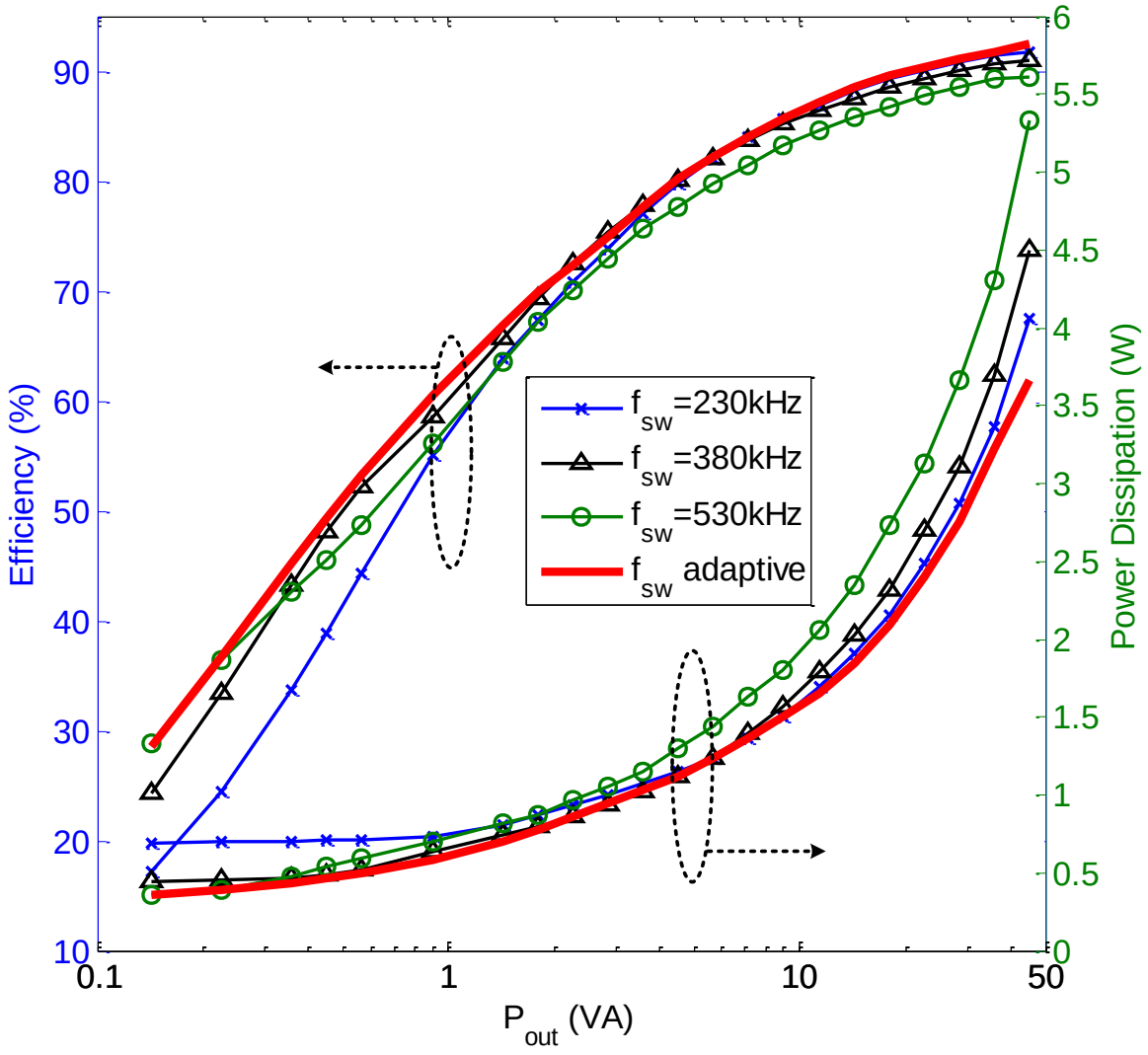


Fig. 4.11. Efficiency and dissipation measurements with 80V V_{DDP}, for f_{sw} regulation enabled as well as for fixed V_{tune} settings. For the fixed V_{tune} cases, f_{sw} is measured in idle.

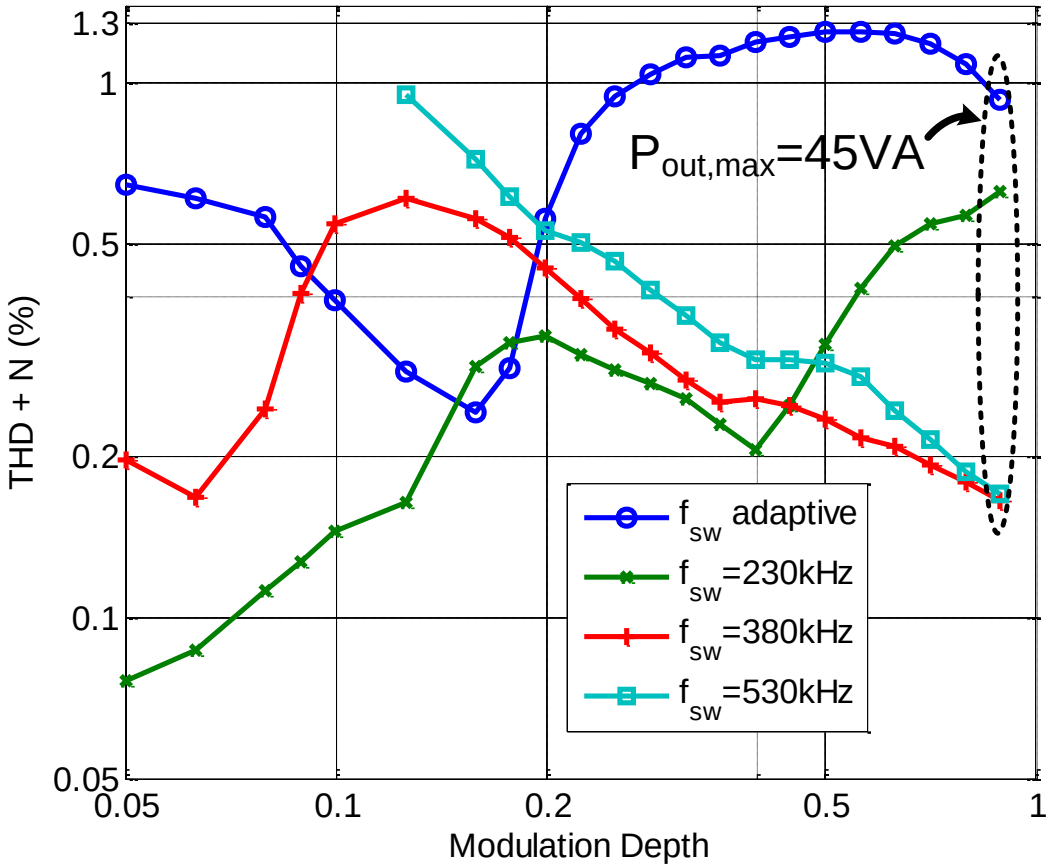


Fig. 4.12. THD+N measurement results with the series-connected 23µF + 1.6Ω load, f_{sig} = 500Hz , V_{DDP} = 80V, for f_{sw} regulation enabled as well as for fixed V_{tune} settings. For the fixed V_{tune} cases, f_{sw} is measured in idle.

The trend for the THD+N performance can be explained as follows: 1) For the low output power regions, i.e. modulation depth M up to 0.05, THD+N is inversely proportional to f_{sw} (see section 5.2). When adaptive f_{sw} is enabled, f_{sw} is regulated to the highest possible value, thus resulting in the largest THD+N. 2) When output power is increased, the ripple will constitute a smaller part of the load current. And since the output node is charged by I_{out}-I_{rip} and discharged by I_{out}+I_{rip}, the switching waveform becomes increasingly asymmetric at higher output powers [48] until it enters hard switching, where the full dead time shows up as distortion. For fixed low switching frequencies the ripple is high, so the distortion increase happens at larger output powers. For the f_{sw} regulated case, the amplifier is kept borderline soft switching, always producing higher distortion. 3) For the high output power regions (M > 0.2), THD+N for the three fixed V_{tune} settings remain similar. The main reason is that the relative distortion introduced by the power switches' turn-on delay for V_{pwm} HSw transitions

[48] is proportional to f_{sw}, while the loop gain for suppressing this error is also proportional to f_{sw} [74]. It remains unclear why the f_{sw} regulated case has higher distortion than the fixed frequency cases. A varying common-mode level of V_{tune} level might be one of the contributing factors. For applications that require lower distortion, a higher-order feedback loop can be used, either for hysteretic feedback [49] or fixed carrier [50], [51] topologies.

A comparison with other high-voltage, high-power class-D designs is shown in TABLE VI. For better comparison, efficiency with a non-capacitive load (12Ω resistor) is also measured. The V_{pwm}-level-based f_{sw}-regulation technique enables this design to achieve best-in-class peak efficiency while significantly outperforming the other amplifiers at lower output powers.

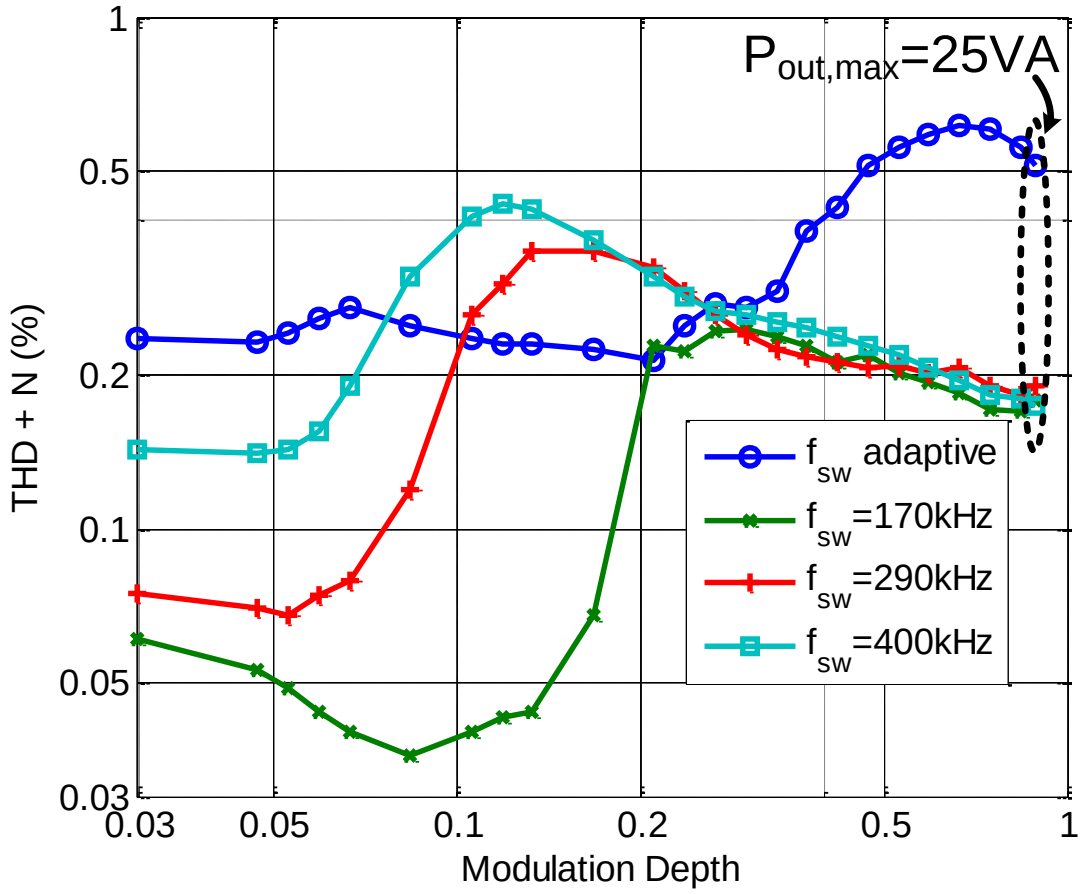


Fig. 4.13. THD+N measurement results with the series-connected 23µF + 1.6Ω load, f_{sig} = 500Hz , V_{DDP} = 60V, for f_{sw} regulation enabled as well as for fixed V_{tune} settings. For the fixed V_{tune} cases, f_{sw} is measured in idle

TABLE VI. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER HIGH-VOLTAGE, HIGH-POWER CLASS-D AMPLIFIERS

Parameters	This work		[1]	[9]	[10]	[13]
Type	Piezo Driver		Audio Amp.	Audio Amp.	Audio Amp.	Audio Amp.
V_{DDP}	80V		60V	20V	50V	18V
$P_{out,max}$/Channel	45VA(1)	45W(2)	100W	20W	240W	13W
Efficiency @ $P_{out,max}$	93%	91%	>90%	89%	N/A	88%
Efficiency @ 0.1* $P_{out,max}$	80%	84%	N/A	<75%	N/A	<70%
Efficiency @ 0.01* $P_{out,max}$	49%	51%	N/A	<30%	N/A	<30%
Idle Loss/Channel (w. output filter)	0.36W		1.6W	0.5W	2.1W	N/A
THD+N	0.015% (@9VA, f_{sig}=100Hz) 0.94% (@45VA, f_{sig}=500Hz)		0.017% (@1W, f_{sig}=1kHz)	0.01% (@10W, f_{sig}=1kHz)	<0.1%	0.7% (@13W, f_{sig}=1kHz)

(1) Load = 23μF+1.6Ω in series
(2) Load = 12Ω

4.5 Conclusions

For high-voltage class-D amplifiers, different dominating power loss mechanisms exist with changing output power level. Simultaneous reduction of the inductor ripple current induced loss and the switching-induced loss across the full output power range can be achieved with an optimal-efficiency-tracking switching frequency regulation loop. This is realized by detecting the output switching node voltage level at the turn-on transition of the power switches. The designed amplifier offers the high peak efficiency of existing class-D designs, keeping heat sinks small, while offering significant energy savings at lower, much more prevalent, output powers.

CHAPTER FIVE

5. Improving Efficiency at Idle/Low Output Power – Dead Time Insertion

5.1 Introduction

We have shown in section 2.5.3 that the insertion of a larger dead time can achieve less idle dissipation in a class-D power stage (Fig. 2.10). This is by taking advantage of the lossless soft switching operation where switching loss P_{sw} is fully eliminated, while reducing ripple current induced loss P_{Irip} at higher switching frequencies. However, this configuration will result in degraded linearity performance, as already shown in the experimental results for the f_{sw}-regulated class-D power stage design in section 4.4 (Fig. 4.13). This chapter will focus on exploring methods for improving the linearity performance while keeping the same high power efficiency performance with dead time insertion. This chapter is organized as follows: section 5.2 analyzes power stage output error in relation to f_{sw} for SSw operation. Methods for correcting the open-loop power stage output error are discussed in section 5.3. Section 5.4 presents a discussion on choosing an optimal class-D feedback loop which introduces minimum error itself while simultaneously providing high loop gain for closed-loop power stage error correction. In section 5.5 conclusions are drawn.

5.2 Power stage output error in SSw operation

For low output powers where $I_{out}<<I_{rip}$ and the two V_{pwm} switching transitions are both SSw (Fig. 5.1), the inductor current I_L at the moment of a V_{pwm} low-to-high transition is I_{out}-I_{rip} while at the moment of a V_{pwm} high-to-low transition it is I_{out}+I_{rip}. Suppose the parasitic

capacitance C_{par} at V_{pwm} is linear, then the V_{pwm} low-to-high transition time t_{LH} and the V_{pwm} high-to-low transition time t_{HL} can be expressed as,

$$t_{LH}=C_{par}V_{DDP}/(I_{rip}-I_{out}) \quad (5.1)$$

$$t_{HL}=C_{par}V_{DDP}/(I_{rip}+I_{out}) \quad (5.2)$$

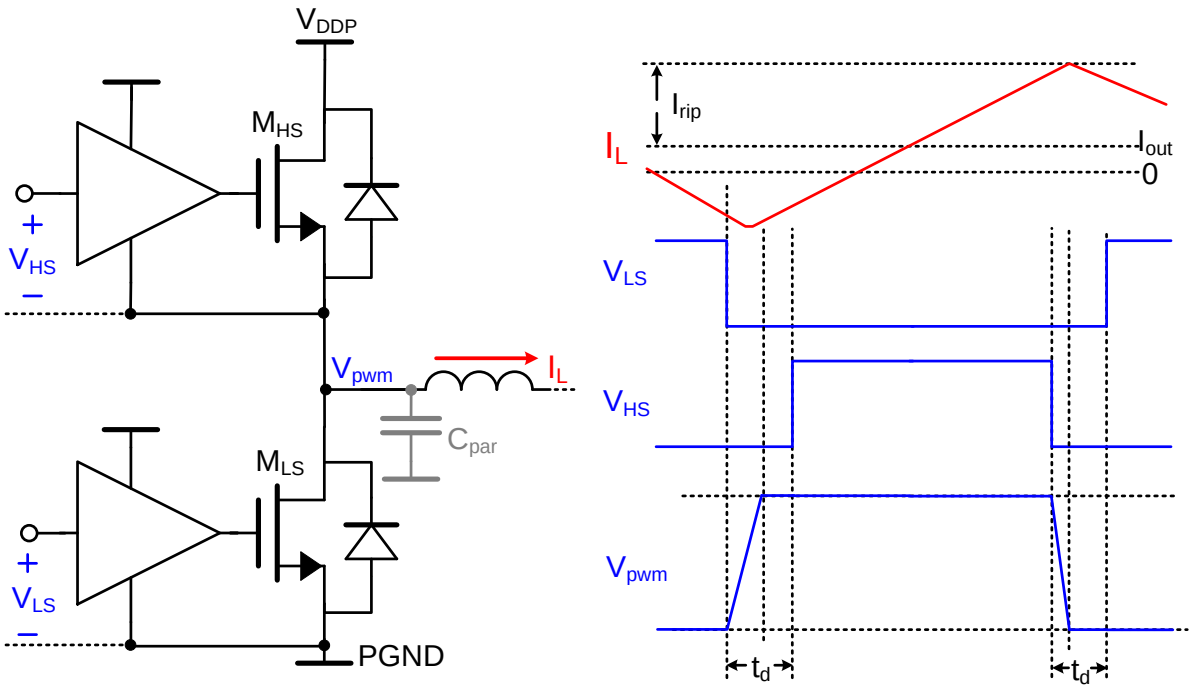


Fig. 5.1. Under low output power, the power stage switching transitions are both SSw.

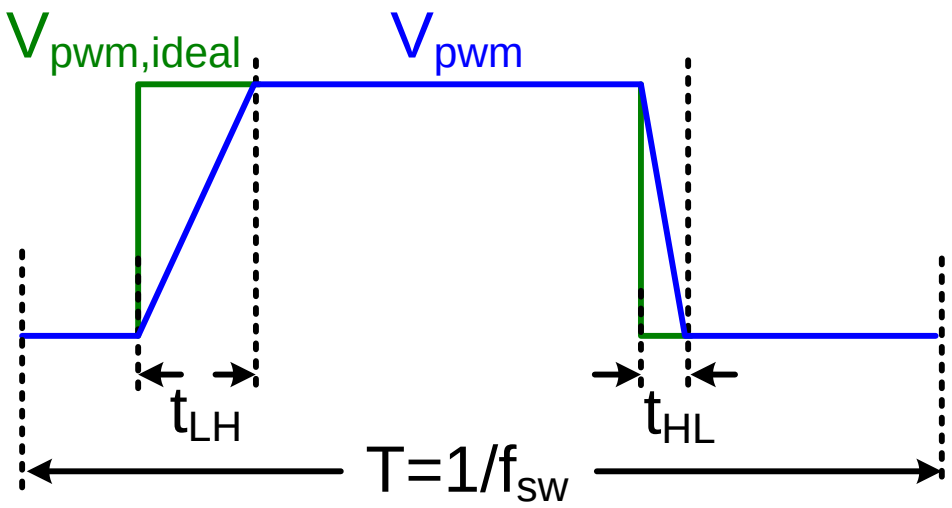


Fig. 5.2. Illustration of open-loop output stage V_{pwm} error when both V_{pwm} transitions are SSw.

Due to this unsymmetrical t_{LH} and t_{HL}, the V_{pwm} output has an error voltage compared to the ideal case as shown in Fig. 5.2. Within one switching cycle $T=1/f_{sw}$, the error voltage caused by t_{LH} and t_{HL} can be expressed as,

$$V_{e,LH}=-0.5V_{DDP}f_{sw}t_{LH} \tag{5.3}$$

$$V_{e,HL}=0.5V_{DDP}f_{sw}t_{HL} \tag{5.4}$$

Combing (5.1)-(5.4), the final error voltage V_e then will be,

$$V_e=-C_{par}V_{DDP}^2f_{sw}I_{out}/(I_{rip}^2-I_{out}^2) \tag{5.5}$$

With $I_{out}<<I_{rip}$, (5.5) can be further simplified to,

$$V_e\approx-C_{par}V_{DDP}^2f_{sw}I_{out}/I_{rip}^2 \tag{5.6}$$

By further inserting the I_{rip} expression from (2.1),

$$V_e\approx 4L_{out}^2C_{par}I_{out}f_{sw}^3/\left[D^2(1-D)^2\right] \tag{5.7}$$

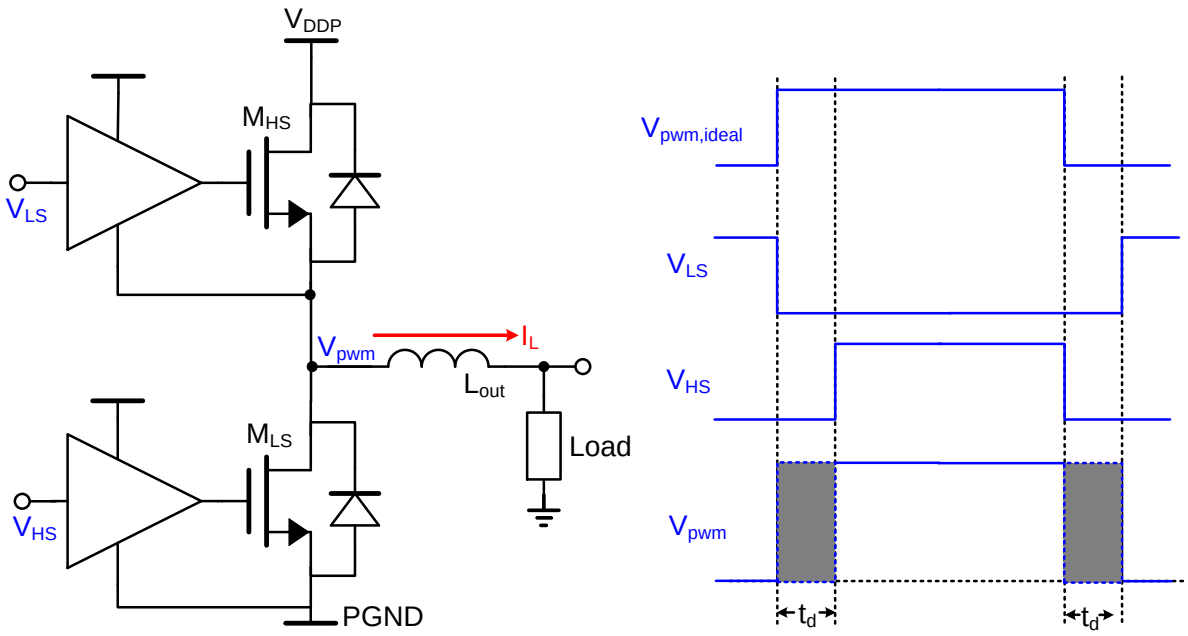


Fig. 5.3. The output V_{pwm} error mainly exists during the dead time, for both HSw and SSw transitions

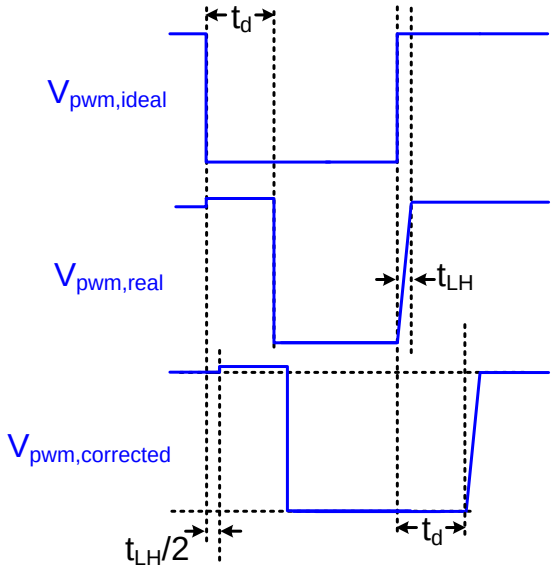


Fig. 5.4. Illustration of V_{pwm} error when both HSw and SSw are present and methods to correct the error. Here the high-to-low transition is HSw and the low-to-high transition is SSw.

As we can see from (5.7), V_e is proportional to f_{sw}^3 for the open-loop power stage V_{pwm} output. Considering that an ideal 1st-order hysteretic-feedback based loop has a loop gain proportional to f_{sw}^2 [74], the final closed-loop output error for a 1st-order hysteretic-feedback based class-D amplifier will be proportional to f_{sw} for low output power, as shown in the experimental result of Fig. 4.13 .

5.3 Output stage error correction

For both HSw and SSw transitions, the output V_{pwm} errors are present within the dead time (Fig. 5.3). Fig. 5.4 shows PWM waveforms in a complete switching cycle with one transition being HSw and the other SSw. Compared to the ideal waveform $V_{pwm,ideal}$, the high-to-low HSw transition only happens after the dead time is finished, which results in an increased pulse width of the real PWM output. For the low-to-high $V_{pwm,real}$ SSw transition, finite slew rate, which is dependent on the inductor current amplitude, also results in certain amount of error voltage, as being analyzed in detail in the previous subsection. This error results in a decreased pulse width of the real PWM in this example. To do error correction, we can use $V_{pwm,ideal}$ as a reference. For the HSw transition, V_{pwm} is not at PGND during t_d. This can later be compensated by delaying the V_{pwm} low-to-high transition by the same amount of time, as shown in Fig. 5.4. The same applies to the SSw transition, where the V_{pwm} high-to-low

transition can be delayed for compensating the missing pulse width where V_{pwm} stays at V_{DDP}. The difference here is that the delay for compensating the error is half the V_{pwm} rising time t_{LH}, assuming a constant slewing rate. Both variable delays can be implemented in the dead time generator as shown in Fig. 5.5(b) (Fig. 5.5(a) shows a common implementation of the dead time generator), and Fig. 5.6 illustrates the controlled output by the inserted variable delay. Since it is the pulse width difference makes the error here, the variable delay cells can be implemented using integrators: first the error voltage is integrated ($V_{error} = \int_{\text{Dead time starts}}^{\text{Dead time ends}} (V_{pwm\_ideal} - V_{pwm\_real})dt$), subsequently for cancelling this prior integrated error voltage, variable delay time only ends when the compensation voltage also reaches V_{error} ($V_{error} = \int_{V_{pwm\_ideal}\ \text{changes state}}^{\text{Variable delay ends}} V_{pwm\_real}dt$). Utilization of this principle for linearity improvement has been reported in [75]. In our settings (Fig. 5.5(b)), transistor-level simulation in Spectre also shows that approximately 3x decrease in THD can be achieved with the compensation delay added and using identical feedback loops.

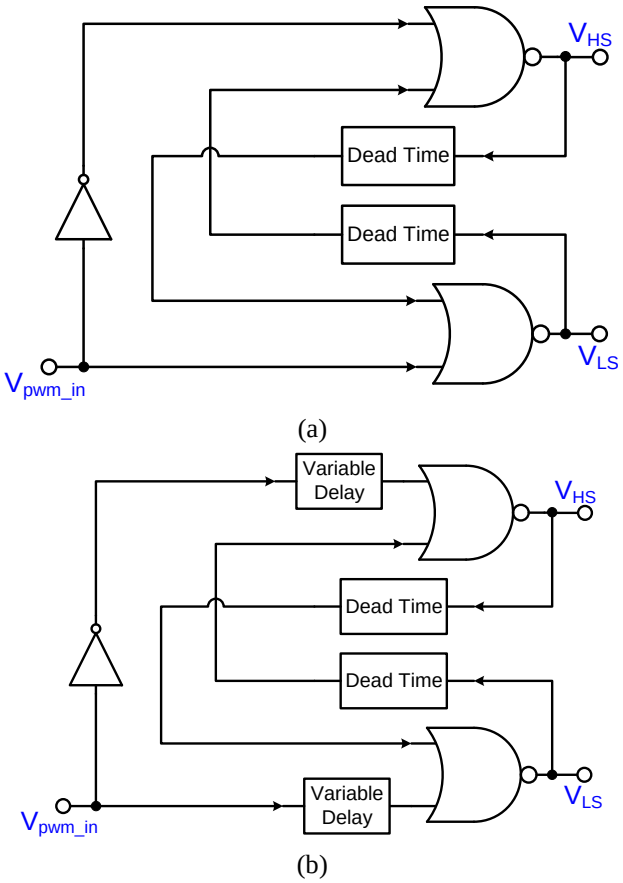


Fig. 5.5. Implementation of the dead time generator (a) original one (b) when incorporating a variable delay for V_{pwm} error correction

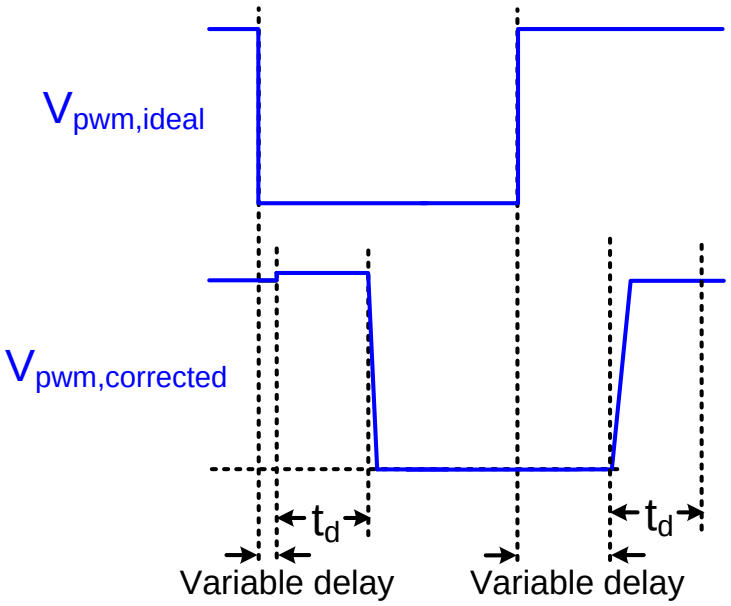


Fig. 5.6. Illustration of corrected V_{pwm} output when variable delay is added to the dead time generator

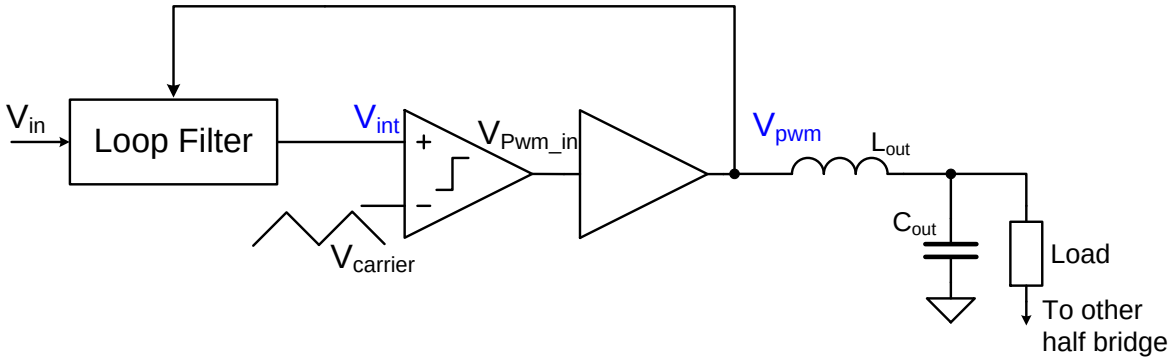


Fig. 5.7. Fixed-carrier PWM feedback loop under discussion

5.4 Feedback loop configuration

The error correction scheme described in the previous section can correct the open-loop power stage output error. However, this will introduce a delay from the PWM input of the power stage to the output V_{PWM}. With this delay present in the output stage, the very high loop gain provided by hysteretic-based feedback loops used in chapter 4 can degenerate significantly [74], so these feedback loops are less suitable to combine with the error correction scheme described here. As an alternative, fixed-carrier PWM feedback loops [8], [12], [14], [16], [18]-[20] can provide a well-defined loop gain and are investigated further here. Fig. 5.7 shows the configuration of the fixed-carrier PWM feedback loop under

discussion with differential input/output (BD type modulation [74]). We choose a bridge amplifier topology for further investigation because this structure can eliminated even-order harmonics, resulting in better THD performance. For the loop filter, we will only discuss 1st-order and 2nd-order loop filters as shown in Fig. 5.8. This is mainly because of the clip-recovery problem typically associated with higher-order loop filters [12],[51].

A 2nd-order loop filter will provide much higher loop gain for output stage error suppression compared to a 1st-order loop filter. However, PWM feedback loops generate THD themselves [52],[54] and 2nd-order PWM feedback loops generate more distortion than 1st-order ones. This is shown in the Simulink simulation results with ideal components in Fig. 5.9(a). For the simulation, f_{sw} is chosen at 500kHz and the signal frequency is at 1.144kHz. For the 1st-order loop, the unity gain bandwidth (UGB) of the class-D amplifier is 80kHz. For the 2nd-order loop, UGB is 80kHz and the zero is located at 40kHz. The THD performance of the feedback loop itself will get even worse with higher signal frequency, as shown in Fig. 5.9(b) with signal frequencies up to 6.485kHz.

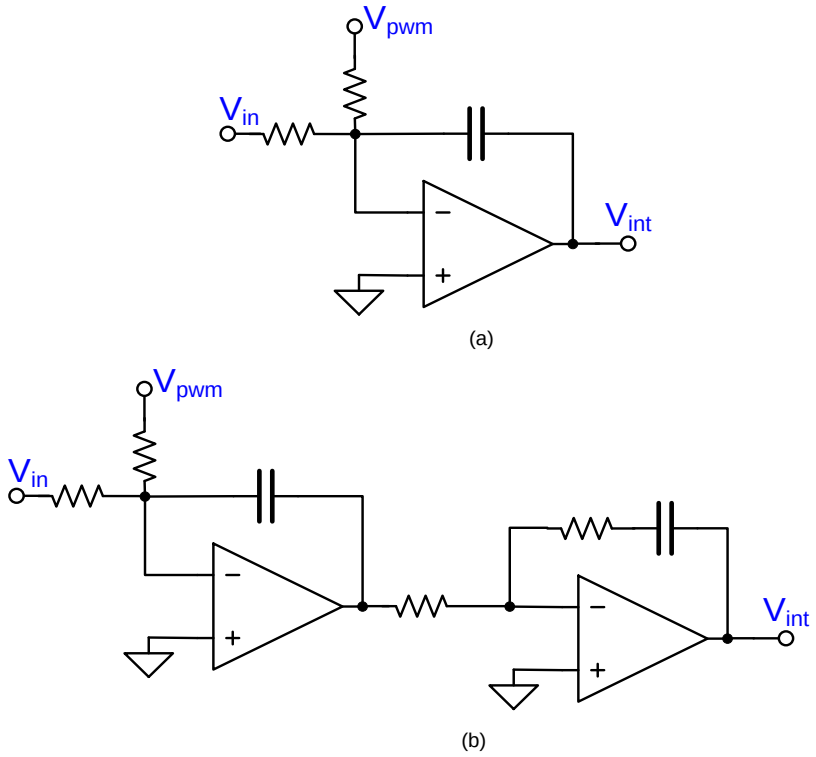
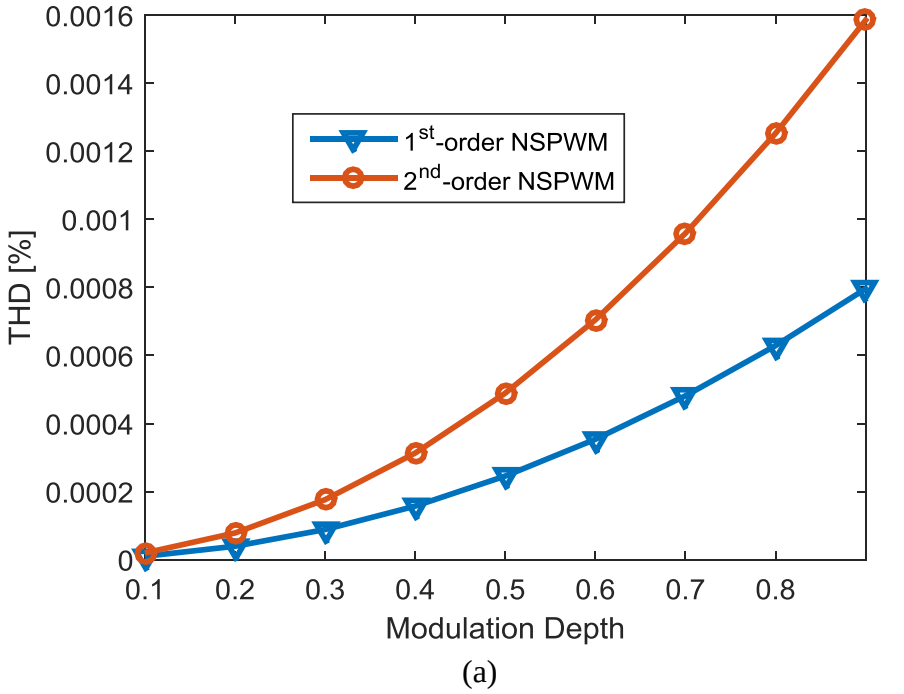


Fig. 5.8. (a) a 1st-order loop filter (b) a 2nd-order loop filter



(a)

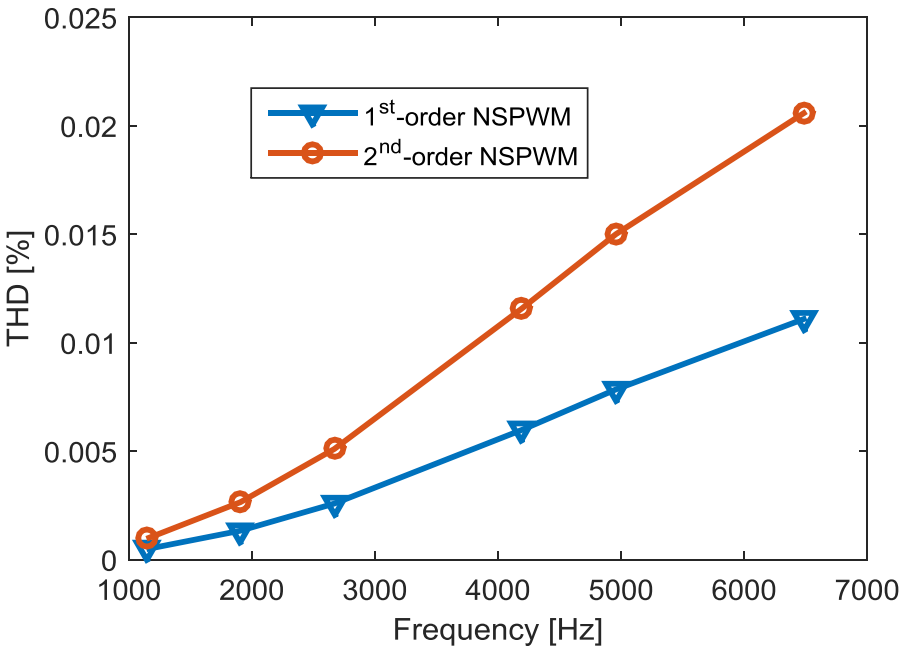


Fig. 5.9. THD of 1st-order and 2nd-order PWM feedback loops. For the Simulink simulation, f_{sw}=500kHz. For the 1st-order loop, unity gain bandwidth (UGB) is 80kHz. For the 2nd-order loop, UGB is 80kHz and the zero is located at 40kHz. (a) For a signal frequency of 1.144kHz and variable modulation depth (b) For a modulation depth of 0.7 and variable signal frequency

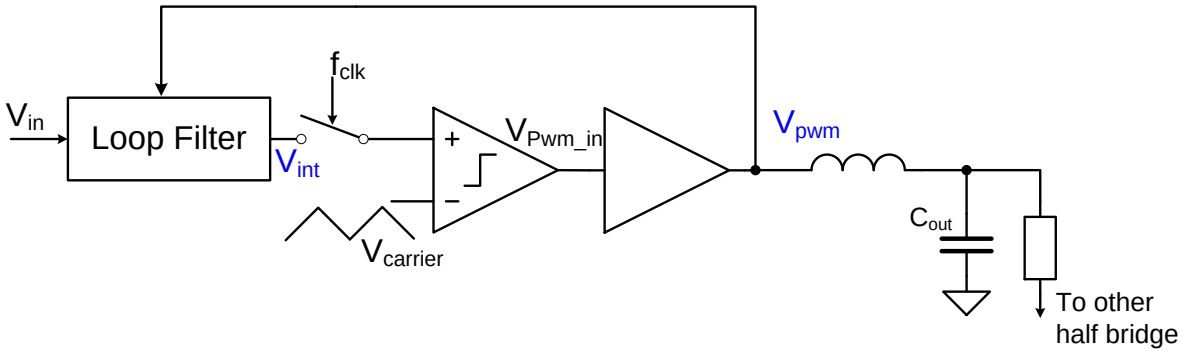


Fig. 5.10. Fixed-carrier PWM feedback loop with sampling added

It is known that the PWM residual ripple on V_{int} is the main source of the distortion [52],[54]. For this reason, sampling V_{int} has been adopted to eliminate this residual ripple and enhance the class-D amplifier linearity performance (Fig. 5.10). The modulator then effectively uses Uniform Sampling PWM (UPWM) [55]. Yet the influence of the sampling clock frequency on the linearity performance has not yet been explored. Fig. 5.11 shows two possible f_{clk} settings and their respective sampling timing arrangements, with one setting being $f_{clk}=2*f_{sw}$ [55] and the other being $f_{clk}=f_{sw}$. THD performance for these two settings with a 2nd-order loop filter are given in Fig. 5.12, together with THD of 1st- and 2nd-order PWM feedback loops using natural sampling (NSPWM). It can be seen that the UPWM loops with $f_{clk}=f_{sw}$ can provide the best THD performance.

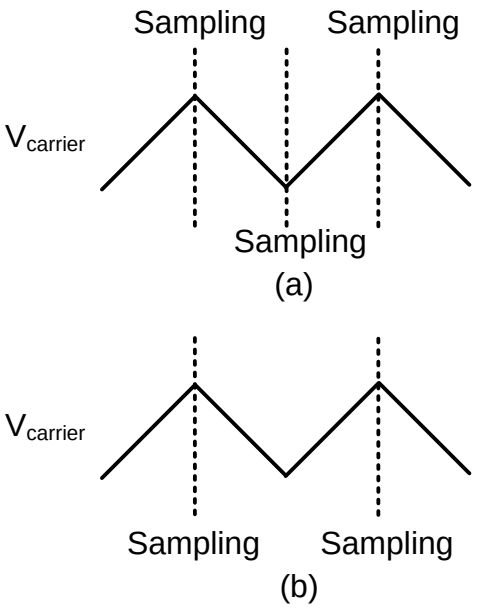


Fig. 5.11. (a) Illustration of the sampling timing with $f_{clk}=2*f_{sw}$. (b) Illustration of the sampling timing with $f_{clk}=f_{sw}$

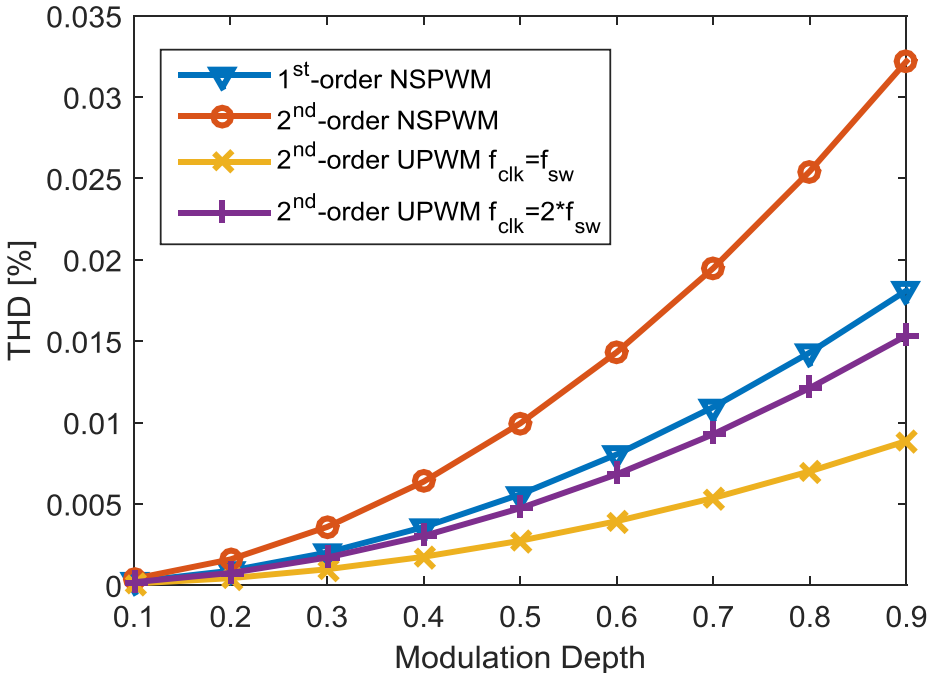


Fig. 5.12. THD performance comparison for various feedback loop implementations. This is based on Simulink simulations with ideal components, signal frequency at 6.485kHz and f_{sw}=500kHz.

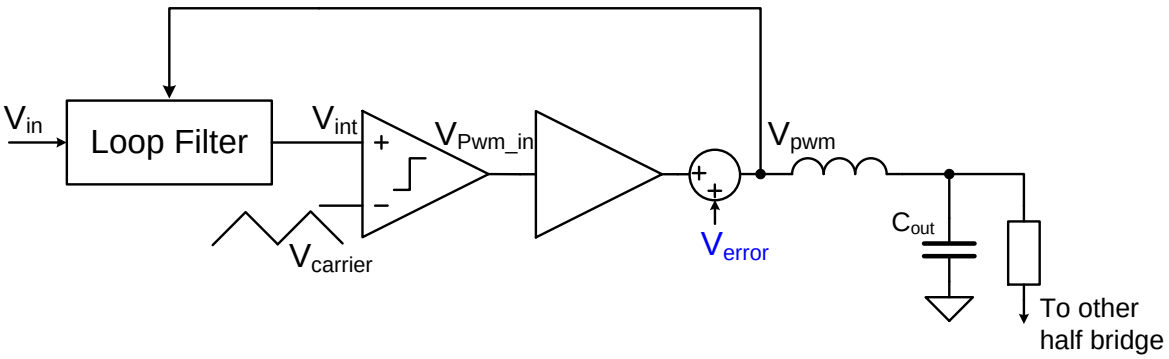


Fig. 5.13. Illustration of simulation setup for verifying the error correction capability of the feedback loops.

Regarding the error correction capabilities for these feedback loops, e.g. for the output stage error described in section 5.2 and 5.3, a simulation setup as shown in Fig. 5.13 is used. Here, V_{error} can be used to model the output stage error or disturbance from the power stage supply voltage. V_{error} attenuation is measured here as V_{error}/residual error voltage at the output. Fig. 5.14 shows the Simulink simulation results. We can see that the error attenuation

capability is only related to the loop gain (loop filter type) and is not influenced by whether sampling is present or the UPWM sampling frequency.

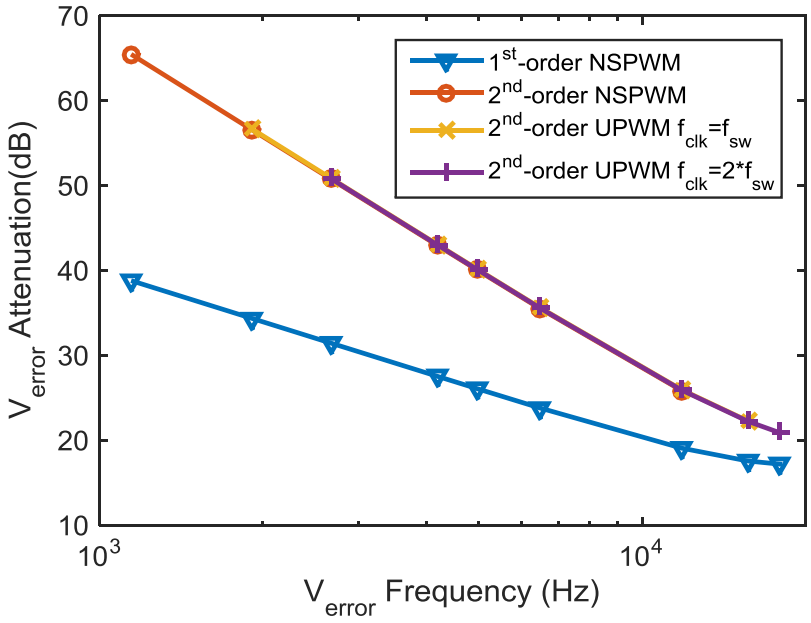


Fig. 5.14. Simulink simulation result of the error attenuation (V_{error}/residual error voltage at output) capability for the various types of feedback loops.

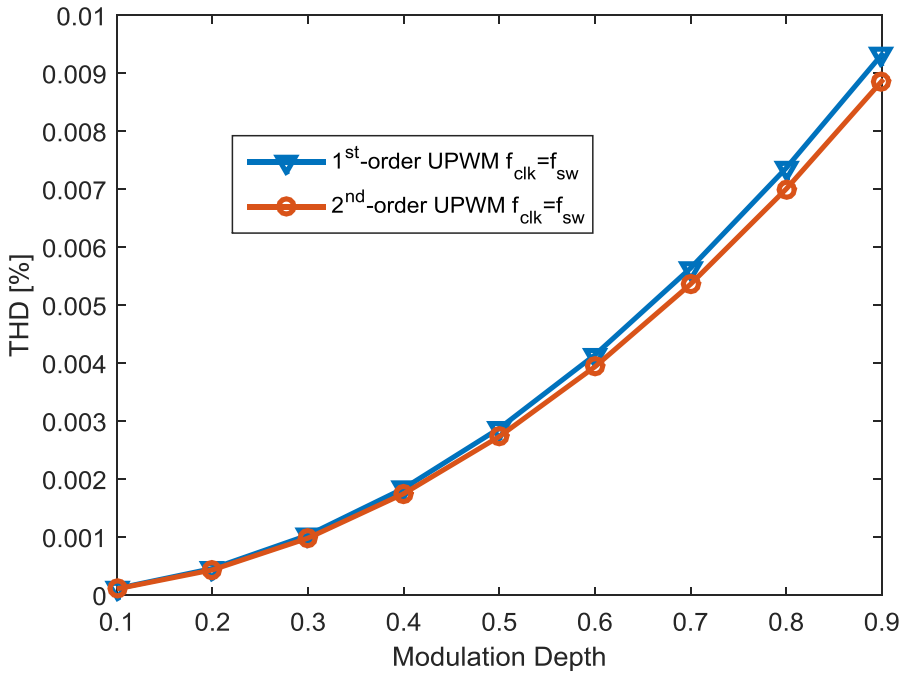


Fig. 5.15. Properties of UPWM with $f_{clk}=f_{sw}$. This is based on Simulink simulation results with ideal components, with signal frequency at 6.485kHz and f_{sw}=500kHz..

Another interesting property of UPWM with $f_{clk}=f_{sw}$ is that the THD introduced by the feedback loop is almost irrelevant to the loop filter configuration. This is shown in Fig. 5.15. As a result, for this configuration, the high loop gain of a 2^{nd}-order loop filter for error correction is the better choice because it doesn't cause THD degradation introduced by the feedback loop itself. The underlying mechanisms for this property are still open to further research..

5.5 Conclusions

The insertion of dead time can be used for efficiency optimization, compromising the linearity performance. Error correction of the open loop output stage can be adopted for linearity improvement. For feedback in a fixed-carrier topology, a higher order loopfilter with uniform sampling at $f_{clk} = f_{sw}$ is the best option.

CHAPTER SIX

6. Conclusions and Future Work

6.1 Summary and Conclusions

In Chapter 1, first a brief introduction was made of power amplifiers as transducer drivers in general, and as piezo-actuator driver in active vibration/noise cancelling applications in specific. This was followed by an overview of common power amplifier types for audio-frequency power amplification. It was shown that a class-D topology can offer the highest power efficiency and thus is chosen as the main research object for analysis and optimization. After an overview of current state of the art class-D designs, the major motivation of this thesis was clarified, i.e. identify the dominating dissipation sources in a high-voltage class-D amplifier and further optimize its power efficiency.

In Chapter 2, to clarify the dominating dissipation sources in a high-voltage class-D amplifier, a dissipation model was built to identify all the contributing dissipation sources in a class-D power stage. With a high output stage supply voltage present, the switching loss at the switching PWM output node can be significant so this was analyzed and modeled in detail. In the switching loss analysis, three different types of switching scenarios were summarized, 1) lossless soft switching, 2) partial soft switching and 3) hard switching. And it was further shown that these three different switching scenarios highly depend on circuit operating conditions, e.g. output load current, inductor ripple current, dead time etc. For verification, the developed loss model was compared with transistor-level simulation results and they matched well with each other. This showed that all the major contributing dissipation sources had been taken into account in the dissipation analysis.

With the developed analytical model, understanding of underlying loss mechanisms in a high-voltage class-D power stage has been established. This led to three directions in which efficiency improvement can be done, 1) reducing switching loss with fast switching at the output PWM switching node, as to minimize V-I overlap loss during the switching transitions. 2) extending high-efficiency output power range by varying the switching frequency, as to simultaneously reduce inductor ripple current induced loss and the switching induced loss. 3) further enhancing efficiency at idle/low output power by switching at relatively higher switching frequency and inserting large dead time, as to minimize inductor ripple current induced loss. The three efficiency improvement direction were exploited in the subsequent three chapters respectively.

In Chapter 3, the design of a fast-switching class-D power stage was discussed. It was first shown that fast switching is associated with significant on-chip supply bounce and that this can jeopardize the functionality and degrade the efficiency of the class-D power stage. To get insight into how the switching speed gets limited, the gate driver sizing issue was discussed in detail. For a conventional gate driver circuit, the driver pull-up current should be much smaller than the pull-down current to avoid cross conduction. With this limitation, it was analyzed that the driver pull-down current should be constrained in the first place as to limit the on-chip supply bounce. Consequently the driver pull-up current is further limited to a great extent, which results in slow switching and high switching loss.

Following this analysis of the conventional driver sizing limitations, the floating gate driver circuit was proposed and analyzed in this chapter. The basic idea is to decouple the pull-up/pull-down driver strength requirement. This is done by an in-cycle variable gate driver strength, i.e. use small pull-down driver strength to limit on-chip supply bounce and employ large keep-down driver strength to avoid cross conduction. This way fast switching transition by large pull-up current and low on-chip supply bounce by relatively small pull-down current can be achieved simultaneously. By further adopting on-chip regulated floating gate driver supplies, the maximum allowable on-chip supply bounce is also relaxed, with the floating regulator circuit shielding the low-voltage gate driver circuits from the high-voltage-amplitude on-chip supply bounce.

Furthermore, the design of a power-efficient and low-delay level shifter circuit was also discussed in this chapter. The level shifter circuit needs to be able to handle the PWM switching node slewing induced common-mode disturbance. In addition, it needs to transfer

with high speed the digital signal between different voltage domains without demanding high current consumption. An active load featuring partial positive feedback is introduced in the level shifter circuit for this purpose. It has high impedance for differential-mode signal transfer while shows low impedance for common-mode disturbance. As a result, the bias current requirement for distinguishing between common-mode disturbance and differential-mode signal transfer is relaxed. In addition, pulsed input signals also help to further reduce the power consumption.

In Chapter 4, using switching frequency regulation to perform optimal efficiency tracking from idle to maximum output power was presented and analyzed, and a class-D amplifier featuring extended high-efficiency output power range was designed. Based on the loss model developed in chapter 2, it was shown that the inductor ripple current induced loss is dominating at low output power regions, as long as the switching transition is lossless soft switching. In this case, the switching frequency can be increased to reduce inductor ripple current induced loss, as long as the switching transitions remain lossless soft switching. On the other hand, if switching loss is present, the switching frequency can be decreased to minimize this type of loss. When the switching frequency is adapted such that it is always at the boundary of lossless soft switching, simultaneously reduction of inductor ripple current induced loss and switching induced loss is achieved.

Following the analysis on switching frequency adaptation, a switching frequency regulation loop was constructed to always get to the optimal switching frequency and in turn the highest efficiency. It is based on detecting the output switching PWM node voltage level at the turn on transition of the output power switches. Based on a 1^{st}-order hysteretic-based amplifier topology, the switching frequency regulation loop is added to the amplifier by tuning the hysteretic window. The realized amplifier achieves >49% power efficiency across two orders of magnitude output power range and always maintains the highest efficiency compared with using fixed hysteretic window settings.

In chapter 5, the feasibility for further enhancing the high-voltage class-D amplifier efficiency at idle/low output power was studied. First, an analysis was done that shows the class-D linearity performance degrades proportional to the increase of switching frequency at low output power, when dead time is inserted in the output stage with a 1^{st}-order hysteretic feedback loop. To correct the dead time induced error, a switching moment retiming can be used to compensate the error and subsequently turn the error into a delay. Following the

introduced open-loop error correction, it was further analyzed what would be the optimal feedback loop with fixed-carrier topologies to further enhance the linearity performance. Sampling at the loop filter output can help eliminate the distortion introduced by the residual switching ripple. Based on this, it was shown that the sampling timing also has an influence on the linearity performance. After comparing various feedback loop topologies based on simulation results, the optimal choice of the feedback loop is to use a higher-order loop filter combined with uniform sampling once per PWM switching cycle.

6.2 Original Contributions

- Detailed dissipation modeling for a high-voltage class-D power stage, with critical inductor ripple current induced loss and switching induced loss identified.
- A sizing procedure for gate drivers in a class D output stage, with limitation of the on-chip supply bounce as a starting point.
- Design of a fast-switching class-D power stage featuring: 1) in-cycle variable gate driver strength, 2) on-chip floating gate driver supply and 3) a power-efficient level shifter circuit featuring an active load with partial positive feedback
- A switching frequency regulation technique that can maintain maximum efficiency from idle to maximum output power.
- Design and realization of a class-D amplifier that employs this switching frequency regulation loop.
- Analysis of the distortion level of an open-loop soft switching power output stage.

6.3 Recommendations for Future Work

- The performed dissipation analysis is made for a class-D power stage with high supply voltage (80V) and hundred-kHz switching frequency. The switching frequency regulation for extending the high efficiency output power range is also tailored for this application. For other applications, e.g. with several- Volt supply and MHz switching frequency, the dominating dissipation sources can vary and another regulating method to reach optimal efficiency may be required.

- Fast switching, though beneficial for switching loss minimization, is not desirable for EMI considerations. Avoiding this tradeoff is a possible direction for further research.

- Multiphase operation in a class-D amplifier can be further explored. This way the power stage has the possibility to maintain lossless soft switching up to maximum output power.

- It has been shown intuitively that uniform sampling once per switching cycle at the loop filter output isolates the UPWM procedure from the feedback loop. This feature can be further explored in relation to external errors as to what extend it can improve THD performance.

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List of Publications

[1] **H. Ma**, R.A.R. van der Zee and B. Nauta, "An Integrated 80-V Class-D Power Output Stage with 94% Efficiency in a 0.14um SOI BCD Process," in *European Solid-State Circuit Conference* (ESSCIRC), Sept., 2013.

[2] **H. Ma**, R.A.R. van der Zee and B. Nauta, "An Integrated 80V, 45W Class-D Power Amplifier with Optimal-Efficiency-Tracking Switching Frequency Regulation," in *International Solid-State Circuit Conference* (ISSCC), Feb., 2014.

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[4] **H. Ma**, R.A.R. van der Zee and B. Nauta, "A High-Voltage Class-D Power Amplifier With Switching Frequency Regulation for Improved High-Efficiency Output Power Range," *IEEE Journal of Solid-State Circuits* (JSSC), vol. 50, no. 6, June, 2015.

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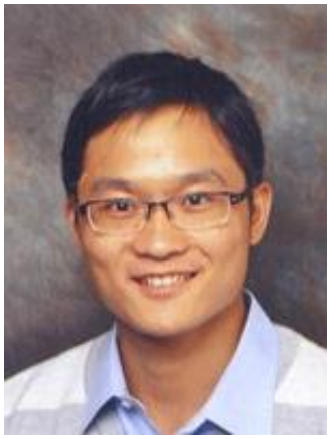
About the Author



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