Transmission Lines in CMOS: An Explorative Study

E. A. M. Klumperink*, R. Kreienkamp, T. Ellermeyer, U. Langmann

Lehrstuhl fuer Elektronische Bauelemente, Ruhr-Universitaet Bochum, Germany
* During April-July 2001 on sabbatical leave from:
MESA+ Research Institute, University of Twente, IC-Design group
P.O. Box 217, 7500AE, Enschede, The Netherlands
http://icd.el.utwente.nl Email: e.a.m.klumperink@el.utwente.nl

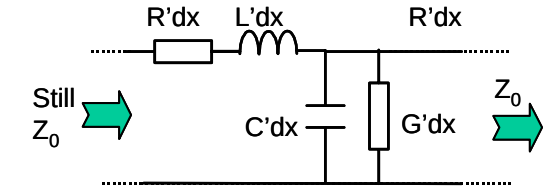
Abstract—**On-chip transmission line modelling and design become increasingly important as frequencies are continuously going up. This paper explores possibilities to implement transmission lines on CMOS ICs via coupled coplanar strips. EM-field simulations with SONNET are used to estimate important transmission line properties like characteristic impedance, propagation velocity and loss in a 0.18 micron CMOS Technology. Both metal losses and substrate losses are modeled. Special attention is paid to the effect of the Silicon substrate, in particular to the so called "slow-wave mode" that can occur in the Si-SiO2 system.**

Keywords – **Transmission line; wave-guide; CMOS; radio frequency; RF; microwave techniques**

I. Introduction

Since the seventies the clock speeds of digital CMOS ICs have continuously moved up from a few MHz to the low GHz region. At these GHz frequencies, the delay of on-chip wires is becoming a major concern, as it doesn't scale gracefully with technology [1][2]. Especially "long-distance" data-exchange between functional modules on a chip is troublesome, as chip sizes increase while clock frequencies also go up. Traditional bus designs using simple wires driven over the full supply swing not only have power dissipation problems, but are also facing serious signal integrity problems due to reflections and cross talk. Alternative design strategies traditionally only required in super computers, might help to overcome these problems [3]. Transmission line modelling, and careful designed line drivers and line receivers play a key role in such design strategies.

Analog circuits for radio- and optical communications typically operate at even higher frequencies than digital circuits. At these RF frequencies low loss passive components are wanted, e.g. in low-noise amplifiers, oscillators and filters. At the low GHz frequencies spiral inductors are used. For higher frequencies, transmission lines could be exploited [4]. A shorted transmission line, for instance behaves as an inductor up to the quarter lambda frequency [7]. In order to achieve high quality factor for the coils, losses should be minimized. For CMOS technology, coplanar stripline structures with losses as low as 0.3dB/mm have been reported, but in non-standard technologies[6][10]. This paper explores transmission line properties of transmission lines in a *standard* industrial 0.18 micron technology with 5 Aluminium layers. Using the SONNET EM-field simulator, the characteristic impedance Z0 and loss for coplanar strips will be examined. Metal losses and substrate losses are modeled and their effect is evaluated. Furthermore special attention will be paid to the so called slow wave-propagation mode, which can occur at low GHz frequencies in SiO2-Si structures with a thin oxide relative to the Silicon thickness [8]. We will examine whether this mode occurs and whether it could be exploited to advantage in contemporary CMOS technologies.



$$Z_0 = \sqrt{\frac{R'+j\omega L'}{G'+j\omega C'}} \approx \sqrt{\frac{L'}{C'}} \qquad V(x) = V(0)\exp(-\gamma x)$$

$$\gamma = \sqrt{(R'+j\omega L')(G'+j\omega C')} \approx j\omega\sqrt{L'C'} + \frac{R'}{2Z_0} + \frac{G'Z_0}{2}$$

Figure 1: Distributed circuit element model for a transmission line section and the resulting equations for characteristic impedance and propagation constant. The approximate formulas only hold for frequencies well above f-RC-LC-takeover.

The structure of the paper is as follows. In section II, transmission line design considerations will briefly be reviewed, aiming for low loss lines. Section III discusses how we simulated the on-chip structures with relatively large vertical metal dimensions using the planar EM field simulator SONNET. In section IV transmission line simulation experiments in CMOS are reported, to estimate achievable characteristic impedance and loss. Section V finally discusses the slow-mode wave propagation mode and its application perspective in CMOS Technology. Finally conclusions are given in section VI.

II. Transmission Lines Design Considerations

Lord Kelvin and Oliver Heaviside already developed a technique to analyze impedance and propagation characteristics of a transmission line using a distributed circuit element model (see Figure 1). In such a model the line is characterized in terms of L' (series inductance per unit length), C' (capacitance per unit length), R' (series resistance per unit length) and G' (shunt conductance per unit length). For lossless lines the well know result for the characteristic impedance is $\sqrt{L'/C'}$ and $1/\sqrt{L'C'}$ for the wave propagation velocity. However, on-chip transmission lines are far from lossless. To illustrate this point, Table 1 gives some typical values for practical wires.

	wire cross-section	**L' [nH/m]**	**C' [pF/m]**	**R' [ohm/m]**
On chip wire	0.5u*0.5u	600	200	150k
PC Board	150u*50u	300	100	5
Twisted pair	~500u diameter	400	40	0.08

Table 1: Typical values of the distributed inductance L', capacitance C' and resistance R' parameters comparing a typical on-chip wire with PC board and twisted pair. Clearly, the loss of on-chip wires is orders of magnitude larger than off chip.

The shunt conductance usually is negligible for on-chip structures (Arz find less than .02S/cm for G' [9]). The values of L' and C' are relatively high for on-chip wires, but are still in the same order of magnitude than for off-chip wires. However, as metal cross-section area is orders of magnitude smaller, the resistance per unit length is many orders of magnitude larger. Furthermore, metal thickness is smaller than the skin depth, typically up to tens of GHz, which means that the resistance and inductance per meter is relatively frequency independent. Hence, DC metal losses are of primary concern if we want to design low loss transmission lines.

Due to the high metal resistance, on-chip wires behave much like RC lines up to the frequency where the inductive series impedance is equal to the resistance per meter. This takeover frequency is:

$$f_{RC-LC-takeover} = \frac{R'}{2\pi L'}$$

Only above this frequency, the approximate equations given in Figure 1 are valid. In that case the main effect of metal loss is signal attenuation, which can conveniently be expressed in dB:

$$Loss[dB] = \frac{10}{\ln(10)}\frac{R'l}{Z_0}$$

For example: a wire with R'=100kohm/m and 50ohm characteristic impedance renders a loss of 8.7dB/mm.

A. Single Microstrip Line

For planar wiring technologies like printed circuit board and IC technologies, the microstrip is probably the most commonly used transmission line structure. Its resistance and capacitance per unit length can be estimated by [3]:

$$R'_{DC,metal} = \frac{\rho_{metal}}{w \cdot h}$$

$$C'_{ms} = \varepsilon_{ox}\frac{w}{d_{ox}} + \frac{2\pi\varepsilon_{ox}}{\ln(4d_{ox}/h)}$$

where ρ_{metal} is the metal resistivity (~28E-9 ohm·m for Al, ~17E-9 ohm·m for Cu), w is metal width, h the metal height and d_{ox} the oxide thickness. Assuming TEM mode wave propagation, the following characteristic impedance is found:

$$Z_{0,ms} = \frac{\sqrt{\mu\varepsilon_{ox}}}{C'_{ms}}$$

From these equations the following design guidelines for microstrips can be extracted:

- In order to achieve low losses wide (large w) and thick wires (large h) are desired. This is because the w- and h-dependence of R' dominates that of C' (due to the presence of the second term in the C' equation)
- In order to minimize the losses and maximize the characteristic impedance, thick oxide is desired. Maximizing characteristic impedance is attractive to save power consumption, as less current is needed for the same voltage swing.

Taking these considerations in mind, the conclusion is that we want to use the thick top metal layers (low resistance R' and low capacitance C') for low loss high Z_0 transmission lines.

B. Coupled Coplanar Striplines

Apart from the metal losses, the silicon substrate is expected to introduce losses. If coplanar coupled strips are used, the field lines tend to concentrate between these lines [4], provided that they are driven in odd mode (anti-phase, balanced). Moreover, using symmetrical balanced driven lines and differential circuit techniques is good on CMOS substrates in order to reduce substrate interference problems.

If coupled lines are used, the mutual inductance and mutual capacitance of the coupled lines affect the characteristic impedance. As a result, the characteristic impedance observed looking into one line depends on the way the other line is driven. The odd-mode impedance is now defined as the impedance observed at one line, under the condition that the other line is driven in anti-phase, while in even-mode the other line is driven with the same signal.

Figure 2 shows the odd-mode and even-mode impedance for a typical pair of coupled strips as a function of their separation distance. At large distance the inductance L' and capacitance C' determine the high frequency characteristic impedance. At low separation distance the mutal inductance M' and capacitance C_m' result in an increased even-mode impedance, and reduced

odd-mode impedance. Thus, for a pair of coupled strips not only the width affects the impedance and loss, but also the strip separation distance s. The effect of s on loss is not so easy to predict. On the one hand, increasing s increases the characteristic impedance which tends to reduce the Loss [dB]. On the other hand small separation distance might be attractive to concentrate the EM-field between the conductors, hence reducing substrate loss. We will examine this effect further via simulations in section IV. However, first we will address the way we do the simulations via SONNET.

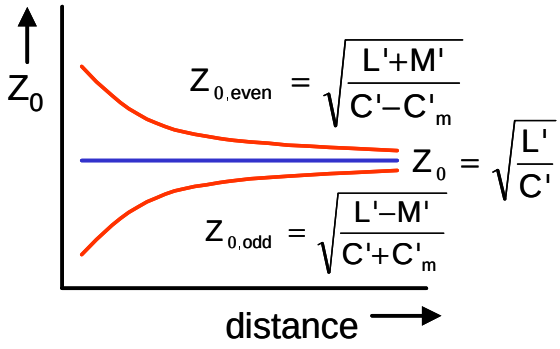


Figure 2: Characteristic Impedance of coupled lines under Odd mode and even mode drive conditions. For large separation distance the coupling is negligible, and the impedance of a single line is found.

III. SONNET SIMULATIONS OF CMOS LINES

We want to simulate coupled transmission line properties for varying metal width and separation. This means that a lot of simulations are needed for many parameter combinations. The SONNET EM field simulator allows parameterizing metal dimensions, is fast and has good convergence properties. However, SONNET basically assumes zero metal layer thickness, and models the skin effect with a frequency dependent resistance of the metal layer segments. For printed circuit board this model works fine. For a CMOS IC however, the metal thickness is typically in the same order of magnitude than metal width or even larger. It is possible to model thick metal in SONNET using two parallel metal layers connected with vertical so-called "VIAs". In order to get confidence in this way of modeling we decided to compare SONNET simulation results with results obtained with the 3D EM-field simulator FastHenry and FastCap developed by the Laboratory of Electronics (Massachusetts Institute of Technology, Cambridge, MA, USA). Table 2 shows the results for a single metal wires with width w, thickness 3 micrometer, located at 3.5 micron distance above a low wide metal ground plan with SiO2 as dielectric.

Looking at the result in the table, it is clear that using a single metal layer model does not give accurate results. It overestimates the inductance as all current is concentrated close to the ground plane. Especially the metal losses are over-estimated. Using two parallel metal layers gives much more accurate results, that are roughly with 10% of the 3D simulations, which is in the order of typical differences found between simulation and measurements.

Parameter	3D	SONNET 1 Metal	SONNET 2 Metal	3D	SONNET 2 Metal
w	2.4	2.4	2.4	4	4
R' [kohm/m]	9.68	30	11.7	7.8	7.6
L' [uH/m]	.40	.69	.44	.344	.365
C' [pF/m]	88	86	83	105	101
Z0 [ohm]	67.4	90	73.5	57.2	60.2

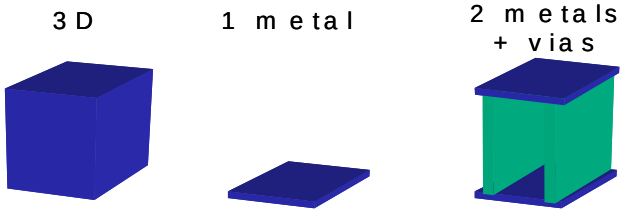


Table 2: Comparison between 3D simulation results and SONNET split metal and single metal simulations

IV. CMOS TRANSMISSION LINE SIMULATIONS

We gathered data from industrial CMOS processes and defined a "typical" 0.18 micron CMOS process with low-ohmic substrate and 5 Aluminium metal layers (copper will be introduced later). On top of a highly doped substrate (10mohm*cm, 600 micron thick), an epi-layer of 4 micron of moderate resistivity is assumed (10ohm*cm). The lower metal layers have a thickness of 0.5 micron for local interconnect, while the top layers for global interconnects have double thickness (1 micron). In order to allow for high density wires, the metal aspect ratio h/w can be as high as 1.3 and will probably go up in the future [2].

We will now simulate coupled transmission line configurations that can be realized in a 0.18 micron CMOS Technology. As motivated in section II, coupled lines in the top metal layer, driven in odd mode are used. We start in section A with coplanar lines above a wide ground plane in metal 1, acting as a shield to the Silicon substrate. In section B the shield is removed to examine the effect of the substrate.

All simulations are done at 40GHz, because this is high enough for Z0 to become frequency insensitive. Furthermore, 1 mm of line is approximately ¼ lambda at that frequency for a TEM mode transmission line with SiO2 dielectric. Hence, microwave engineering techniques [7] could potentially be applied on chip at that frequency, and the transmission line properties in that frequency region are of interest.

A. M5-SiO2-M1 Coupled strips

Figure 3 shows a cross-section of the structure that was simulated. A 30micron wide metal1-layer is used as a ground plane with 0.5 micron thickness. The actual coupled lines are realized in 1 micron thickness metal5, 4.3 micron above the metal 1 plane.

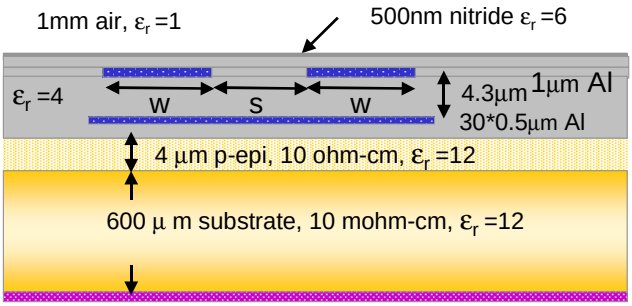


Figure 3: Coplanar striplines in Metal 5 above a Metal 1 groundplane. M1 shield the substrate from the lines.

The metal width w of the coupled strips and separation distance s are the key design parameters. The simulated characteristic impedance is shown in Figure 4. As expected, the curves have the same shape as the curves in Figure 2. The achievable values are in the range of 30-100 ohm, with high values for narrow wires.

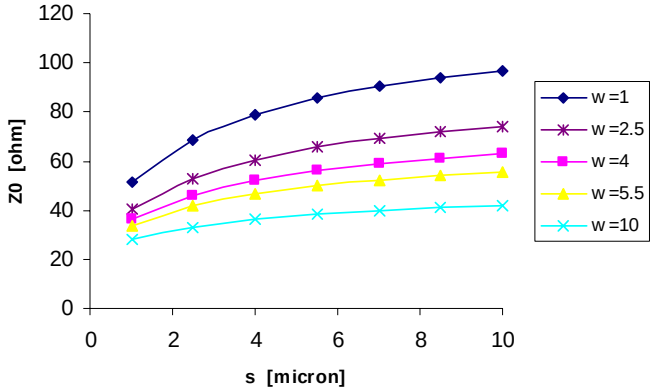


Figure 4: Odd mode characteristic impedance of metal 5 coplanar striplines above a metal 1 ground shield as a function of separation distance s for various strip widths w.

Figure 5 shows the loss in dB/mm at 40GHz. In accordance with the expectation in section II, it decreases with metal width. It also decreases with metal separation, as the (metal) resistance remains constant, while the characteristic impedance goes up, resulting in less loss per mm.

Increasing metal width and separation monotonically reduces loss. However above approximately 5 micron width and separation, the loss does only reducing slowly. Hence w=5 and s=5 seems a reasonable practical compromise between characteristic impedance (~50ohm), metal loss (~1.2dB/mm) and area. Detailed analysis of the results shows that there is a small frequency dependence in R' and L' due to the skin effect. At 40 GHz the resistance is roughly doubled.

B. M5 strips above Silicon (M1 removed)

The same simulations were repeated after removing the metal 1 shield. The resulting characteristic impedance curves are shown in Figure 6. The curves very much look like those with metal shield, except that the impedance is somewhat higher due to the thicker oxide between metal 5 and the grounded epi-layer (effectively the 600 micron substrate as a ground plane due to its very high doping (resistance ~ 1ohm/square).

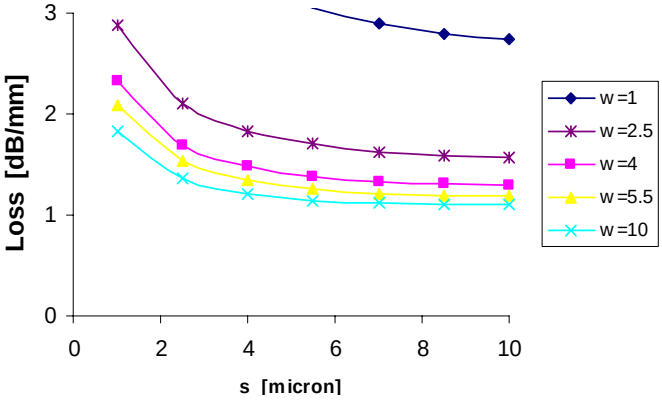


Figure 5: Loss in dB/mm of metal 5 coplanar striplines above a metal 1 shield.

The loss simulation results are not shown as they look very much the same as those in the previous section. Instead, Figure 7 shows the loss for w=5.5 micron, to allow for a detailed comparison. Somewhat surprisingly, the removal of M1 has a slight positive effect on loss. Although the substrate add some loss, the effect on characteristic impedance is stronger (+15%). As a combined result the loss slightly decreases by the removal of the metal 1 shield.

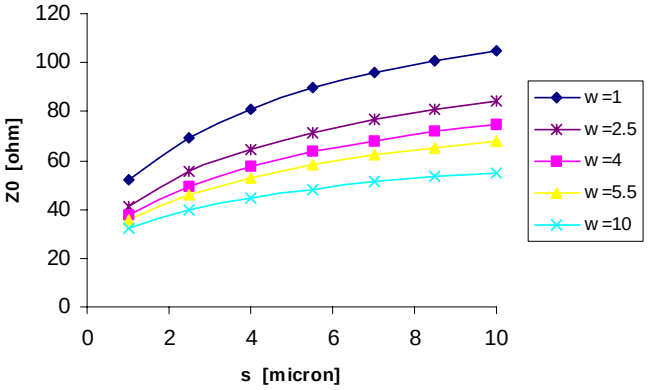


Figure 6: Odd mode characteristic impedance of metal 5 coplanar striplines above unshielded epi (no M1 shield).

We also did some other experiments. In some technologies there are more thick top metal layers. In that case it is effective to use two metal layers in parallel, as the metal losses are reduced more than the characteristic impedance increases. Of course, IC technologies with copper metal layers also have lower loss. For 1 micron copper we found that the losses reduce from 1.2dB/mm to 0.8dB/mm (5 micron strips at 5 micron separation distance).

Also coplanar waveguides proposed by Kleveland were simulated. The best loss was around 1 dB/mm. Better results below 0.3dB/mm have been published, but this is in a technology with thicker copper layers [6] or with special post-processing techniques to increase the characteristic impedance by means of a dielectric with low dielectrical constant (e.g. polyamide [10]).

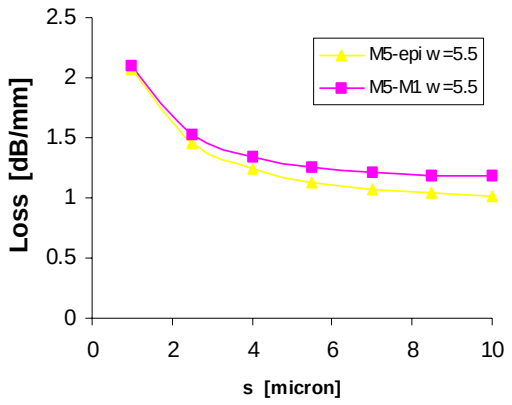


Figure 7: Detailed comparison of the loss of M5 coplanar strips above a metal 1 ground shield and unshielded epi-layer.

In all technology scaling scenarios, metal losses are increasing. Especially if the metal layer thickness comes close to 100nm, drastic increases in wire resistance above bulk resistance are expected due to thin film effects like grain boundary effects and surface scattering effects [1]. With this predicted increase of metal resistance in downscaled technologies, metal losses are likely to become even more of a problem for the design of on-chip low-loss transmission lines, unless a thick low ohmic metal layer remains available. Such "super-wires" are assumed in some technology scenarios, e.g. RF components and for clocking nets, although others assume that the top-layers will also be downscaled (see papers in the April issue of IEEE Proceedings, e.g. [2]).

V. SLOW-WAVE MODE

Transmission lines are usually designed to convey EM-waves with a Transversal Electrical and Magnetical component (TEM-mode). The propagation speed of such waves is somewhat lower than the speed of light, depending on the dielectricum ($c/\sqrt{\varepsilon_r}$). For SiO2 which has a dielectric constant of around 4, this leads to a wavelength of about 1mm at 40GHz. Hence, exploiting wavelength dependent microwave effects on chip, e.g. impedance transformations using a ¼ lambda waveguide, only is possible at very high frequencies. In the seventies, Hasegawa [8] suggested that much smaller structures are possible if a Si-SiO2 sandwich is used as a dielectric between two metal layers (see Figure 8). In this wave propagation mode, the propagation speed can be more than an order of magnitude lower than for the TEM mode, if d_{ox} is much smaller than d_{si}. In the original paper this effect is described by the so-called Maxwell-Wagner polarization mechanism, which results in a high effective dielectrical constant:

$$\varepsilon_{r,effective} = \frac{d_{ox} + d_{Si}}{d_{ox}} \varepsilon_{r,SiO_2}$$

An intuitive way to understand how this slow propagation speed can result is to examine which dimensions determine L' and C', and hence the propagation speed [6]. For commonly used transmission line structures with a single dielectric, the same physical dimensions determine L' and C' in the opposite way. As a result, the dimensions dependency falls out of the equation for propagation speed and depends only on the speed of light and dielectrical constant.

However, the SiO2-Si sandwich does not have this property. Actually, the Si acts as a conductor for voltage changes between the metal layers, and voltage changes on the top metal layer are followed by charge at the Si-SiO2 interface up to frequencies as high as a few GHz (depending on the doping level of the Silicon). Hence, the effective C' is equal to the oxide capacitance per meter, and depends only on d_{ox} and NOT on d_{Si}. In contrast, the inductance L' depends on the distance between the metal layers, and hence on $d_{ox}+d_{Si}$. Due to these different dependencies, L' remains roughly the same than for the TEM mode, but C' is much higher, especially if $d_{ox} << d_{Si}$. In this way the effective epsilon can be as high as hundred or more, much higher than that of Si (12) and SiO2 (4).

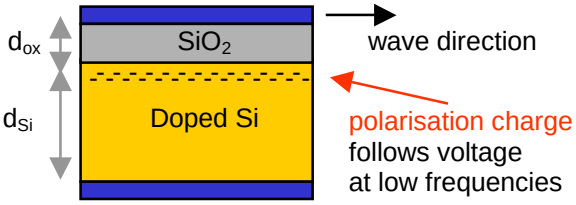


Figure 8: Si-SiO2 sandwich used as dielectricum. L' is determined by dox+dSi, while C' is determined by dox. As a result the propagation velocity can be much lower than in TEM-mode.

Figure 9 gives an overview of the three main wave propagation modes in the Si-SiO2 system as a function of Silicon resistivity. At low frequencies, the slow-wave mode occurs. At high frequencies and high resistivity (i.e. low doping), the Silicon approximately acts as and insulator, and TEM mode wave propagation occurs. On the other hand, if the doping is high and the Silicon has low resistivity, it acts more or less as a conductor. Hence EM fields don't penetrate deep in the Silicon and only a thin "skin" layer carries the main current (skin effect mode wave propagation). In the region in between, for moderate resistivity, the slow-mode occurs up to the highest frequency. Detailed analysis shows that the maximum frequency (the top of the red curve) at which the slow wave occurs is approximately given by [8]:

$$f_{slow,max} \approx \frac{1}{2\pi\rho_{Si}\varepsilon_0\varepsilon_{SiO_2}} \frac{d_{ox}}{d_{Si}}$$

This peak value is achieved at a certain "characteristic" resistivity given by [8]:

$$\rho_{char} = \sqrt{\mu_0 d_{ox} d_{Si} / (3\varepsilon_0 \varepsilon_{SiO_2})}$$

For typical CMOS layers thickness, the highly doped Si substrate effectively acts as a conductor. However, a thin oxide layer in combination with epi-layer Silicon can show the slow-wave up to frequencies well in the GHz region.

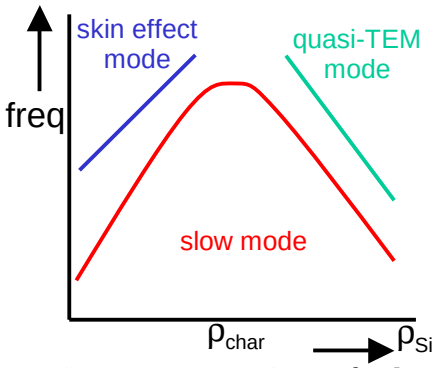


Figure 9: Overview of the three wave propagation modes that can occur in a Si-SiO2 system depending on the Si-substrate resistivity.

Figure 10 shows a SONNET simulation result for a single lossless metal microstrip separated with 40nm oxide thickness from the epi-layer. The open ended transmission line of 4mm length has a real impedance at ¼ wavelength length, occuring already below 1GHz, which indeed corresponds to an effective dielectric constant of 400 as expected!

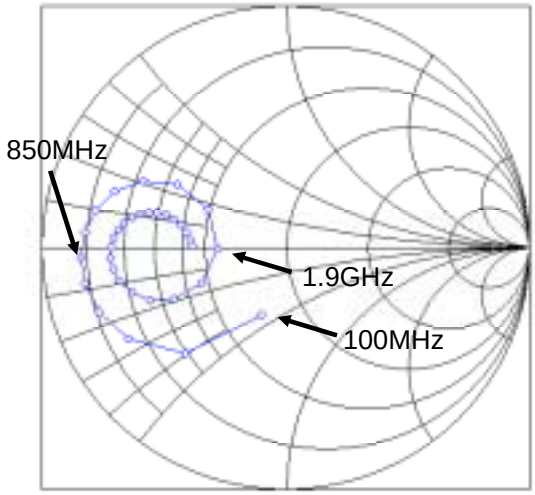


Figure 10: Smith card with S11 of a 4mm long open microstrip. Already below 1 GHz, 1/4 lambda is achieved (real impedance).

Such thin oxide thickness may be feasible in the near future. However, metal resistance unfortunately again is impeding low transmission line loss. This is because not only the wavelength but also the characteristic impedance of a slow-wave transmission line is lowered due to the high effective epsilon. As a result, the metal resistance must be very low, typically even an order of magnitude lower than in the previous section. Such low ohmic resistance layers are not available close to the Silicon epi-layer in the foreseeable future, unless superconductors are being introduced. Hence, unfortunately the slow-wave mode doesn't seem of much benefit. On the other hand awareness of the effect may be of crucial value, especially if dispersion of signal on transmission lines is a problem.

VI. Conclusions

With the ever increasing operating frequencies of CMOS ICs, transmission line design and modeling is becoming increasingly important. In this paper we explored possibilities to implement low loss transmission lines in a standard 0.18 micron CMOS process. Coupled coplanar transmission lines in odd mode seem a good choice because of substrate interference rejection. We found that characteristic impedance level between 30 and 100 ohm are possible and that losses below 1dB/mm are hard to achieve, mainly due to metal resistance. With the predicted increase of metal resistance [1] in downscaled technologies, metal losses are likely to become even more of a problem, unless a thick top metal layer remains available.

We also explored the potential of exploiting the so-called slow-wave propagation mode, which can occur if a sandwich of thin SiO2 and Si is used as dielectric between two conductors. It was shown that the wavelength indeed can be reduced drastically, allowing for on-chip quarter wavelength lines in the low GHz region. However, not only does the wavelength reduce, but also does the characteristic impedance. Hence metal resistance for low loss lines should be very low. As thick metal layers close to the Silicon epi-layer are not available, the application perspective of this slow-mode on CMOS chips seems limited. On the other hand, awareness of its existence is important, especially if dispersion of a signal during signal transfer is of critical importance.

VII. Acknowledgements

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VIII. References

[1] J. Davis et al, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century", Proceedings of the IEEE, Vol. 89, No. 4, pg. 305-324, April 2001.

[2] R. Ho, K. W. Mai, M. A. Horowitz, "The Future of Wires", Proceedings of the IEEE, Vol. 89, No. 4, pg. 490-504, April 2001.

[3] W. J. Dally, J. W. Poulton, "Digital Systems Engineering", Cambridge Press, 1998.

[4] T. H. Lee, S. S. Wong, "CMOS RF Integrated Circuits at 5GHz and Beyond", Proceedings of the IEEE, Vol. 88, No. 10, pg.1560-1571, October 2000.

[5] H. B. Bokoglu, "Circuits, Interconnections, and Packaging for VLSI", Addison-Wesley Publishing Company, 1990.

[6] B. Kleveland, T. Lee, S. Wong, "50-GHz interconnect design in standard silicon technology", IEEE MTT-S Intr. Microwave Symposium, June 1998.

[7] P. A. Ricci, "Microwave Enigineering", Prentice-Hall, ISBN 0-13-581711-0, 1988.

[8] H. Hasegawa, M. Frurukawa, H. Yanai, "Properties of Microstrip Line on Si-SiO2 System", IEEE Transactions on Microwave Theory and Techniques", Vol. MTT-19, No. 11, pg. 869-881, November 1971.

[9] U. Arz, D. F. Williams, D. K. Walker, H. Grabinski, "Asymmetric Coupled CMOS Lines— An Experimental Study", IEEE Transactions on Microwave Theory and Techniques", Vol. MTT-48, No. 12, pg. 2409-2414, December 2000.

[10] G. Ponchak, et al, "Low-Loss CPW on Low-Resistivity Si Substrates with a Miromachined Polyimide Interface Layer for RFIC Interconnects", IEEE Transactions on Microwave Theory and Techniques", Vol. MTT-49, pp. 866-870, No. 5, May 2001.