

# Thermal design issues and performance of microcalorimeter arrays at sub-Kelvin temperatures

M.L. Ridder<sup>a</sup>, M.P. Bruijn<sup>a</sup>, H.F.C. Hoovers<sup>a</sup>, A. Germeau<sup>a</sup>, N.H.R. Baars<sup>a</sup>, E. Krouwer<sup>a</sup>, J.J. van Baar<sup>b</sup>, R.J. Wiegerink<sup>b</sup>.

a) SRON National Institute for Space Research.  
Sorbonnelaan 2  
3584 CA Utrecht  
The Netherlands  
M.L.Ridder@sron.nl

b) MESA<sup>+</sup> Research Institute  
University of Twente  
P.O. Box 217  
7500 AE Enschede  
The Netherlands  
r.j.wiegerink@el.utwente.nl

## Abstract

We have produced 5 x 5 pixel arrays of microcalorimeters using bulk micromachining. Analysis of our data provides the thermal conductivity parameters of  $\text{Si}_x\text{N}_y$ , 1  $\mu\text{m}$  thick membranes at 100 mK. Moreover we find that the thermal transport at 100 mK in Si beams, with dimensions 1.25 mm x 0.35 mm x 35  $\mu\text{m}$  (length x height x width) is dominated by ballistic phonons with a mean free path of 110  $\mu\text{m}$ . These thermal parameters can be used for modelling future 32 x 32 pixel arrays. In addition we operated three pixels in a 5 x 5 array of microcalorimeters and find that the pixel to pixel reproducibility is very good. When used as an X-ray microcalorimeter individual pixels have a thermal decay time of 200  $\mu\text{s}$  and their energy resolution is between 6 and 7 eV for 5.89 keV X-ray photons.

## Keywords

Microcalorimeter, array, X-ray detector, thermal properties of  $\text{Si}_x\text{N}_y$  and Si, micromachining.

## INTRODUCTION

One of the future missions in spaced based astronomy, which is currently under study, is ESA's XEUS (X-ray Evolving Universe Spectroscopy) mission. XEUS will observe the early universe at X-ray wave lengths. One of the main instruments for XEUS is a high resolution imaging X-ray detector based on an array of cryogenic microcalorimeters: the narrow field 2, imager which is optimized for the energy range from 1 to 30 keV. Requirements for this detector are an energy resolution of 2 eV for 1 keV photons and 5 eV for 7 keV photons, a time constant smaller than 100  $\mu\text{s}$ , and high absorption efficiency (> 90% up to 7 keV). This imaging spectrometer will have 32 x 32 pixels [1].

In the first section of this paper we will briefly overview the essential components of a microcalorimeter as well as the performance of single pixel microcalorimeters. Next, the design and processing routes of arrays of microcalorimeters

will be addressed followed by the characterisation of a 5 x 5 pixel array configuration.

This characterisation will concentrate on two issues. First, we derive the material parameters that govern the thermal transport in  $\text{Si}_x\text{N}_y$ -membranes and Si at a temperature of 100 mK. We plan to use these parameters to design a full sized 32 x 32 pixel array for XEUS.

Second, we have operated three representative pixels of a 5 x 5 array and studied their performances as an X-ray microcalorimeter. These experiments are discussed.

## SINGLE PIXEL MICROCALORIMETERS

The basic physics and theoretical performance of a voltage-biased detector with a superconductor-to-normal phase transition thermometer (TES) are well established [2,3] and will not be repeated here. Figure 1 shows a schematic of the key components of a single pixel microcalorimeter.

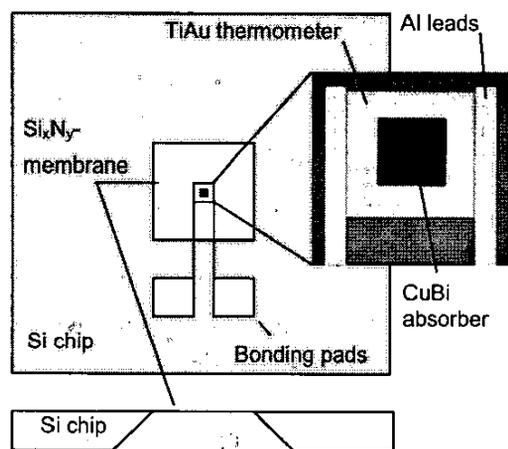


Figure 1. Schematic of a single pixel microcalorimeter (top view and cross-section). The inset is a photograph showing a lithographed microcalorimeter.

The TiAu TES is designed such that it has a critical temperature of 100 mK. At the center of the TES a CuBi absorber is lithographed. An absorber of this type is able to

meet the requirements of high absorption efficiency, and can be shaped such that a filling factor of 95% of the array can be achieved. The  $\text{Si}_x\text{N}_y$ -membrane provides a weak thermal coupling between the microcalorimeter and the heat bath (formed by the Si chip, with typical temperature of 20 mK). The microcalorimeter, which is voltage biased, self-heats to a stable set point in the superconducting transition at about 100 mK. In case an X-ray photon is absorbed the current through the device decreases and this change of current is measured with a low-noise SQUID (Superconducting Quantum Interference Device) current amplifier.

In recent years the focus has been on the optimization and the understanding of single pixel microcalorimeters. The best sensors, as produced and measured at SRON, have an energy resolution  $\Delta E_{\text{FWHM}} = 3.9$  eV for 5.9 keV photons, combined with an effective time constant of 150  $\mu\text{s}$ . Similar sensors equipped with a high (90%) absorption efficiency Bi absorber showed an energy resolution of 5.3 eV [4]. This level of performance is very close to the theoretical limit and is amongst the best-reported values in literature [5,6,7] and close to the XEUS requirements. The experience with these sensors forms the basis for the design of the array structures.

#### DESIGN AND PROCESSING ROUTES FOR MICROCALORIMETERS ARRAY

In developing arrays of TES microcalorimeter we identify a number of specific requirements such as: keeping the thermal cross-talk between pixels as low a possible, providing a proper heat bath for each pixel, and achieving sufficient mechanical robustness of the detector. The requirements should be met without sacrificing the optimal pixel to pixel performance in terms of energy resolution and thermal time constant. For the sensor array fabrication two different processing routes are being pursued.

The first option is based on bulk micromachining, where the support structure is formed by etching deep, vertical slots in the backside of a Si (110) wafer, using anisotropic wet etching. The resulting beams have a [111] orientation and a smooth surface, see fig. 2a. The typical dimensions of the Si beams in a 5 x 5 pixel array are 1.25 mm x 0.35 mm x 35  $\mu\text{m}$  (length x height x width). A good thermal conductance of the Si beams is essential to provide a proper heat bath to each of the pixels in the array. A micrograph of one of the arrays is presented in fig. 2b. This array is bulk micromachined. Because of limitations in our present characterization setup, not all pixels have been wired to the perimeter. Instead we have chosen to read out three representative pixels, one in the center, one at the edge and one in the corner of the array. The other positions are occupied by heaters strips which are connected in parallel so that bias power can be applied across the whole array.

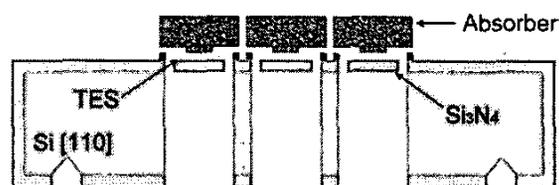


Figure 2a. Schematic side view of a pixel array, formed by bulk micromachining. Slots are wet etched into a  $\text{Si}_x\text{N}_y$  coated Si (110) wafer.

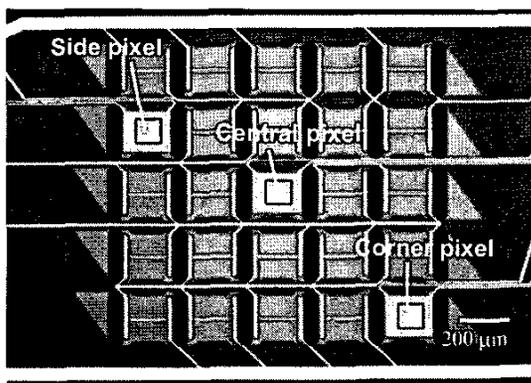


Figure 2b. Top view of an 5 x 5 pixel array on a perforated  $\text{Si}_x\text{N}_y$ -membrane using bulk micromachining. The three microcalorimeters are patterned and consist of a TiAu thermometer and a Cu absorber. Membranes are  $200 \times 180 \mu\text{m}^2$  and have a thickness of 1  $\mu\text{m}$ . They are suspended by 30  $\mu\text{m}$  wide legs. On the Si-beams (formed by wet-etching) the wiring is visible. Three representative pixels can be read out. The narrow, horizontal, lines seen at the remaining membranes, are heater elements.

The second processing route is based on surface micromachining. In that case a shallow cavity underneath each membrane is created by using a patterned poly-Si sacrificial layer. The cavity is emptied at the end of the production process, either by wet TMAH etching from the front side or through a dry etched access hole from the backside. The expected advantage of the surface micromachining route is that it results in a structure with better thermal conductance and lower thermal cross talk as the pixels are located much closer to the Si chip which is the heat bath.

Furthermore, the structure is mechanically more rigid and it opens the way for conducting the wiring under the pixel, see fig. 3a. Figure 3b shows a micromechanical prototype of a surface micromachined support structure.

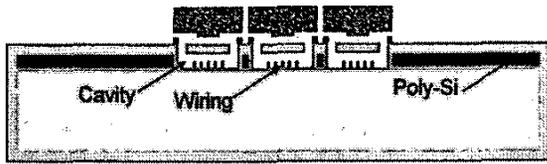


Figure 3a. Schematic side view of a pixel array, formed by the surface micromachining route. A poly-Si sacrificial layer is used to create a cavity underneath each pixel. Access to the cavity is either from top or bottom side (the latter possibility is not shown in this figure).

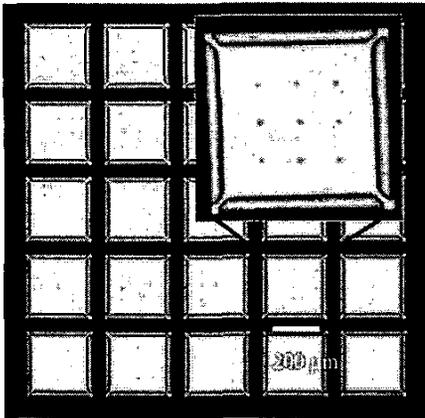


Figure 3b. Micromachined prototype of an 5 x 5 array produced using surface micromachining. The inset shows an enlarged image of a free hanging  $\text{Si}_x\text{N}_y$ -membrane, suspended by four support legs. The membranes are located above a 2  $\mu\text{m}$  deep cavity in the poly-Si layer.

For both the bulk micromachining option and the surface micromachining options, the TES and absorber are positioned on a slotted membrane and their production route is identical. The slots separate the membranes from each other and prevent thermal cross talk between pixels. The width of the  $\text{Si}_x\text{N}_y$ -legs between the membranes and the Si beam is used to tune the thermal coupling of the pixel to the heat bath. Figure 4 shows an exploded view of an array pixel. The CuBi absorber is mushroom shaped to allow for a high filling factor.

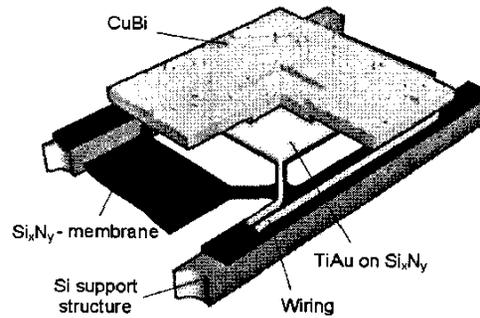


Figure 4. Basic layout of a sensor pixel. A mushroom-shaped CuBi absorber contacts the central part of a TiAu thermometer.

At this moment we have produced arrays along both routes but only lithographed TESs and absorbers on the bulk micromachined arrays.

#### ARRAY FABRICATION AND THERMAL CHARACTERISATION OF THE $\text{Si}_x\text{N}_y$ -MEMBRANE

We produced 5 x 5 pixel arrays with  $\text{Si}_x\text{N}_y$ -legs of 15, 30, 60 and 200  $\mu\text{m}$  width respectively, see figure 5.

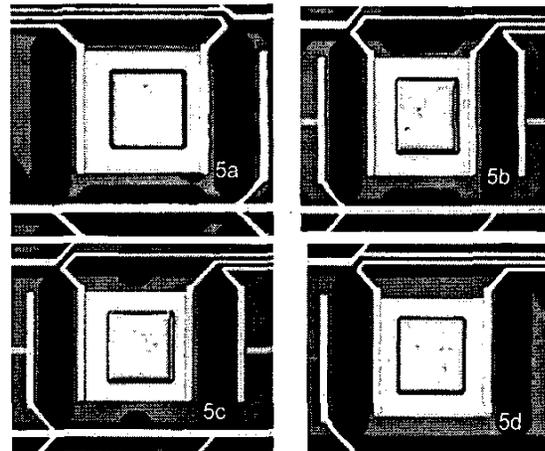


Figure 5 a-d. Micrograph of four array pixels with 15, 30, 60 and 200  $\mu\text{m}$  wide support legs. Note that these pixels do not have a mushroom shaped absorber.

For all four arrays we measured the Joule power  $P$  (power plateau) needed to bring the TES of the side pixel into its superconducting transition (i.e. a temperature  $T_c$ ). By measuring  $P$  as a function of the temperature of the heat bath ( $T_b$ ) the power law exponent  $n$  of the thermal transport in the  $\text{Si}_x\text{N}_y$ -membrane can be determined:  $P = K (T_c^n - T_b^n)$ . The prefactor  $K$  depends on the geometry of the  $\text{Si}_x\text{N}_y$ -leg. Figure 6 shows a representative measurement from which  $n$  and  $K$  are determined.

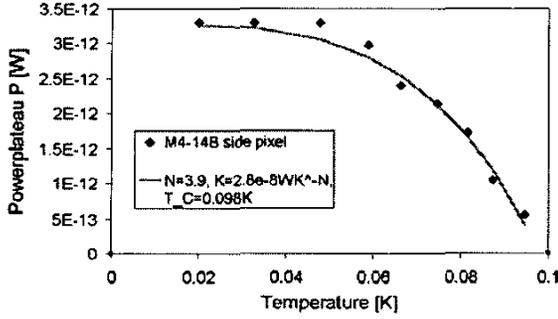


Figure 6. Power plateau measurements of a side pixel on a membrane with  $\text{Si}_x\text{N}_y$ -legs of  $60 \mu\text{m}$ . The electrical power  $P$  to bias a TES in its transition is measured as a function of the bath temperature  $T$ . Elementary fitting yields the thermal parameters  $n$  and  $K$  of the membrane.

Table 1 shows that the coupling of the pixels to the heat bath can be tuned (i.e. the magnitude of the power plateau changes) and summarizes the material parameters for the side pixel of each array. The value of  $n$  (listed in Table 1) of the four pixels averages close to 3.6. The pixels were fabricated in a single  $\text{Si}_x\text{N}_y$  batch so it is expected that  $n$  should be similar. An independent measurement of the thermal conductivity  $\kappa(T)$  on a closed membrane resulted in values of  $\kappa(T) = 0.016T^{2.8} \text{ Wm}^{-1}\text{K}^{-1}$  ( $n = 3.8$ ) which is in agreement with our values.

Table 1. The values of the power plateau and the material parameters  $n$  and  $K$  of the  $\text{Si}_x\text{N}_y$ -membrane obtained from measurements on the side pixel of arrays with different sizes of the  $\text{Si}_x\text{N}_y$ -legs.

Width of $\text{Si}_x\text{N}_y$ -legs [ $\mu\text{m}$ ]	Power plateau [pW]	$n$ [-]	$K$ [ $\text{W}/\text{K}^n$ ]
15	0.6	$3.3 \pm 0.4$	$2 \cdot 10^{-9}$
30	$1.8 \pm 0.2$	$3.5 \pm 0.3$	$6 \cdot 10^{-9}$
60	$3.4 \pm 0.3$	$3.9 \pm 0.4$	$30 \cdot 10^{-9}$
200	$4.6 \pm 0.3$	$3.5 \pm 0.4$	$20 \cdot 10^{-9}$

### PERFORMANCE OF THREE PIXELS IN ONE ARRAY

In addition to the extraction of the  $\text{Si}_x\text{N}_y$  and Si material parameters we have also studied the performance of three pixels in the array with the  $200 \mu\text{m}$  wide  $\text{Si}_x\text{N}_y$ -legs (the side, central, and corner pixel, respectively).

Table 2 lists the power needed to bias each of the three pixels, and the respective values of  $n$  and  $K$ .

The magnitude of the power plateau of all three pixels is identical within the measurement accuracy which indicates that all three pixels have a similar coupling to the heat bath (or, in other words, the Si-beams provide a sufficient thermal conductance). The values of  $n$  and  $K$  of the three

pixels agree and indicate the accuracy to which these parameters can be inferred from these measurements.

Table 2. Performance of three pixels in an array with  $200 \mu\text{m}$  wide  $\text{Si}_x\text{N}_y$ -legs.

pixel	Power plateau [pW]	$n$ [-]	$K$ [ $\text{W}/\text{K}^n$ ]	$\tau_{\text{eff}}$ [ms]	$\Delta E$ [eV]
Side	$4.6 \pm 0.3$	$3.5 \pm 0.4$	$20 \cdot 10^{-9}$	$0.2 \pm 0.05$	6.4
Central	$4.2 \pm 0.3$	$3.7 \pm 0.2$	$20 \cdot 10^{-9}$	$0.2 \pm 0.05$	7.4
Corner	$4.6 \pm 0.3$	$3.9 \pm 0.4$	$30 \cdot 10^{-9}$	$0.2 \pm 0.05$	-

Table 2 also list the effective time constant of all three pixels and the energy resolution at  $5.89 \text{ keV}$  of two of the pixels. We observe that the time constant is the same for all pixels, which is expected since the power plateaus and heat capacities are the same. The energy resolution of the two measured pixels is almost identical. The expected (theoretical) energy resolution of this detector is about  $5 \text{ eV}$  so there remains a discrepancy between the measured and expected energy resolution. Moreover, the thermal time constant is now  $200 \mu\text{s}$  whereas we are aiming for  $100 \mu\text{s}$  for the XEUS application. By further tuning of the coupling of the pixel to the heat bath, this number should, in principle, be reduced. From these performance data we conclude that the current performance in terms of the thermal time constant and energy resolution is close to the requirement for XEUS but that the full requirements are not yet met.

An ideal array detector should have pixels with an identical performance. Figure 7 shows the resistance versus temperature curves of three pixels in the array. As can be seen, all three pixels have a transition close to  $100 \text{ mK}$  and the width and shape of the transition is almost identical. These curves are measured at low current and indicate that, under these conditions, the TESs behave very similar.

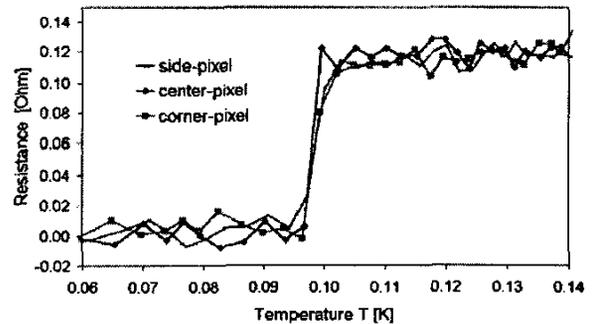


Figure 7. Resistance vs. temperature of a side-, corner- and center- pixel of a microcalorimeter array with  $200 \mu\text{m}$   $\text{Si}_x\text{N}_y$ -legs, measured at low current.

Figure 8 depicts the current voltage characteristic of the three pixels under biasing conditions. At voltages above about  $0.8 \mu\text{V}$  the TESs are in the normal state, and the

curves coincide. In this regime the slope of the current voltage curve is equal to the normal state resistance of the TES. At voltages below  $0.8 \mu\text{V}$  the TES are in the superconducting transition. We note that the curves are almost coincident and that the pixel to pixel performance under biasing conditions should be very similar.

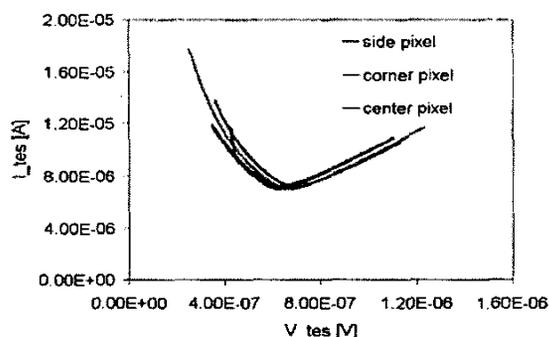


Figure 8. Current voltage characteristics of three pixels measured under typical biasing conditions.

#### Pixel performance with additional heat load

Although only three pixels are wired in the array with the  $200 \mu\text{m}$  wide  $\text{Si}_x\text{N}_y$ -legs, we can simulate the heat load imposed by the other pixel by running a current through the heaters that are placed on the other 22 membranes. We performed two types of measurements. The first measurement was the determination of the power plateau of the central pixel and a reference thermometer on the Si chip as a function of the bath temperature. The second measurement was to determine these power levels as a function of the power applied to (a subset of) the heaters on the other pixels. These data was used as input in a finite element model. Figure 9 displays the temperature distribution in the membrane, when 4 pW is dissipated in each heater and the center pixel is biased at 3.1 pW.

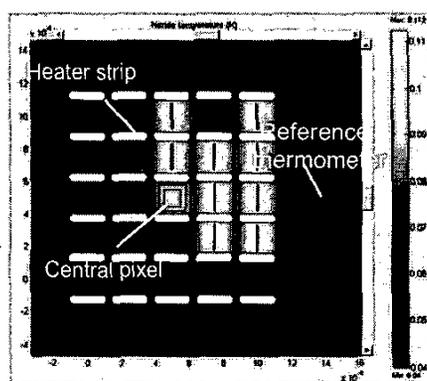


Figure 9. Finite element model of the temperature distribution in the  $\text{Si}_x\text{N}_y$ -membrane. Additional heat load is generated by 9 heaters strips. The central pixel and a reference thermometer on the chip can be biased.

By analyzing the finite element model we can make a good estimate of several thermal conductivity parameters:

- The coefficient of thermal conduction between the chip and the sample holder was  $0.025 \text{ W/K}^4\text{m}^2$ , assuming a Kapitza-like coupling. This is a rather low value, which can be improved by a better mounting technique.
- The coefficient and exponent of the thermal conductivity of the Si-nitride membrane. The best fit is  $\kappa = 0.0086T^{2.6} \text{ W/mK}$ .
- The thermal conductivity of the narrow Si support beams. Expressed in a mean free path [8] this value is  $110 \mu\text{m}$ , larger than the width, which indicates ballistic phonon transport in these beams.

Using the same finite element model we calculated that in case of cooling at the bottom of the Si-beams, an  $32 \times 32$  pixel array can be operated when each pixel dissipates 4.6 pW.

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