CMOS CIRCUITS FOR ANALOG SIGNAL PROCESSING

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Summary

Design choices in CMOS analog signal processing circuits are presented. Special attention is focussed on continuous-time filter technologies. The basics of MOSFET-C continuous-time filters and CMOS Square Law Circuits are explained at the hand of a graphical MOST characteristics representation.

Introduction

High packing density, high speed and low power consumption are the keys towards economically attractive signal-processing circuits. The high volume of digital CMOS circuits production, the high yield expectation and the demand for combined digital and analog circuits have challenged to exploit the possibilities of CMOS technology for analog applications.

A major problem in integrated continuous-time active RC filter applications is to achieve controlled, accurate and reproducible integration time constants. In SC-technology [1],[2] reproducible time constants are defined by means of capacitance ratios and the clock frequency. For switched capacitor circuit realization, also analog amplifiers [3]-[4] and switches had to be designed in CMOS technology. Together with the need for on-chip continuous-time prefiltering for anti-aliasing purposes, this has triggered the interest of analog designers to investigate the possibilities of analog continuous-time CMOS circuits for signal processing.

The shrinking of minimum dimensions towards the sub-micron range is profitable for cost and speed in digital circuits. For analog circuits, the functional dependence of analog CMOS circuits on device parameters such as channel length, limits the use of minimal dimensions. Nevertheless, analog circuits are attractive for signal processing if the input signals are analog, while simple processing is required and the output signal again has to be in analog form. In such cases the A/D and D/A conversion circuitry does not pay off. Also if digital signal processing acquires to much computational power at a high speed (particularly for real time processing at high signal frequencies), analog signal processing may offer an attractive alternative. In many cases, analog circuits consume less chip area and have a lower power consumption than their digital equivalents.

Analog signal processing circuits may be composed of function blocks, performing amplification and signal processsing functions like multiplication, summation, signal delay, squaring, square rooting or frequency filtering. This paper will concentrate on analog filter functions. In continuous-time CMOS filters the problem of reproducable time constants is solved by adaptive control of linearized MOST resistances or transconductances. One way is linearization of the MOST channel conduction in the linear mode, leading to the so-called MOSFET-C filters [5]. An approach to linearize transconductances is the application of CMOS Square-Law circuits to construct linear V-I converters and linear I-V converters with electronically controlled linear input resistance [6]. In both the MOSFET-C filters as well as in transconductance circuits, the time constants have to be electronically controlled via reference tuning circuits [7],[9]. This paper will review the basic circuit building blocks for continuous-time CMOS filters. Special attention is given to a graphical representation of the MOST I-V linearization techniques.

Simple MOST model

Graphical representation at the hand of a simple MOST model may be helpful for understanding the problem and its solution. Let $C_{ox}^{\square}$ represent the gate oxide capacitance per unit area and assume a constant channel-substrate depletion capacitance $C_d^{\square}$ per unit area. With the voltages referred to the common substrate, V_C denotes a channel voltage, which can vary between the source voltage V_S and the drain voltage V_D. Under the condition of onset of strong inversion, the gate threshold voltage $V_T(V_C)$ is related to the channel voltage V_C by:

$$(V_T(V_C) - V_{T0} - V_C)\, C_{ox}^{\square} = V_C\, C_d^{\square} . \qquad (1)$$

Defining $\alpha = (C_d^{\square}/C_{ox}^{\square} + 1)$, the threshold voltage $V_T(V_C)$ is:

$$V_T(V_C) = V_{T0} + \alpha\, V_C . \qquad (2)$$

The channel saturation voltage $V_{sat}(V_G)$ is the reverse relation:

$$V_{sat}(V_G) = (V_G - V_{T0})/\alpha . \qquad (3)$$

Conformably to the classical derivation of the MOST current voltage relation [10], the inversion charge density is expressed as:

$$Q_C^{\square}(V_G,V_C) = (V_G - V_T(V_C))\, C_{ox}^{\square} , \qquad (4)$$

and integration along the channel leads to the expression for the drain

current in the linear operation region:

$$I_D = K \{(V_G - V_{T0}) - (\alpha/2)(V_S + V_D)\}(V_D - V_S) , \quad (5)$$

or

$$I_D = (K/2\alpha)\{(V_G - V_{T0} - \alpha V_S)^2 - (V_G - V_{T0} - \alpha V_D)^2\} . \quad (6)$$

For $V_D > V_{sat}(V_G)$ this expression reduces to the saturated drain current,

$$I_{D,sat} = (K/2\alpha)(V_G - V_{T0} - \alpha V_S)^2 . \quad (7)$$

The currents of (6) and (7) are graphically represented by the shaded areas in figs. 1 a and b.

MOSFET-C filters

Tsividis et.al. [5],[7] have replaced the resistors in active RC-filters by MOS transistors, operating in the linear mode. For complete filter circuits the reader is referred to the literature. The resistance value of such transistors is electronically controlled via the gate voltage V_G. From (5) it follows for the MOST channel conductance:

$$G_C = K \{(V_G - V_{T0}) - (\alpha/2)(V_S + V_D)\} . \quad (8)$$

Graphically, the MOST current flowing in G_C is proportional to the shaded area in fig. 1a. For a linear resistance, this value must be signal independent, which requires $(V_S + V_D)$ being constant. With v_S and v_D denoting the signal components superposed on the bias voltages V_S and V_D, the signal current is proportional to the double-shaded area in fig. 2b. A more practical solution is the cancellation of nonlinearities by a fully balanced differential approach as represented in fig. 3b. Design problems are now moved towards the fully differential balanced amplifiers. Also differential balanced filter structures with single ended opamps have been described [8]. For filter applications, control of the resistance value is obtained by means of a tuning reference filter [7].

MOST Square - Law Circuits

A different approach for analog signal processing is achieved by exploiting the square-law characteristic of a MOST in the saturated mode [6],[11]. For a MOST in saturation with source connected to substrate the drain current of (7) reduces to:

$$I_D = (K/2\alpha)(V_G - V_{T0})^2 . \quad (9)$$

For the difference and sum currents of two identical MOS transistors M_1 and M_2, with gate-source voltages V_a and V_b, the following relations can be

derived [6]:

$$I_1 - I_2 = (K/2\alpha)\ (V_a + V_b - 2V_{T0})\ (V_a - V_b)\ , \qquad (10)$$

and

$$I_1 + I_2 = (K/4\alpha)\ \{(V_a + V_b - 2V_{T0})^2 + (V_a - V_b)^2\}\ . \qquad (11)$$

Under the condition of a constant sum $V_2 = (V_a + V_b)$ of the gate-source voltages, the current difference is linear proportional to the difference in gate voltage $(V_a - V_b)$, which can be written as $(2V_a - V_2)$. Based on this so-called *two-transistor linear and squaring principle* [11], several linear V-I and I-V converters have been developed. A graphical representation of the currents in the V-I converter of fig. 4a is given in fig. 4b. Filter functions operating up to several 100 Khz and with a dynamic range in the order of 60 dB for a 26th order filter have been demonstrated. [9]. Besides linear I-V and V-I converters, also non-linear circuits such as analog multiplier, current squaring and current divider circuits have been developed in this class [11]-[13].

MOST Scaling

As some of the analog design techniques rely on the quadratic MOST characteristics, they can not fully exploit the minimum dimensions, because of drain voltage dependent channel shortening effects. However, by clever design and balanced differential techniques, degradation of the ideal characteristics can be compensated [14]. The details and ultimate limits in this field are not yet clear. Modeling and characterisation of devices in the modern processes is of great importance. A new design challenge is also found in the combined bipolar and CMOS (BICMOS) processes, where the analog designer has a free choise for the type of each individual transistor.

Conclusion

The potential of analog CMOS circuits is not yet fully exploited. Several circuit design principles have recently been disclosed. Their ultimate potential in dynamic range and bandwidth will also depend on the ability for scaling in modern CMOS and BICMOS processes. Progress requires research in the complete field of the IC area, i.e. device modeling, electronic design principles, reproducibility, reliability and CAD for analog circuits. The advantage of combined processes like BICMOS, may push a new wave in analog integrated electronics. This may be exaggerated by the fact that in the advanced digital VLSI area, one is also forced to design at the limits of the analog perfomances of the basic digital circuits.

References

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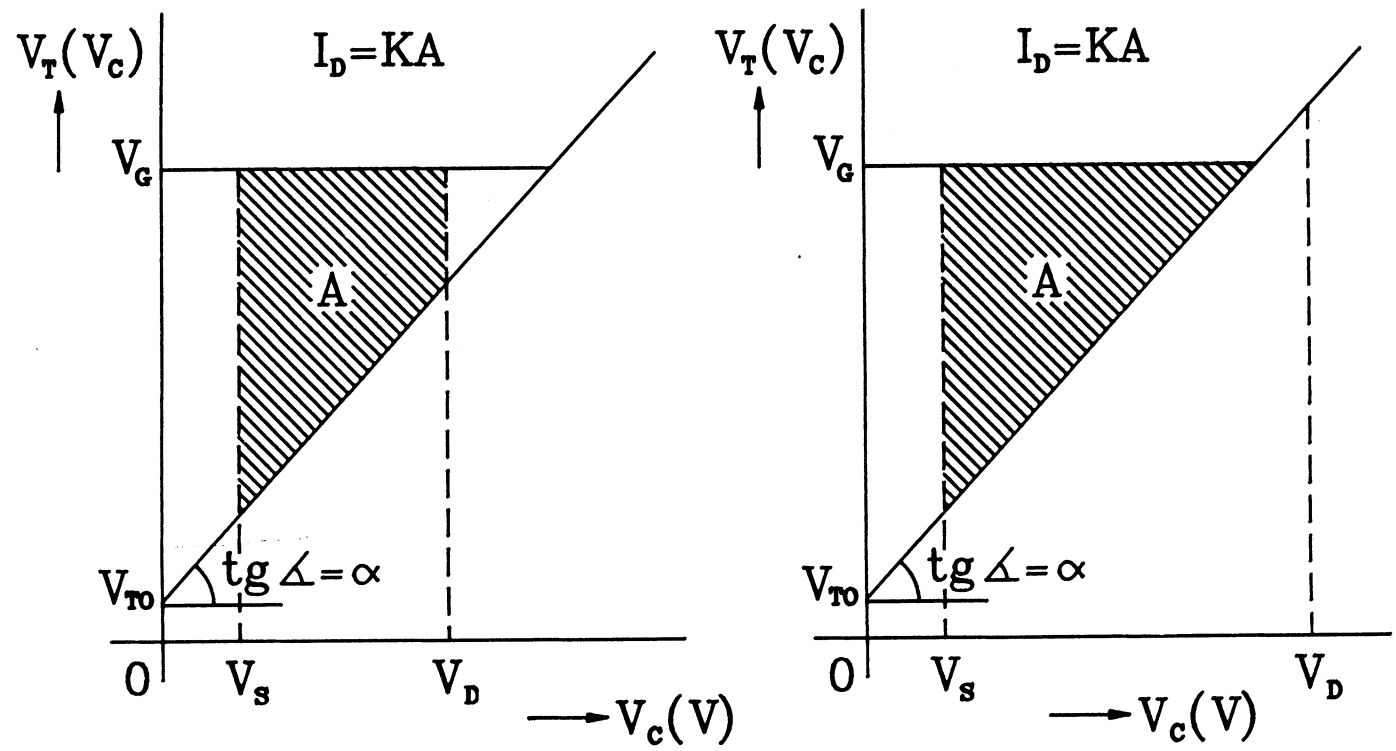

Fig. 1.a: The MOST current is proportional to the shaded area A. For $V_D < V_{D,sat}$ the MOST operates in the linear region.

b: For $V_D > V_{D,sat}$ the MOST is saturated. The proportionality constant $K = \mu C_{ox}^{\square} W/L$.

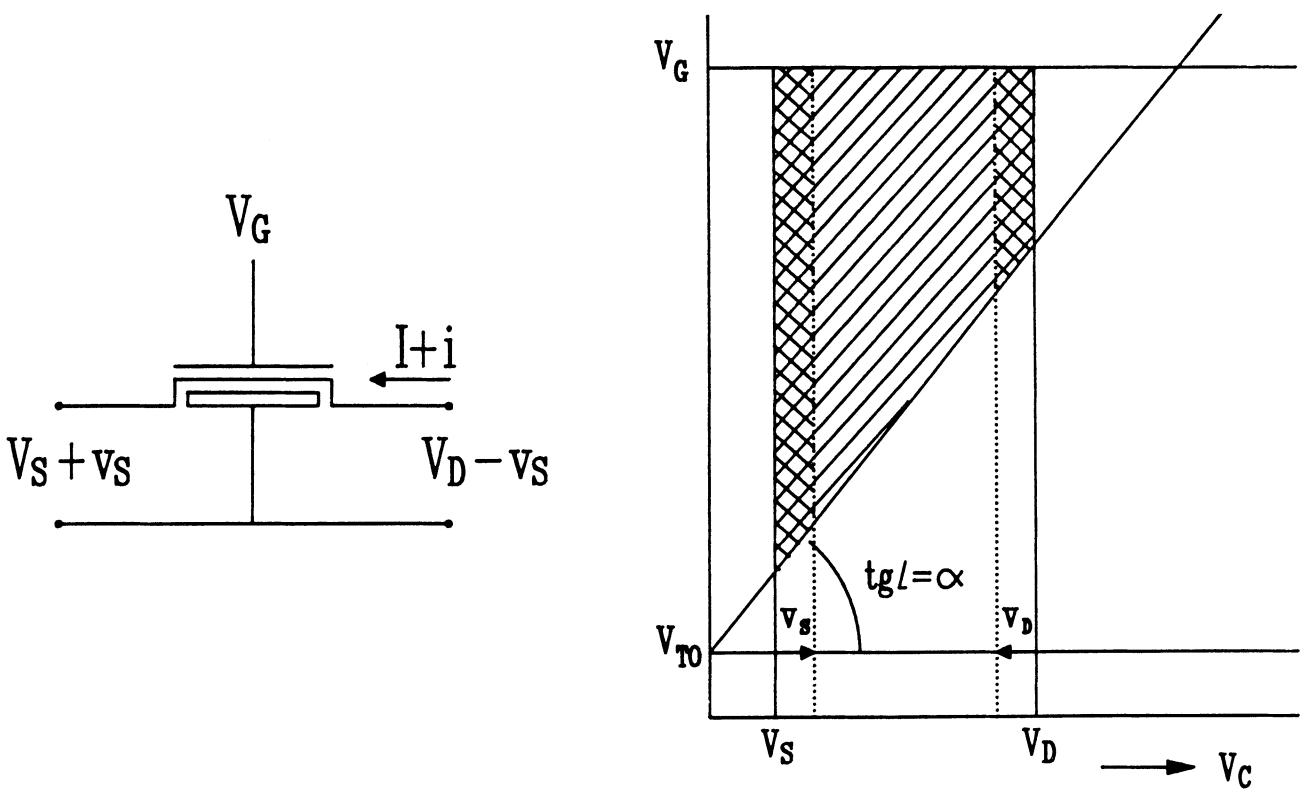

Fig. 2.a: MOST channel conductance under the condition $v_D = - v_S$.

b: The shaded area ▨ represents the bias current I; the shaded area ▨ represents the signal current: $i = - 2 v_S K \{ V_G - V_{TO} - \alpha (V_S - V_D) / 2 \}$.

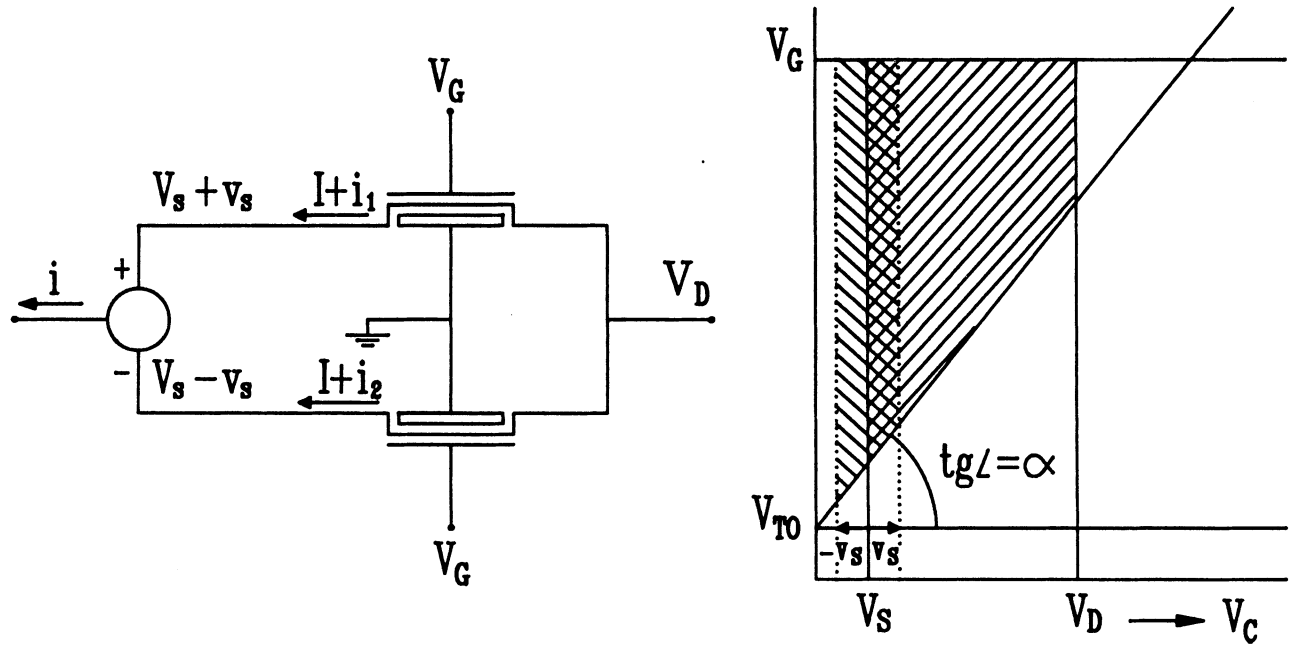

Fig. 3.a: Differential MOST source current $i = i_1 - i_2$, caused by a differential source voltage $2\ v_s$.

b: The shaded area ▨ represents the bias current I in each individual MOST; the shaded area ▨ represents the differential source current $i = -\ 2\ v_s\ K\ (\ V_G - V_{TO} - \alpha\ V_S\ )$.

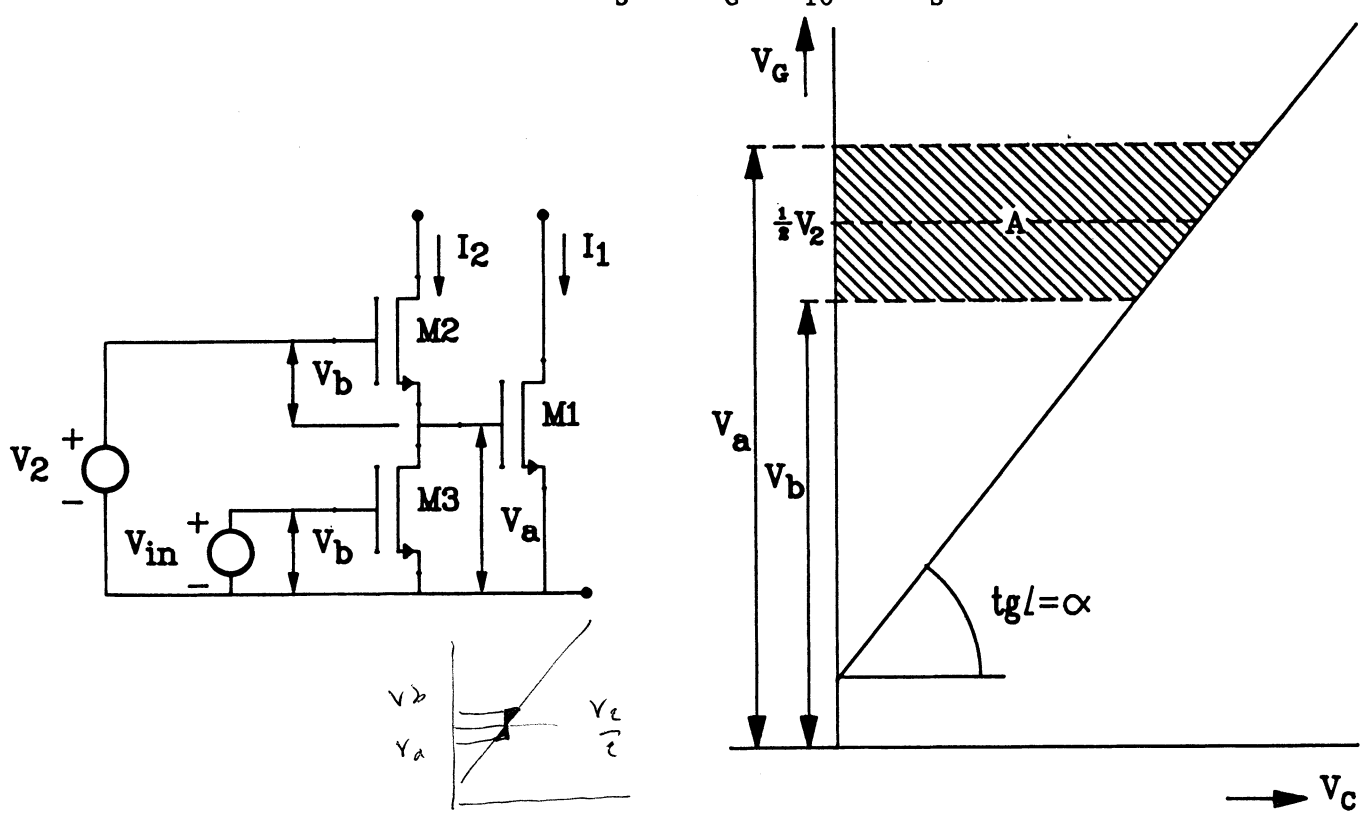

Fig. 4.a: The linear V-I converter. $M_1 = M_2 = M_3$.

b: The differential current is proportional to the shaded area ▨ : $I_1 - I_2 = K / \alpha\ (\ V_2 - V_{TO}\ )\ (\ V_a - V_b\ )$.