LOW POWER FOLDING A/D CONVERTERS

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Abstract

This paper describes the design and implementation of low power folding A/D converters in CMOS technology. The main advantage of the folding architecture is a reduced number of comparators by the implementation of an analog preprocessing circuit, resulting in a very compact, low power and high speed A/D converter. Design issues and low power implementation of the analog preprocessing and comparators are discussed. Two prototype folding A/D converters are presented, one for 5 V supply voltage and one for 3.3 V supply voltage. The first design operates at 70 MHz clock frequency and dissipates 110 mW. The 3.3 V low voltage design operates at 45 MHz and dissipates only 45 mW. Chip area is 0.75 mm^2 in 0.8 μm CMOS technology.

1 Introduction

For high speed applications different A/D converter architectures are available. In bipolar technology folding A/D converters have proven to be successful in the area of compact, very high speed data conversion [3] [4] [5]. Folding A/D converters are capable to fulfill the ever increasing demand for low power, embedded data conversion applications.
In this paper the implementation of a low power folding A/D converter in CMOS technology will be described. Major advantages of the implementation of folding techniques in CMOS technology are a high sample rate in combination with low power operation [1]. Furthermore, the chip area of this type of converter is extremely small.
First the folding A/D converter architecture is presented and compared to

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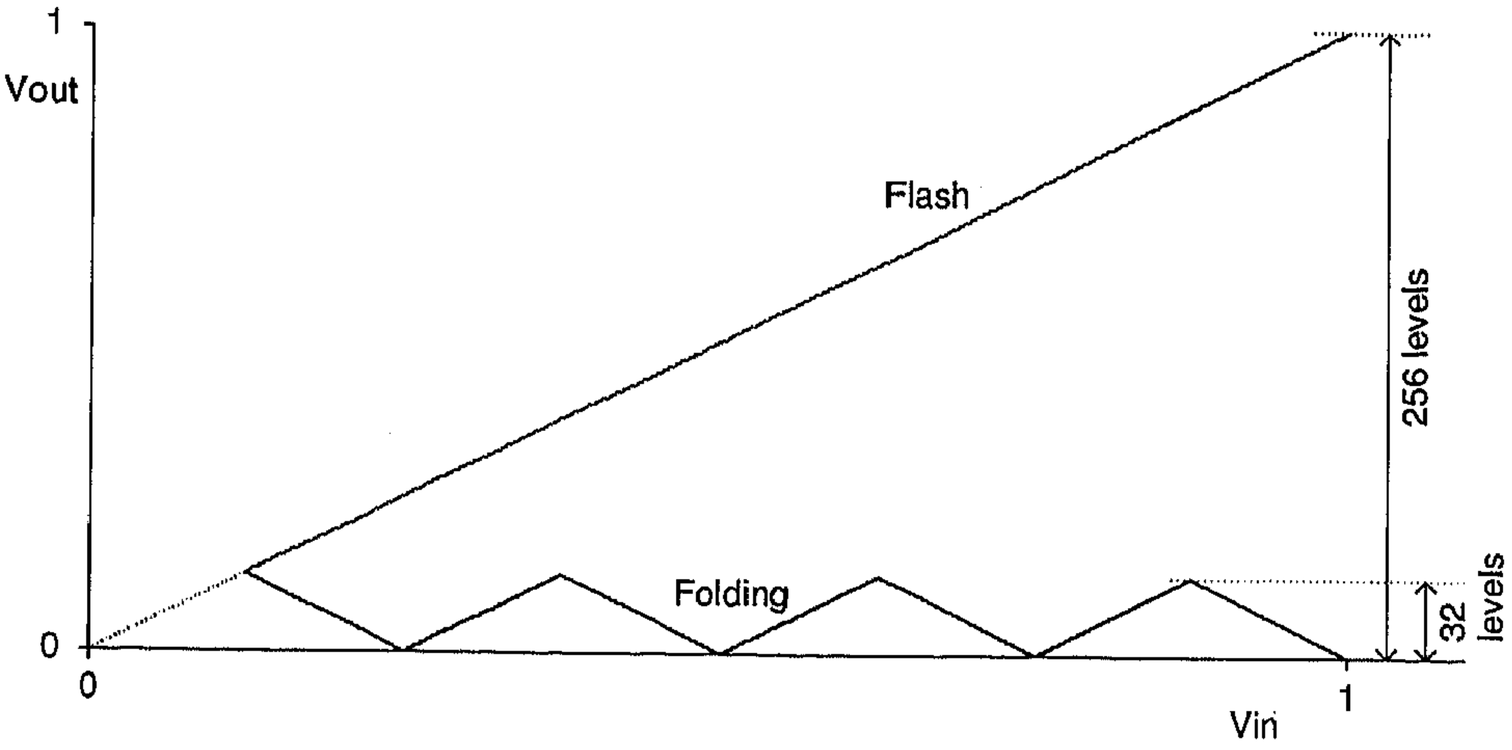

Figure 1: *Signal conversion in full flash and folding A/D converters*

a full flash architecture. Second, the generation of folding signals is described and it will be made clear that the analog preprocessing circuitry can be designed in such a way that a low power A/D converter can be constructed. Design issues for high speed low power A/D converters are discussed: power requirements of the reference ladder, sampling time uncertainty, sampling clock time uncertainty and bit error rate of the comparator are calculated.
Finally, experimental results of the designed prototype folding A/D converters are presented [1].

2 Basic folding concept

With an eight bit A/D converter the digital output code consists of $2^8 = 256$ codes, corresponding with 256 levels of the applied input signal. In a full flash A/D converter architecture $2^8 - 1 = 255$ comparators are needed for the analog to digital conversion of the input signal. By means of an analog preprocessing circuit in folding A/D converters the number of comparators can be reduced significantly.
Figure 1 shows the basic signals for full flash and folding A/D converters to be digitized by the comparators.
As mentioned, conversion to the digital code in a full flash A/D converter is performed by comparing V_{in} in 255 comparators C_1 to C_{n-1} with 255 reference voltages (figure 2).

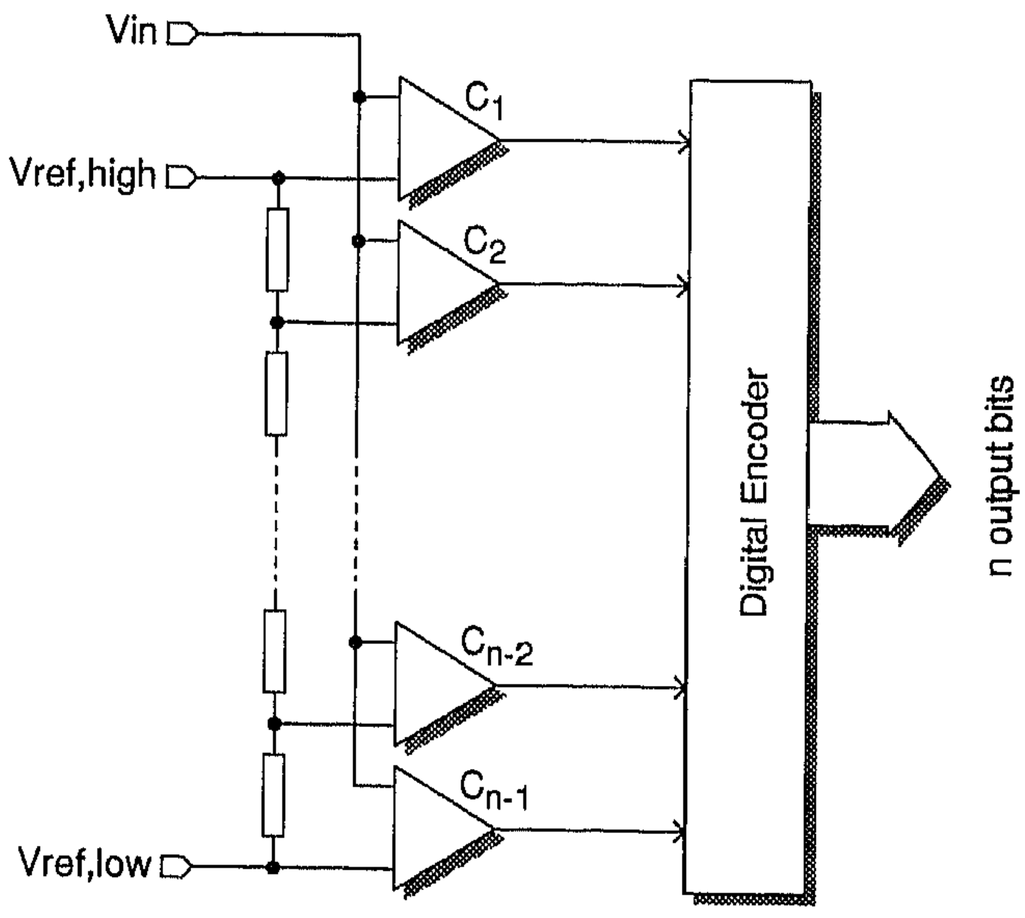

Figure 2: *Block diagram of full flash A/D converter*

A folding A/D converter generates the 256 level output code with a quite different approach. The triangle shaped line in figure 1 shows a derived *folded* version of the input signal. The amplitude of this folding signal is reduced to one eighth of the original input signal. The folding factor (F_F) of this signal equals 8. Obviously, the folding factor of a folding signal can be any integer number in the range

$$2 \leq F_F \leq 2^n, \tag{1}$$

with n the number of bits. A complete signal conversion can now be split up into two parts:

1. The *coarse* bits are derived from the folding edge corresponding to V_{in}. Since there are eight edges, in this example 3 bits of coarse information can be derived from this.

2. The *fine* bits are determined by the folding signal level. Only 5 bits = 32 signal levels have to be distinguished in the folding signal.

Drawback of the folding operation is an increased internal frequency compared to the full flash A/D converter. For a sine wave input signal the maximum internal frequency $f_{int,max}$ yields

$$f_{int,max} = \frac{\pi f_{in} F_F}{2} \tag{2}$$

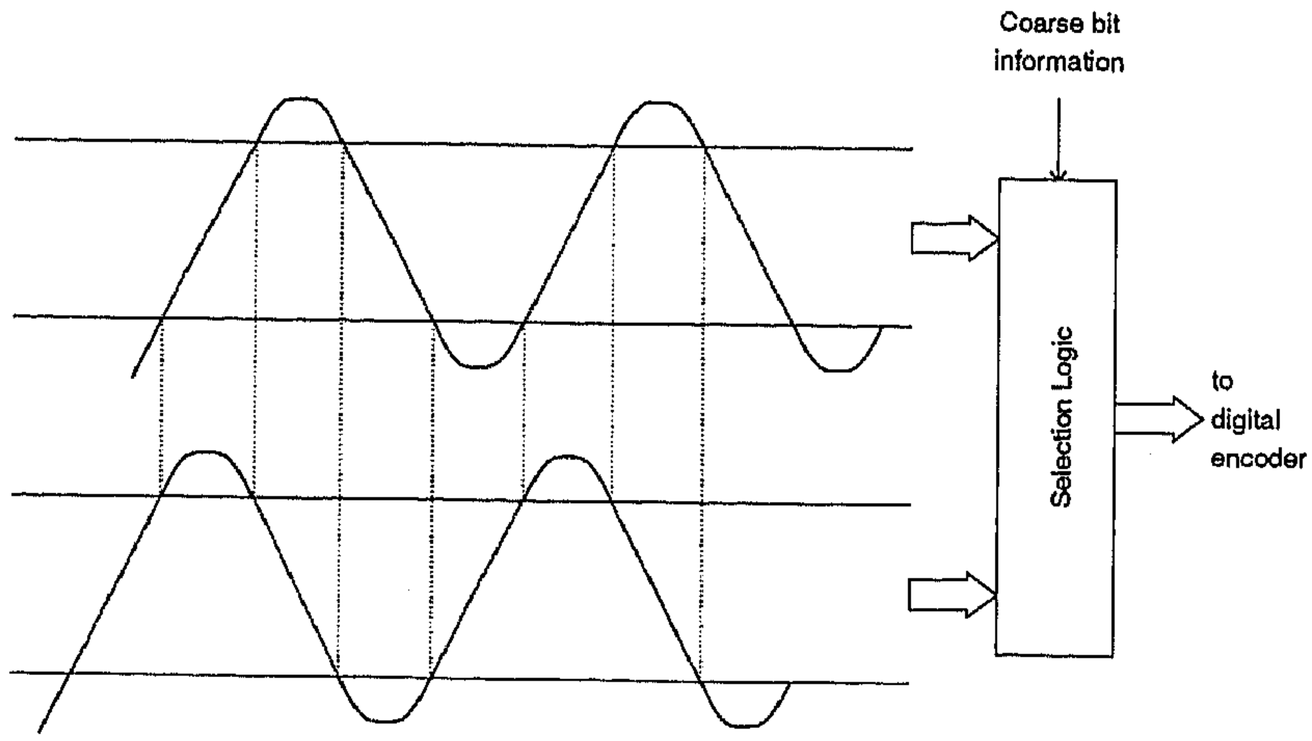

Figure 3: *Twin folding signal generation in a double folding system*

with f_{in} the input signal frequency. For high frequencies this will lead to rounding of the tops in the triangle shaped folding signal.

A double folding system in figure 3 could solve this high frequency rounding problem.
The information around the tops of the folding signals can be discarded. For any input signal, one of the two folding signals will be in its linear region. Assuming selection logic selects the right folding signal, in the linear region of a folding signal only 16 levels need to be distinguished. This process of adding folding signals to reduce the number of levels to be distinguished in a folding signal can be repeated. Finally, a system can be constructed with 32 folding signals (figure 4).
With 32 folding signals only one level has to be detected in a folding signal. In a differential or balanced folding signal, the only information to be gathered is whether it is positive or negative, so only the zero crossings in the folding signal are of main importance.
Figure 5 shows a block diagram of the folding A/D converter. The analog preprocessing block generates the required 32 folding signals. The fine flash A/D converter consists of only 32 comparators, one comparator per folding signal for zero crossing detection, and a 5 bits fine encoder. The coarse flash A/D converter contains another 8 comparators. Since the folding operation is time continuous, a sample and hold amplifier is not necessary for a folding A/D converter. However, addition of a sample and hold amplifier may enhance the analog input bandwidth of the folding A/D converter.

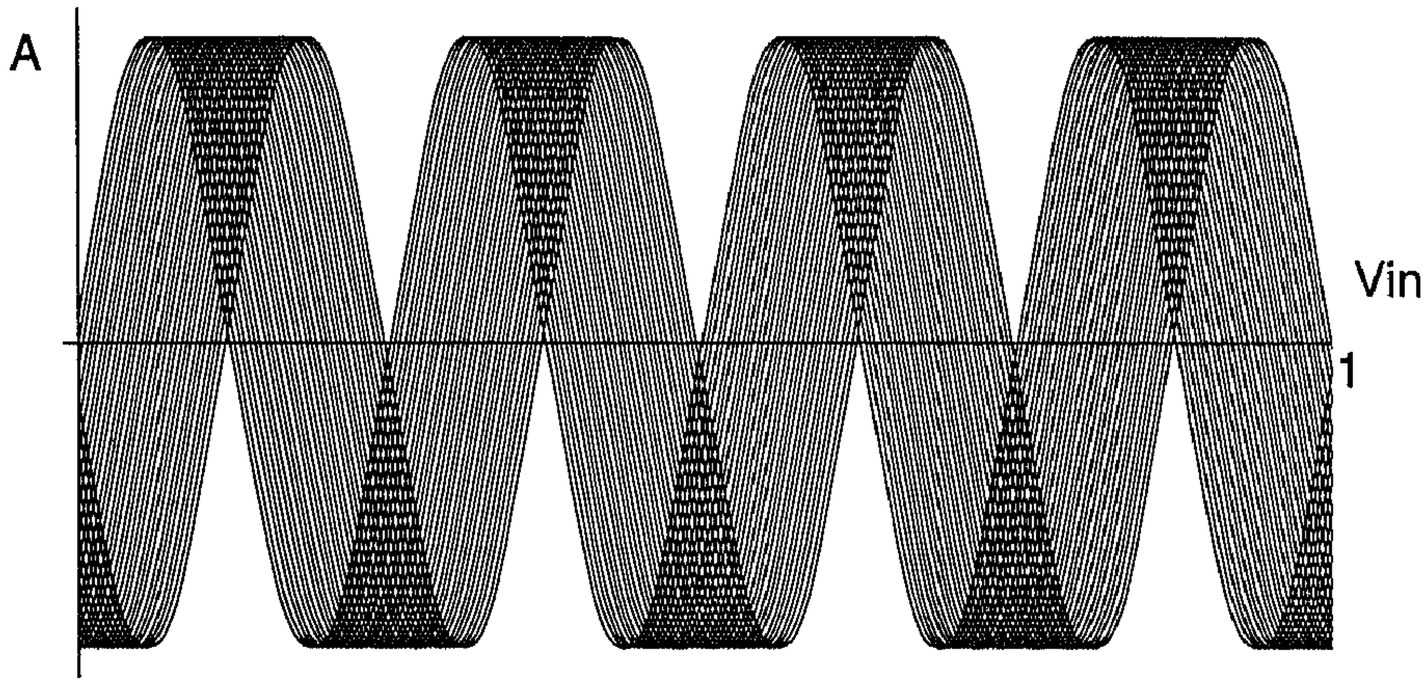

Figure 4: *Generation of 32 folding signals: only the zero crossings are of interest*

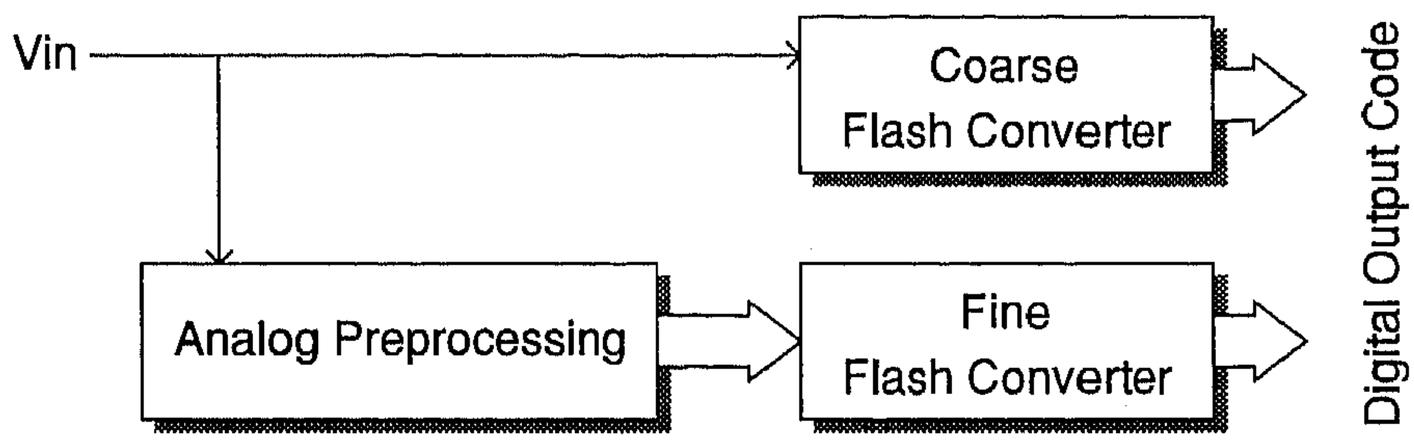

Figure 5: *Folding A/D converter block diagram*

Totally 40 comparators are necessary in this design, which makes a low power design possible. However, the reduction of comparator count has introduced the necessity of the analog preprocessing block. A power efficient implementation of the analog preprocessing is required to exploit the reduced comparator count.

3 Folding signal generation

In the prototype A/D converter four folding blocks generate four folding signals in parallel. Figure 6 shows the implementation of a folding block. It consists of 11 NMOS differential pairs with the drains of the odd and even numbered pairs cross-coupled. One of the differential pair transistors

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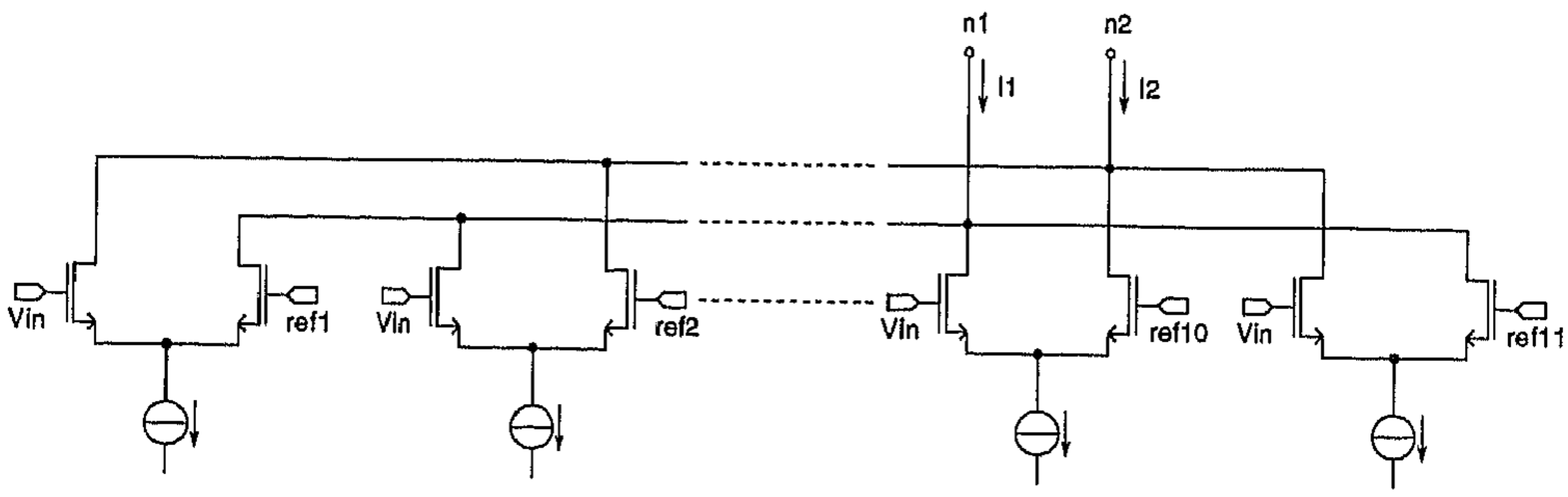

Figure 6: *Folding block implementation with current output* $I_1 - I_2$

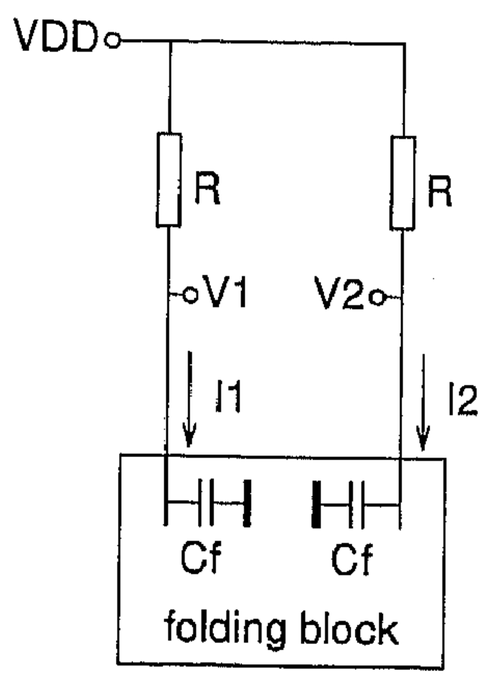

Figure 7: *Basic I to V conversion of folding current*

is connected to V_{in}, the other transistor is connected to a reference ladder tap. The output current $I_1 - I_2$ is a folding signal, shown in figure 4. The main part of the capacitance C_f at the nodes $n1$ and $n2$ is formed by the drain-substrate capacitances of the input differential pair transistors. Since the differential pair transistors have large areas (100 μm^2) for offset reduction [6], capacitances at nodes $n1$ and $n2$ are 1 pF. The frequency of the current $I_1 - I_2$ will have an increased maximum frequency according to equation 2.

For the resistive interpolation[1] of folding signals (section 4) the folding current $I_1 - I_2$ has to be converted to a folding voltage $V_1 - V_2$. Basic circuit for this I to V conversion is shown in figure 7.

[1]For current interpolation also an I to V conversion exists in the current mirrors.

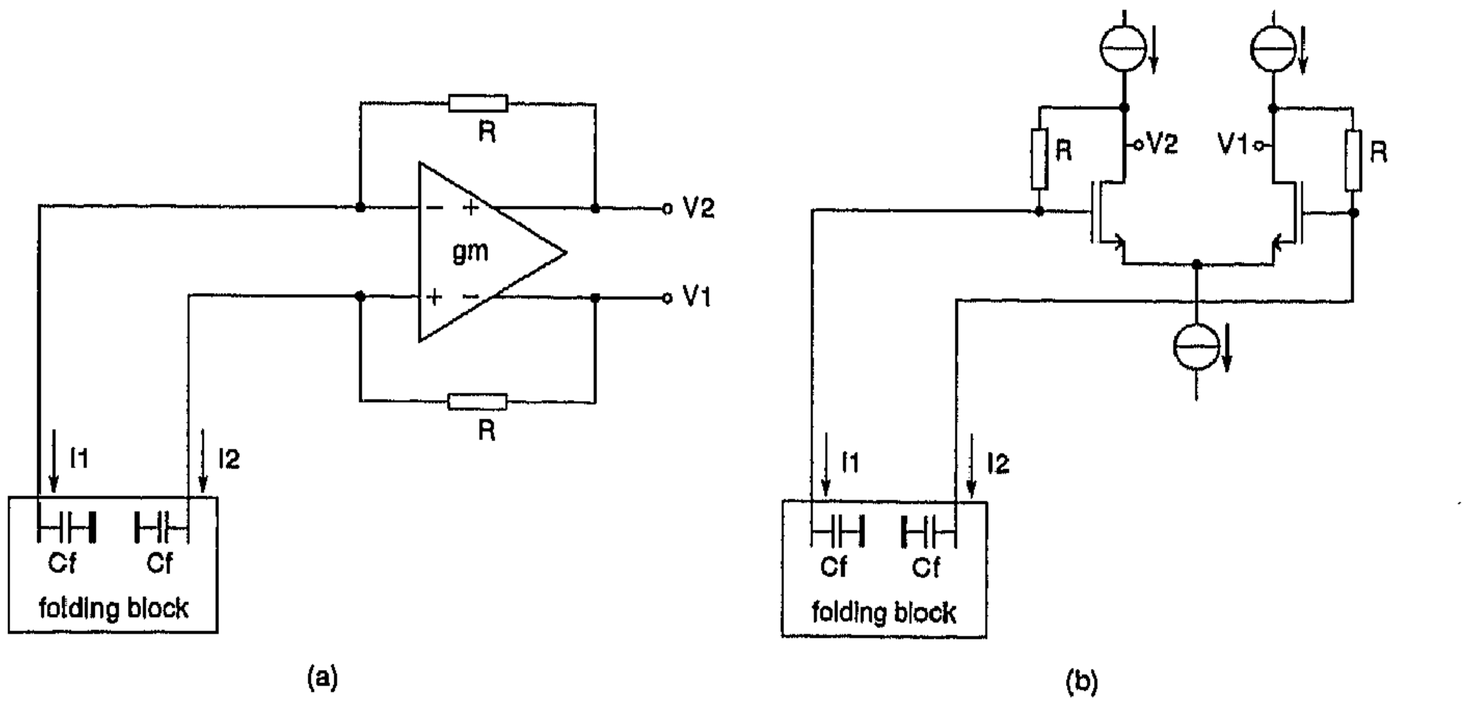

Figure 8: *(a) Improved I to V conversion of folding current (b) Circuit implementation*

The output voltage $V_1 - V_2$ yields

$$V_1 - V_2 = (I_1 - I_2)R, \tag{3}$$

the bandwidth f_{-3dB} of the system equals

$$f_{-3dB} = \frac{1}{2\pi RC_f}. \tag{4}$$

A large output voltage $V_1 - V_2$ is advantageous for the reduction of the influence of offsets in the additional preprocessing circuitry. However, this will lead to an unacceptable low analog input bandwidth, limited to only a few megahertz. A transimpedance amplifier, constructed with an OTA and feedback resistors R_1 and R_2 in figure 8(a), will improve the bandwidth available in the system. The output voltage $V_1 - V_2$ is according to equation 3. The bandwidth in the system equals

$$f_{-3dB} = \frac{g_m}{2\pi C_f}. \tag{5}$$

Comparing equations 4 and 5 makes clear that the available bandwidth is increased by a factor $g_m R$. In the designed prototype A/D converter $g_m R \approx 20$. Figure 8 (b) shows the implementation of the improved I to V conversion circuit.

Four folding blocks are operating in parallel with different offsets with respect to the input signal. The number of 32 folding signals could be

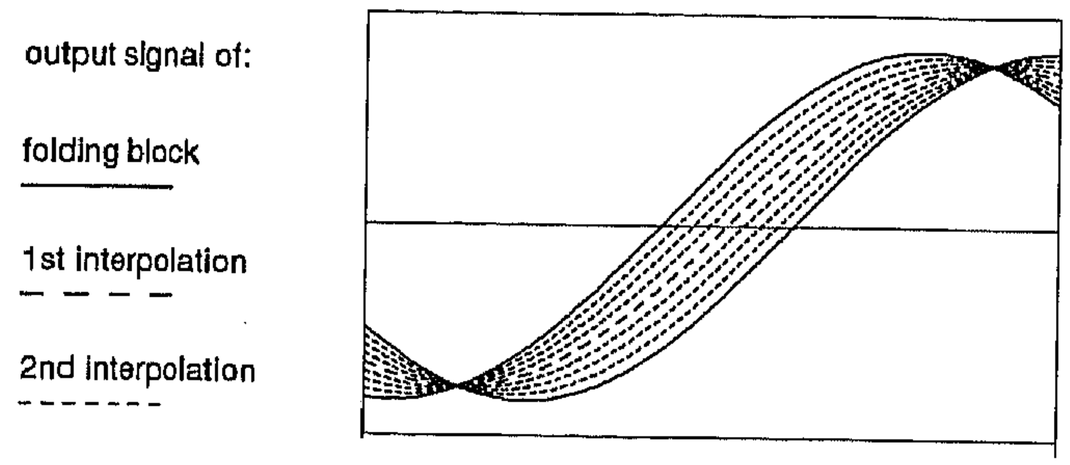

Figure 9: *Two stage implementation of folding signal interpolation*

generated by using 32 folding blocks in parallel. In this case however, the complexity and power of the folding system would not be less than the complexity of a full flash A/D converter. Resistive interpolation is a convenient way to generate the missing 28 folding signals since it costs no additional power. Total power dissipation of the analog preprocessing is determined by the generation of only four folding signals.

4 Interpolation of folding signals

In figure 10 a block diagram of the complete analog preprocessing including interpolation is shown. The interpolation of the missing 28 signals has been split up into a first 2 times interpolation stage and a final four times interpolation stage. The first interpolation stage doubles the number of folding signals to eight. The adjacent amplifier blocks increase the amplitude of the eight folding signals. Finally 32 folding signals are available. Interpolation signals are shown in figure 9.
Interpolation is a very low cost way to increase the number of folding signals. Furthermore, resistive interpolation helps in reducing differential non-linearity (DNL) errors [8]: a single folding signal is influenced by its neighboring folding signals as well. This results in an averaging of offset errors.

A single ended version of the first interpolation stage is shown in figure 11. The output signals of the folding blocks are F_1, F_2, F_3 and F_4. The output impedance of the folding blocks is modeled by the resistors R_o. For instance, signal V_5 can be expressed as a function of F_2, F_3, F_4, R_o and R_i:

$$V_5 = \frac{R_o(F_2 + F_4)}{Q} + \frac{(2R_o + R_i)F_3}{Q}, \tag{6}$$

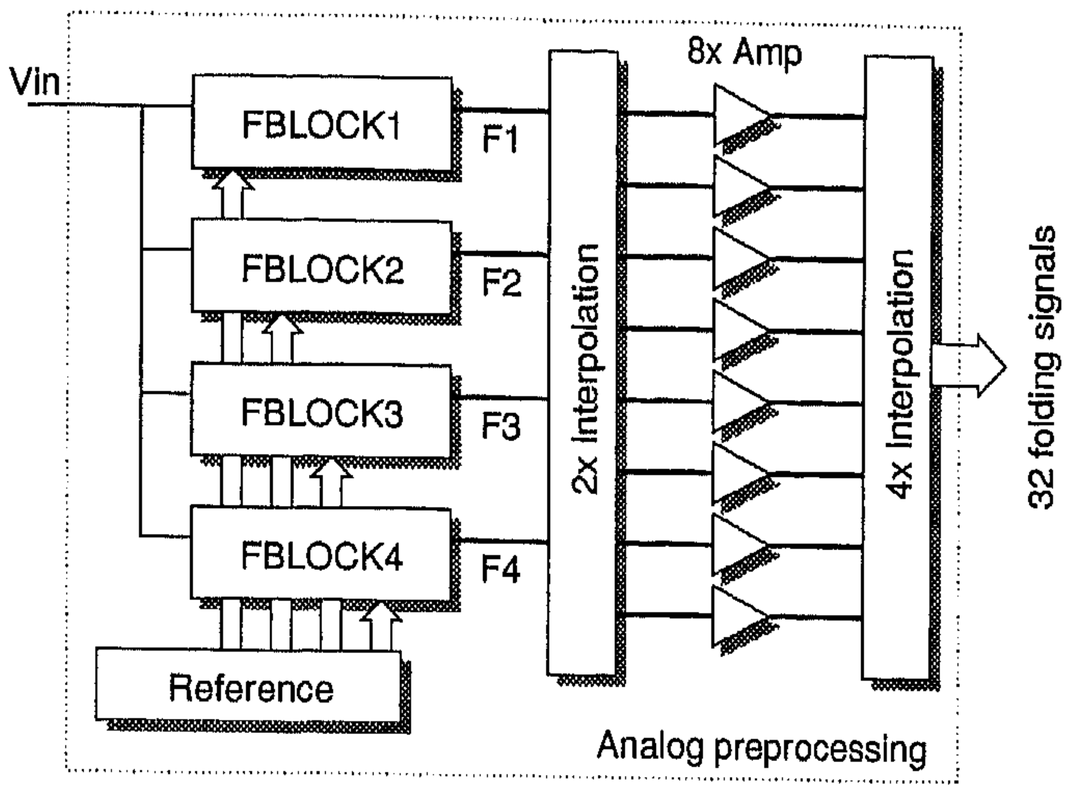

Figure 10: *Complete analog preprocessing with interpolation*

with

$$Q = 4R_o + R_i + \frac{2{R_o}^2(2R_o + R_i)}{{R_i}^2 + 2R_iR_o}. \tag{7}$$

The DNL error correction factor ECF is defined as:

$$ECF = \frac{DNL_{corrected}}{DNL_{uncorrected}}. \tag{8}$$

From equations 6 and 7 it can be derived that ECF yields:

$$ECF = \frac{R_o + R_i}{Q}. \tag{9}$$

For this A/D converter the interpolation resistors ($\frac{R_i}{2}$) have a value of 1200 Ω. The output impedance of the folding blocks equals 250 Ω. This results in

$$ECF = 0.77, \tag{10}$$

a DNL improvement of 23%. Since the interpolated folding signals are averaged between two of the input folding signals F, final DNL will be improved additionally by a factor 2.

A similar derivation can be done for the second interpolation stage.

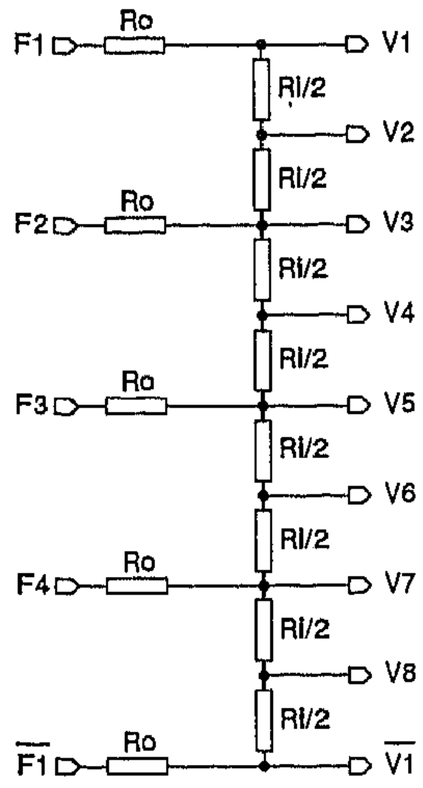

Figure 11: *Single ended representation of the first interpolation stage*

5 Architecture overview of converter

A block diagram of the complete folding A/D converter is shown in figure 12.

The analog preprocessing block is implemented according to figure 10. 32 fine comparators generate the 5 fine bits. One of the folding signals represents the MSB-2 bit. The output signals of the 8 coarse comparators are synchronized with this MSB-2 bit and deliver the MSB and MSB-1 bits. Synchronization of coarse and fine comparators is necessary due to the delay of the analog preprocessing. Latency of the folding A/D converter

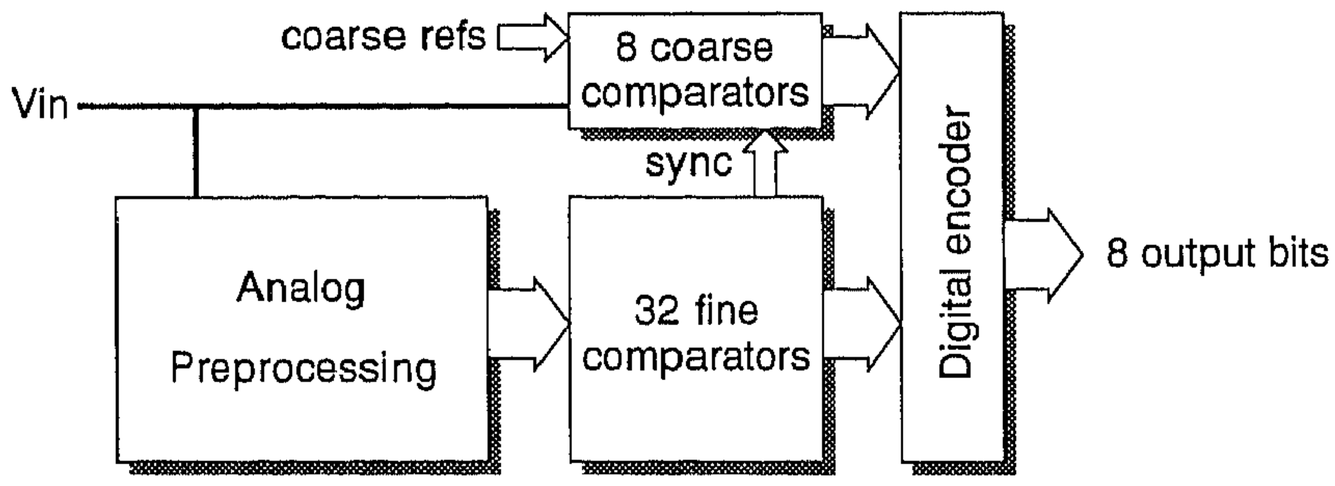

Figure 12: *Block diagram of folding A/D converter*

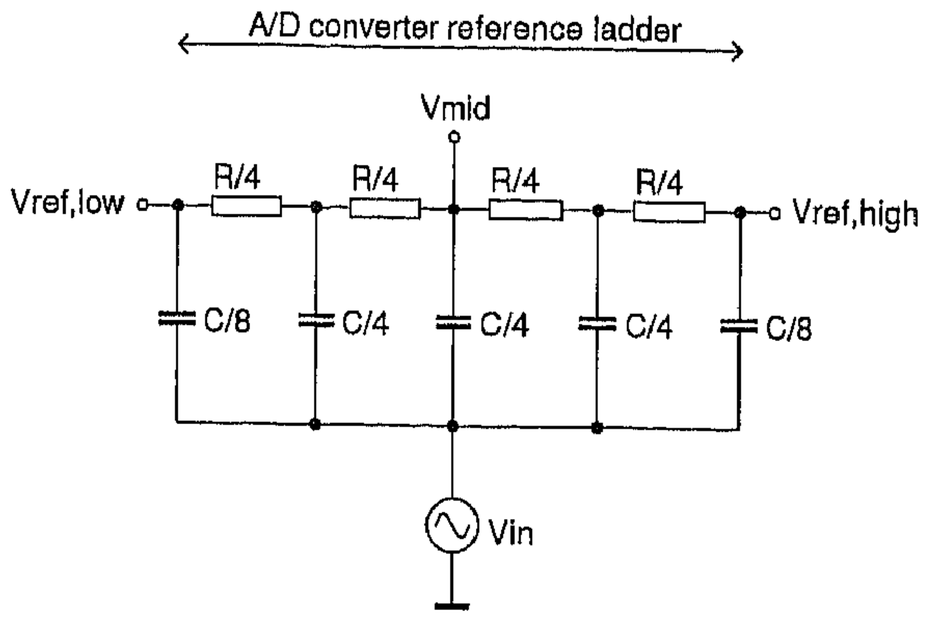

Figure 13: *Model of A/D converter reference ladder*

is 1.5 clock cycles. This is clearly an advantage of the folding architecture compared to SAR, pipeline or multi-step A/D converter architectures.

6 Design issues for high speed low power

6.1 Power requirements of the reference ladder

A folding block needs 11 equidistant reference voltages to determine the zero crossings of the folding signal; total number of reference voltages to be generated is 44. Feed through of the input signal via the gate-source capacitances of the differential pair transistors will result in deterioration of the reference voltages. Zero crossings of the folding signals will shift and this will lead to harmonic distortion in the analog preprocessing circuit. If an upper bound to the shift of the reference voltages is defined, the minimum required reference ladder impedance can be calculated.
A basic model of the reference ladder is shown in figure 13.
Total reference ladder impedance equals R, divided in four sections of $\frac{R}{4}$ each. The total coupling capacitance between input and reference ladder of the 44 differential pairs of the four folding blocks equals C, divided in three section of $\frac{C}{4}$ each and two sections of $\frac{C}{8}$. Obviously, this a simplified model, but by simulation it can be shown that the deterioration of V_{mid} matches to the calculated deterioration in this model. For calculations half of the model in figure 13 can be used (figure 14).
V_{in} will feed through on V_{mid} according to:

$$\frac{V_{mid}}{V_{in}} = \frac{\alpha(\alpha + 32)}{\alpha^2 + 32\alpha + 128}, \tag{11}$$

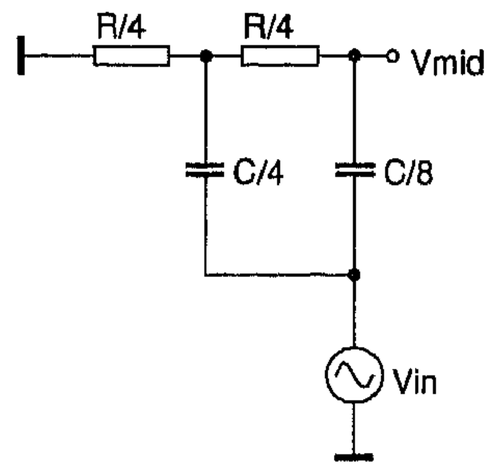

Figure 14: *Simplified calculation model of A/D converter reference ladder*

with

$$\alpha = \pi f_{in} RC \tag{12}$$

in which f_{in} is the input signal frequency. In practice a valid assumption for α is

$$\alpha << 1. \tag{13}$$

In this case equation 11 can be simplified to

$$\frac{V_{mid}}{V_{in}} = \frac{\pi}{4} f_{in} RC. \tag{14}$$

The required reference ladder impedance can be derived from equation 14:

$$R = \frac{\frac{4}{\pi}\frac{V_{mid}}{V_{in}}}{f_{in}C}. \tag{15}$$

In the above expression $\frac{V_{mid}}{V_{in}}$ gives the allowed maximum feed through at the middle tap of the reference ladder. For instance, in the eight bit A/D converter $\frac{V_{mid}}{V_{in}} = \frac{1}{256}$ results in a maximum reference ladder deterioration of 1 LSB. With n the number of bits of the converter, ϕ the allowed feed through in LSB, equation 15 can be rewritten as

$$R = \frac{4\phi}{\pi 2^n f_{in} C}. \tag{16}$$

Total effective feed through capacitance C is determined by the number of differential pairs (44) and the number of differential pairs for which yields

$$V_{in} > V_{ref,i} \tag{17}$$

with $V_{ref,i}$ the reference voltage of a single differential pair. The minimum required reference ladder power P_{LAD} equals

$$P_{LAD} = \frac{2^{3n}(\alpha V_{LSB})^2 f_{in} C \pi}{4\phi}, \tag{18}$$

in which α represents the overlap of the reference ladder over the actual input range of the A/D converter. This overlap is necessary for symmetry reasons. V_{LSB} is the input voltage for one least significant bit. As an example, with $f_{in} = 10$ MHz, $C = 2$ pF, $\phi = 1$ LSB, $\alpha = 1.5$, $V_{LSB} = 5.5$ mV:

$$R = 250\ \Omega \tag{19}$$

$$P_{LAD} = 18\ \text{mW}. \tag{20}$$

The reference ladder voltage for the 3.3 V design, including overlaps for symmetry, equals 2.1 V. Actual A/D converter input range equals 1.4 V for this design.

6.2 Sampling time uncertainty

The digital counterpart of the analog input signal will have additional errors if the sampling in the comparators of the A/D converter is done with a timing uncertainty [2]. The maximum allowed sampling time uncertainty will be calculated for a sine wave input signal (figure 15). Suppose a sampling time uncertainty Δt, the amplitude variation of the sampled input signal will be ΔA. Allowed maximum peak-to-peak value for ΔA equals the quantization step q (1 LSB) in the converter:

$$q = \frac{2X}{2^n}, \tag{21}$$

with n the number of bits of the A/D converter and X the amplitude of the input signal.
Assume a sine wave input signal, $V_{in} = X\sin(\omega t)$. The sampling time uncertainty Δt is given by:

$$\Delta t = \frac{\Delta V_{in}}{X\omega\cos(\omega t)} \tag{22}$$

and with $\Delta V_{in} = q$, f_{in} the input signal frequency and $\omega = 2\pi f_{in}$:

$$\Delta t = \frac{q}{X\omega\cos(\omega t)} = \frac{2^{-n}}{\pi f_{in}\cos(2\pi f_{in} t)}. \tag{23}$$

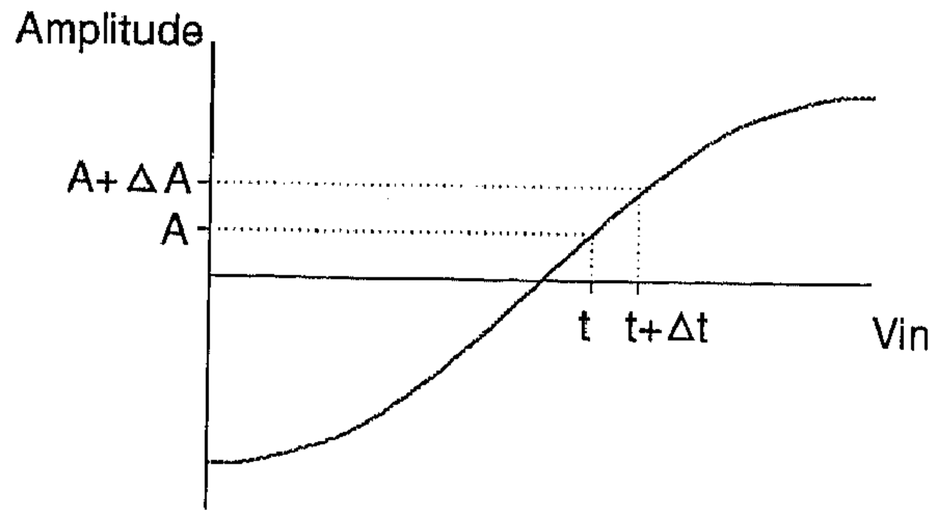

Figure 15: *Timing uncertainty for sine wave input signals*

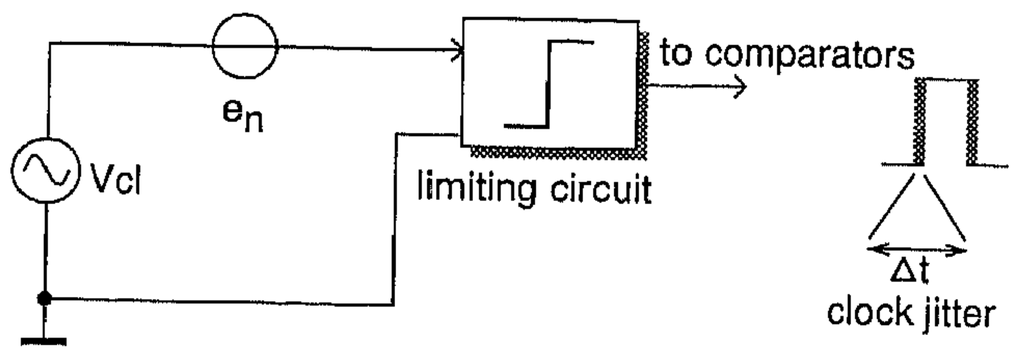

Figure 16: *Calculation model for short term clock jitter*

Maximum Δt is reached at the zero crossing of the input signal. At that moment $\cos(2\pi f_{in} t) = 1$:

$$\Delta t_{max} = \frac{2^{-n}}{\pi f_{in}}. \tag{24}$$

For an 8 bit A/D converter and $f_{in} = 10$ MHz, Δt_{max} becomes 125 ps. The clock buffer driving the comparators must be designed with this timing uncertainty constraint.

6.3 Sampling clock time uncertainty

Figure 16 shows a model for calculation of the short term clock time uncertainty.
Noise of the limiting circuit is modeled by source e_n. Clock input $V_{cl} = Y \sin(\omega t)$. ΔV_{cl} is given by:

$$\Delta V_{cl} = Y \omega \cos(\omega t) \Delta t. \tag{25}$$

Maximum value of Δt is given by equation 24. Assuming mostly thermal

noise in the limiting circuit gives

$$\Delta V_{cl} = e_n = \sqrt{4kTR_N\Delta f}. \tag{26}$$

In this equation R_N is the equivalent noise resistance of the limiting circuit. Equations 25 and 26 give the R_N necessary as a function of the clock frequency $f_{cl} = \frac{\omega}{2\pi}$ and amplitude Y and the maximum allowed Δt. The equivalent noise bandwidth Δf is assumed $5\pi f_{cl}$ for a first order limiting circuit and 10 harmonics of the base frequency in the output square wave. R_N is given by:

$$R_N = \frac{\pi f_{cl} Y^2 {\Delta t_{(rms)}}^2}{5kT}. \tag{27}$$

From the above it has become clear that the bandwidth in the clock circuit has to be about $5\pi f_{cl}$. If a differential pair structure[2] with transconductance gm_i is assumed as limiting circuit, gm_i can be expressed as a function of the gain in the limiting circuit A_s, the load capacitance of the comparators C_L and the clock frequency f_{cl}:

$$gm_i = 10\pi^2 A_s C_L f_{cl}. \tag{28}$$

Equations 27 and 28 put a demand on the transconductance of the limiting circuit. The most severe expression determines the transconductance necessary in the A/D converters clock circuit.

6.4 Comparator implementation and bit error rate

A comparator implementation is shown in figure 17. The master part of the comparator consists of a folded cascode input stage, loaded with a latch pair. Clock signal is C_m. In the reset phase, $C_m = VDD$, the input signal is pre-amplified. The gain A_{PRE} is determined by the transconductances of the input differential pair transistors N_1, N_2, latch pair transistors N_3, N_4 and clock switch N_5:

$$A_{PRE} = \frac{gm_{N1}}{2gm_{N5} - gm_{N3}}. \tag{29}$$

The latch phase is initiated with a falling edge of clock signal C_m. Transistors N_3 and N_4 will form a positive feedback loop.
The bit error rate of the comparator is defined as the probability of a meta stable state (figure 18(b)) that occurs during the latch phase of the comparator. A meta stable state results in an undecided output signal of the comparator. The digital encoder of the A/D converter may encode a wrong output code in this case. Therefore, a bit error prediction is necessary to ensure proper operation of the A/D converter.

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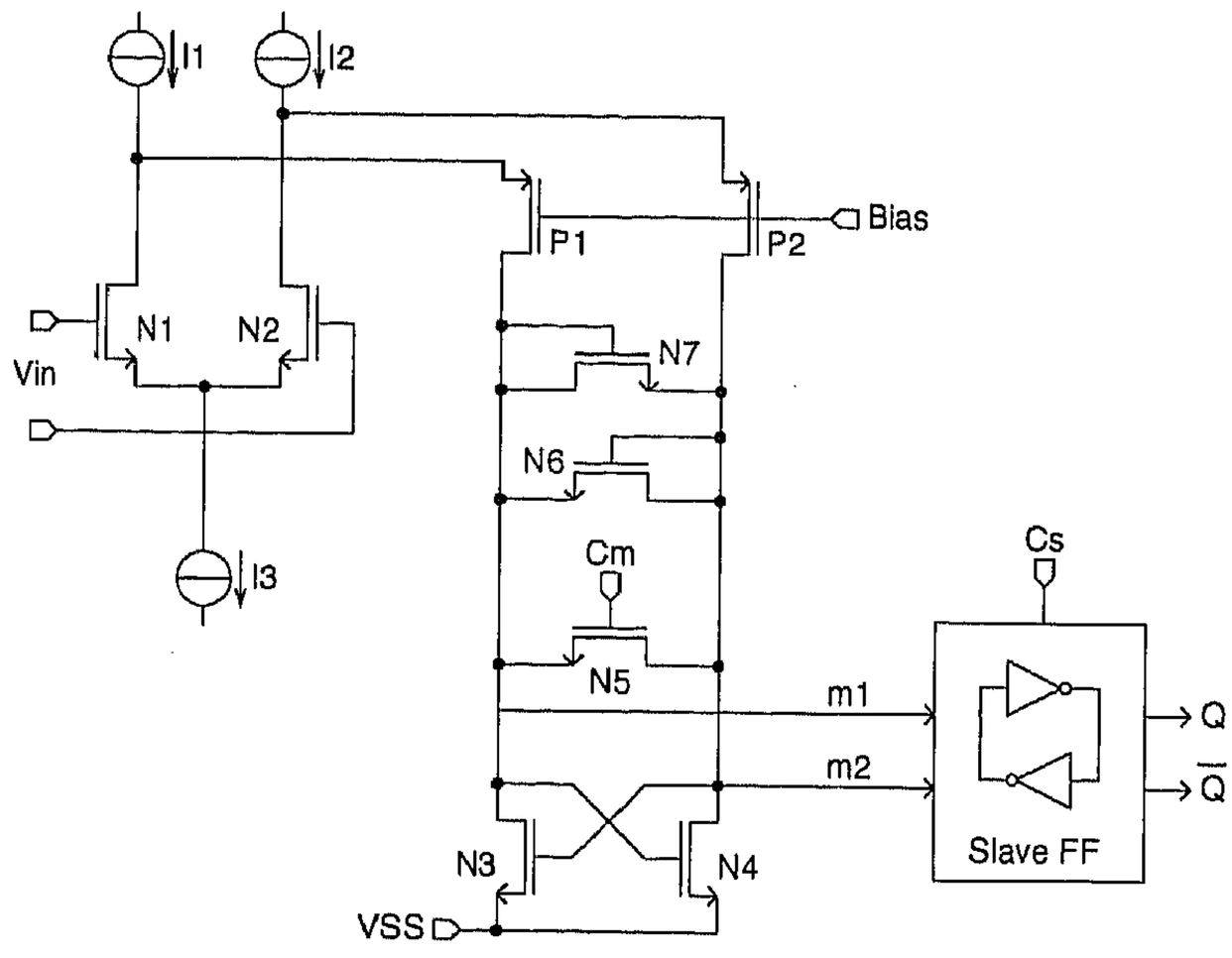


Figure 17: *Schematic diagram of the master-slave comparator*

A calculation model for the bit error rate is shown in figure 18(a). In [7] it is derived that the probability of an occurrence of a meta stable state whose duration t is longer than time interval t_n is given by:

$$P(t > t_n) = \mathrm{e}^{-\frac{A-1}{\tau}t_n}, \tag{30}$$

with A and $\tau = RC$ according to figure 18. Time interval t_n can be considered half of the sampling period:

$$t_n = \frac{1}{2f_{cl}} \tag{31}$$

with f_{cl} the clock frequency. The factor $\frac{A-1}{\tau}$ has to be maximized to decrease the probability of the occurrence of a meta stable state. For the comparator in figure 17 this factor is given by:

$$\frac{A-1}{\tau} = \frac{gm_{N3}}{C_{m1,2}} - \frac{1}{R_{o3}C_{m1,2}} \approx \frac{gm_{N3}}{C_{m1,2}}. \tag{32}$$

In this equation $C_{m1,2}$ is the capacitance at and between nodes m_1 and m_2 and R_{o3} the output resistance of transistors N_3 and N_4. Equation 30 can

[2]If the limiting circuit is implemented with a positive feedback loop, equation 28 can not be applied.

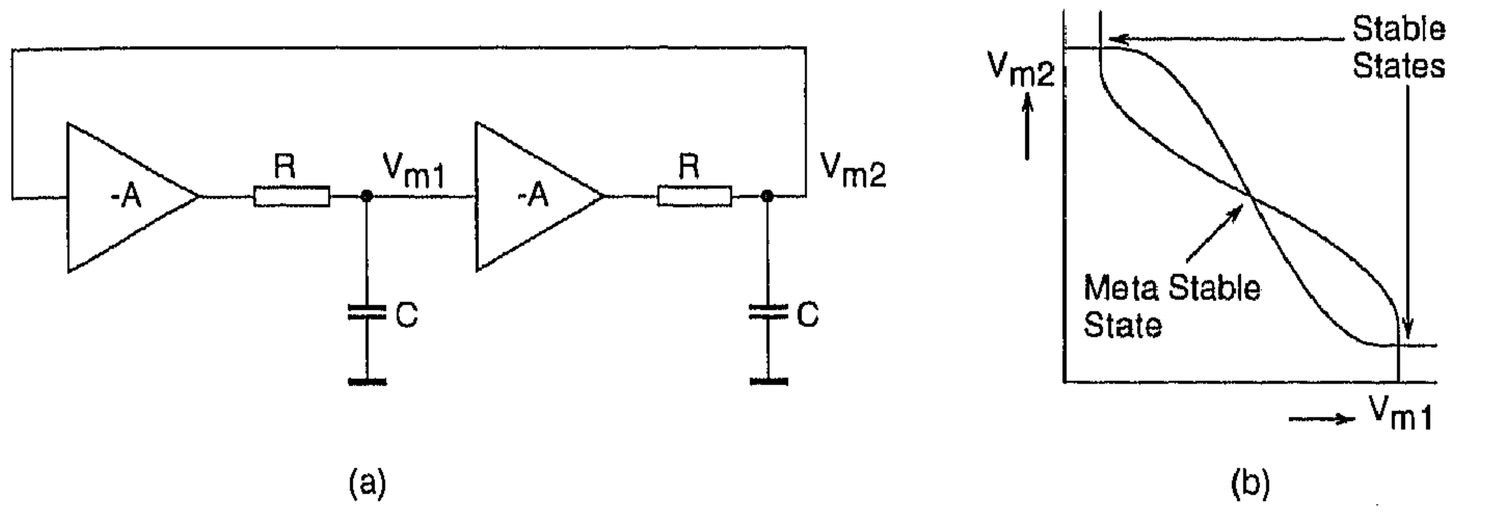


Figure 18: *(a) Calculation model for Bit Error Rate (BER) (b) Meta Stability*

be rewritten as:

$$BER = P(t > t_n) = \mathrm{e}^{-\frac{gm_{N3}}{2C_{m1,2}f_{cl}}}. \tag{33}$$

The power dissipation of the comparator is determined by the BER and maximum allowed offset. Offset of the comparator is determined by matching of transistors N_1, N_2, transistors N_3, N_4 and current sources I_1, I_2. The minimum dimensions for transistors N_3 and N_4 directly influence $C_{m1,2}$ and thus the BER. The ratio $\frac{gm_{N3}}{C_{m1,2}}$ determines the power necessary for a given offset.
For example, the comparator in the prototype A/D converter has a ratio $\frac{gm_{N3}}{C_{m1,2}} = 1.9 \cdot 10^9$, resulting in $BER = 7 \cdot 10^{-10}$. At a clock frequency of 45 MHz this means a probability of one error every 32 seconds.
The offset of the comparator $\sigma_{offset} = 2.5$ mV. 1 LSB in a folding signal at the input of the comparator equals 30 mV. The maximum DNL error at $3\sigma_{offset}$ equals 0.25 LSB. Therefore, offset compensation is not necessary in this design, which is advantageous to achieve a high clock frequency in the system.

7 Experimental results

Different prototype folding A/D converters have been made for 5 V and 3.3 V supply in a standard 0.8 μm CMOS process [1]. Chip area for both types is 0.75 mm^2. Power dissipation is 110 mW for the 5 V design and 45 mW for the 3.3 V design. Maximal clock frequencies are 70 MHz and 45 MHz respectively. Differential non-linearity (DNL) and integral non-linearity (INL) are shown in figure 19.

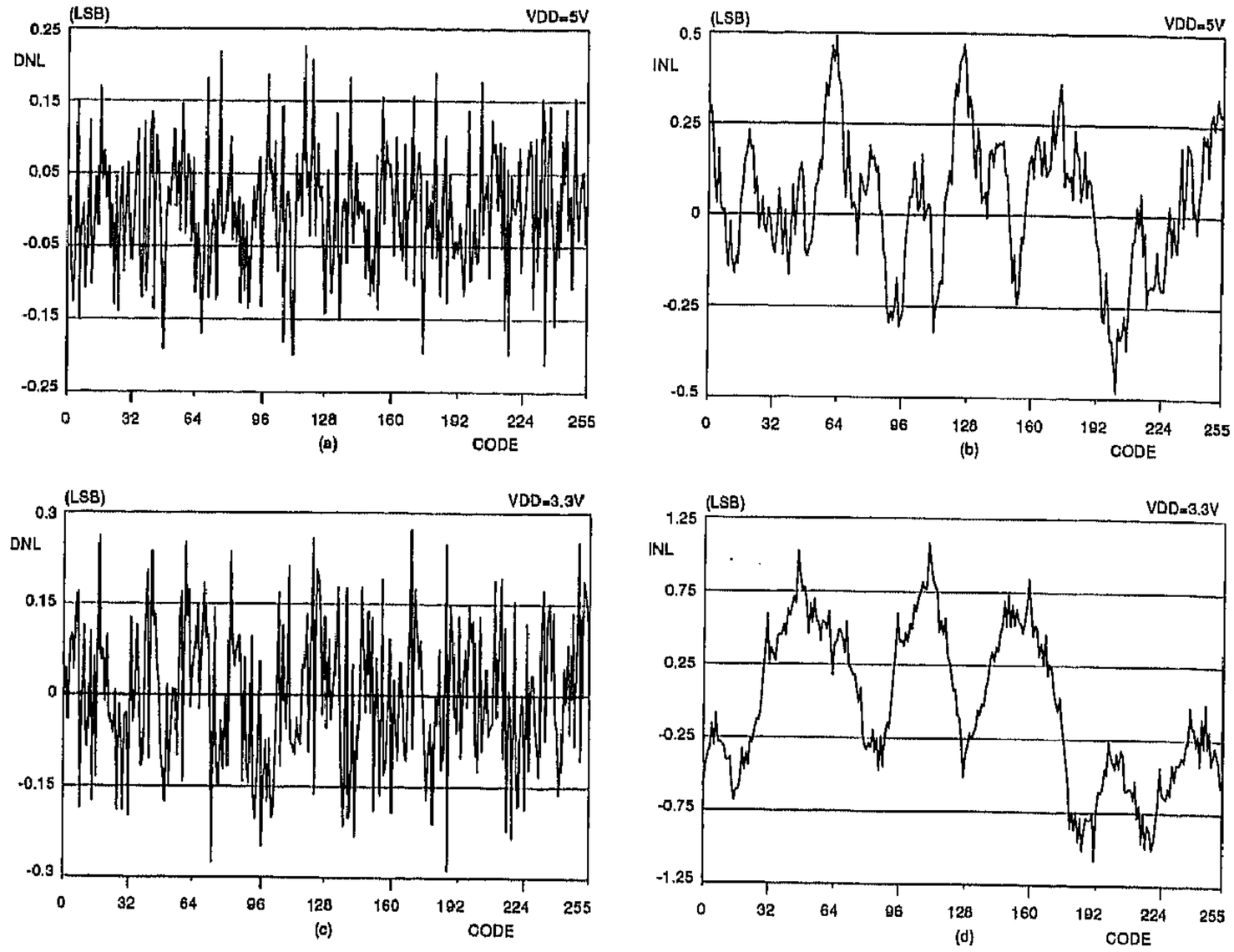
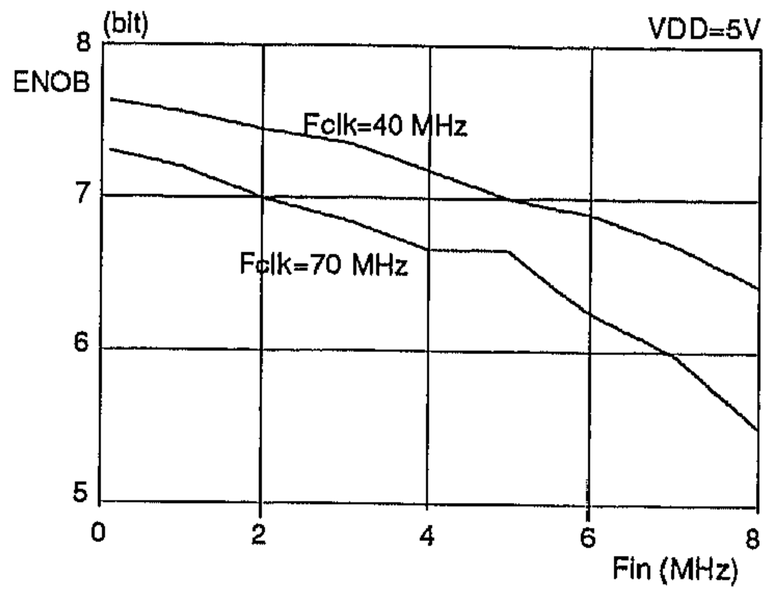


Figure 19: *DNL and INL for the 5 V and 3.3 V folding A/D converters*



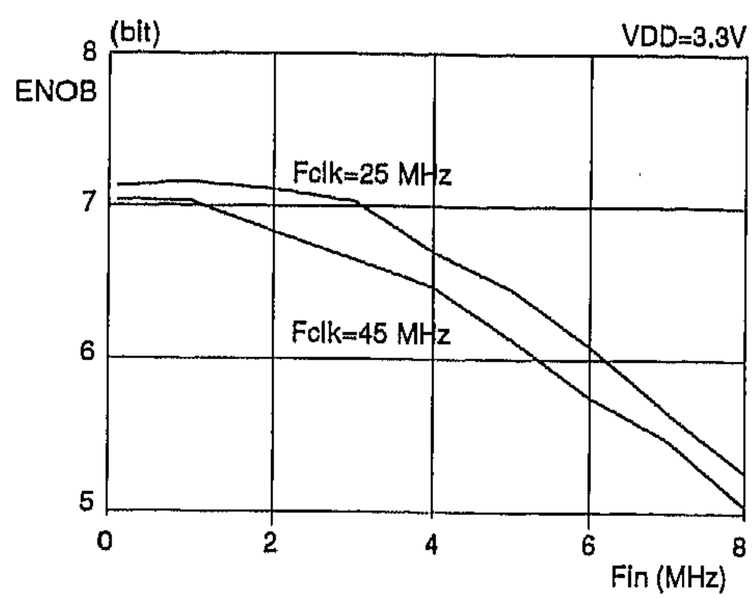


Figure 20: *Effective number of bits (ENOB) for the 5 V and 3.3 V design versus input frequency*

The effective number of bits (ENOB) represents the $\frac{S}{N}$ ratio and total harmonic distortion (THD) of the A/D converter. The ENOB versus the analog input frequency is shown in figure 20.

8 Conclusions

The implementation of folding and interpolation techniques in CMOS technology have been described. It has been shown that by the analog preprocessing operation a low power, high speed and compact A/D converter can be realized. The power dissipation of the reference ladder can be kept low due to the reduced number of input differential pairs. Furthermore, resistive interpolation helps in minimizing the power dissipation of the analog preprocessing by generation of missing folding signals without any additional power dissipation.
The comparators in the A/D converter are evaluated with respect to the bit error rate (BER). The BER directly determines the power necessary in the comparator.
As an example prototype A/D converters demonstrate the presented techniques. Experimental results have shown that the designed folding A/D converters satisfy the expected performance.

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