FA 16.3: A 70MSample/s 110mW 8b CMOS Folding Interpolating A/D Converter

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In bipolar technology the folding and interpolation technique has proven to be successful for high sample rates [1,2]. This paper investigates the possibilities of this technique in CMOS. The major advantage of folding and interpolation in CMOS lies in the field of high sample rate in combination with low power consumption and small chip area. The folding converter requires little power to drive the input compared to other converters since the input behaves like a linear and constant capacitor [5]. For similar reasons the power consumption of the reference ladder of the folding converter can be kept low. 8b CMOS designs reported in References 3 and 4 achieve 85MSample/s and 100MSample/s respectively. Both designs however have a power dissipation of more than 1W, too much for embedded applications. The circuit reported here runs at 70MSample/s and dissipates only 110mW.

Figure 1 shows the architecture of the ADC. The converter can be split into a parallel operating coarse and fine part. The coarse part generates a 3b coarse code from the analog input signal by means of a simple flash structure. The fine part generates the remaining 5 fine bits, and is based on the folding and interpolation technique [1,2].

The aim of an 8-times folding technique is to preprocess the analog signal so that one comparator is used for 8 different input signal levels instead of only one, like in a full flash architecture. Therefore the coarse part has to consist of 3b to decide which of the 8 possibilities is valid. Four folding blocks FB0-FB3 generate four folding signals F0-F3as shown in Figure 2. The folding blocks consist of 11 simple long-tailed pairs with the outputs of the odd and even numbered pairs cross-coupled as shown in Figure 3. The inputs of the long-tailed pairs are connected to the input signal and the reference ladder. The differential output current I1-I2 is of the shape of a folding signal in Figure 2. Since 11 long-tailed pairs are connected to the nodes n1 and n2 in the folding block, the parasitic capacitance at these nodes is very large (2pF). Furthermore the current I1-I2 has a much higher frequency than the analog input signal, inherent to the folding operation. Therefore a transimpedance amplifier is added to minimize the voltage swing across the nodes n1 and n2 and thus to eliminate the effect of the large parasitic capacitances on these nodes. The four folding signals are designed to have different offsets with respect to the input signal. Especially at high frequencies, the peaks of the folding signals are distorted (solid lines in Figure 2), however, one of the four signals is always in its linear region around zero crossing. With 32 folding signals instead of four, only the zero crossings itself would be of interest, and even more distortion in the peaks of the 32 folding signals would be allowed. The lacking 28 signals are generated by resistive interpolation [1]. A first resistive interpolator generates four additional signals from F0-F3 and the resulting 8 folding signals are fed into voltage amplifiers for 8 times amplification. After the amplification, another four times interpolation resistor network generates 32 folding signals that are fed into 32 comparators that detect the zero crossings of the 32 folding signals. The outputs of the 32 comparators are fed into digital encoding logic and generate the 5 fine bits.

The actual circuit implementation is fully differential to achieve immunity for substrate noise and crosstalk. This allows embedded application of the converter in large system ICs. In the folding blocks the transistors have large gate areas, and thus offsets are small. The resistive interpolation principle helps in further reducing the effects of internal offsets. Thanks to the signal enhancement in the amplifiers, the fine comparators have large input signals (1 LSB=40mV) so small transistors can be used without offset compensation [5]. Thus higher sample rates can be achieved.

Two designs are reported; one for 5V and one for 3.3V supply. The converters are realized in a 0.8μm CMOS process. Chip micrographs are shown in Figure 6. At 5V supply the maximal sample rate is 70MSample/s and the power dissipation is 110mW (including the reference ladder). At 3.3V supply the maximal sample rate is 45MSample/s and the dissipation is 45mW. The effective number of bits (ENOB), which is a representation of the signal-to-noise-and-distortion ratio, is measured on aHP82000 mixed-mode test system. Differential non-linearity (DNL) is shown in Figure 4 and the ENOB versus analog input frequency is shown in Figure 5. Experimental data is summarized in Table 1.

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References

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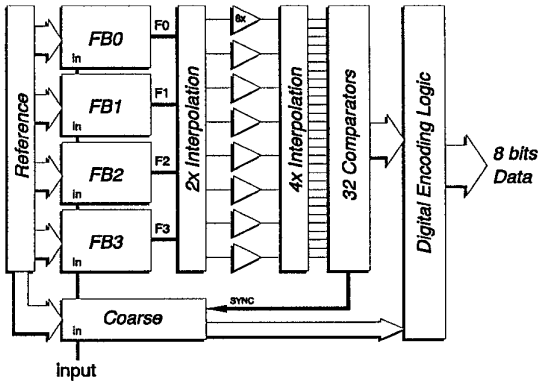


Figure 1: Block diagram of the folding ADC.

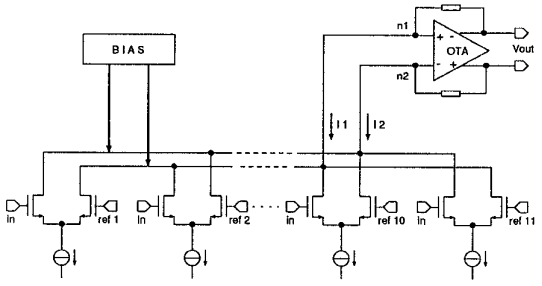


Figure 3: Folding block.

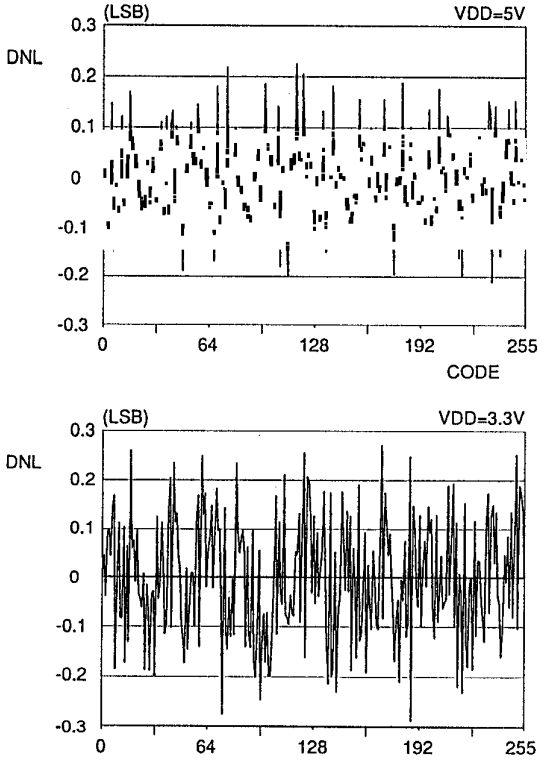


Figure 4: Measured DNL for 5V and 3.3V designs.

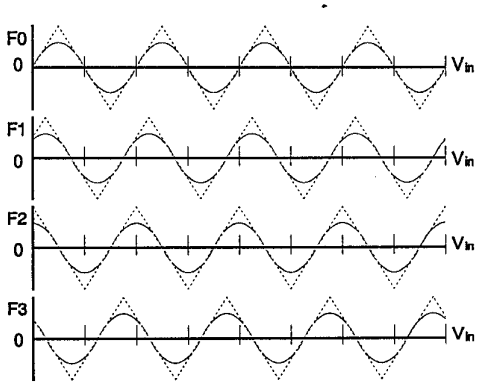
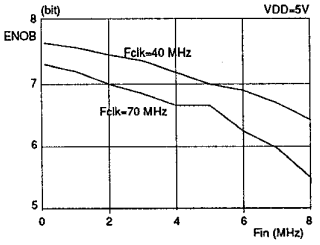


Figure 2: Folding signals F0-F3.



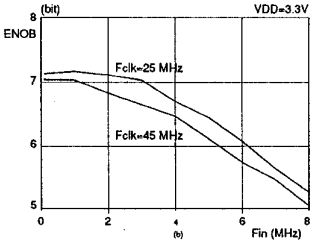


Figure 5: Measured signal-to-noise-and-distortion ratio (effective no. of bits) of full-swing input signal versus input frequency, for 5V and 3.3V design.

Figure 6: See page 379.

Resolution	8b	
Input impedance	4.8 pF	
Reference ladder resistance	720Ω	
Active area	0.8mm²	
Technology	0.8μm, 1PS, 2AL, CMOS	
Supply voltage	5V	3.3V
Analog input	2Vpp	1.4Vpp
Integral nonlinearity	±0.5LS	±1.0LSB
Differential nonlinearity	±0.2LSB	±0.3LSB
Max. clock frequency	70MHz	45MHz
Power dissipation	110mW	45mW

Table 1: Measured results.

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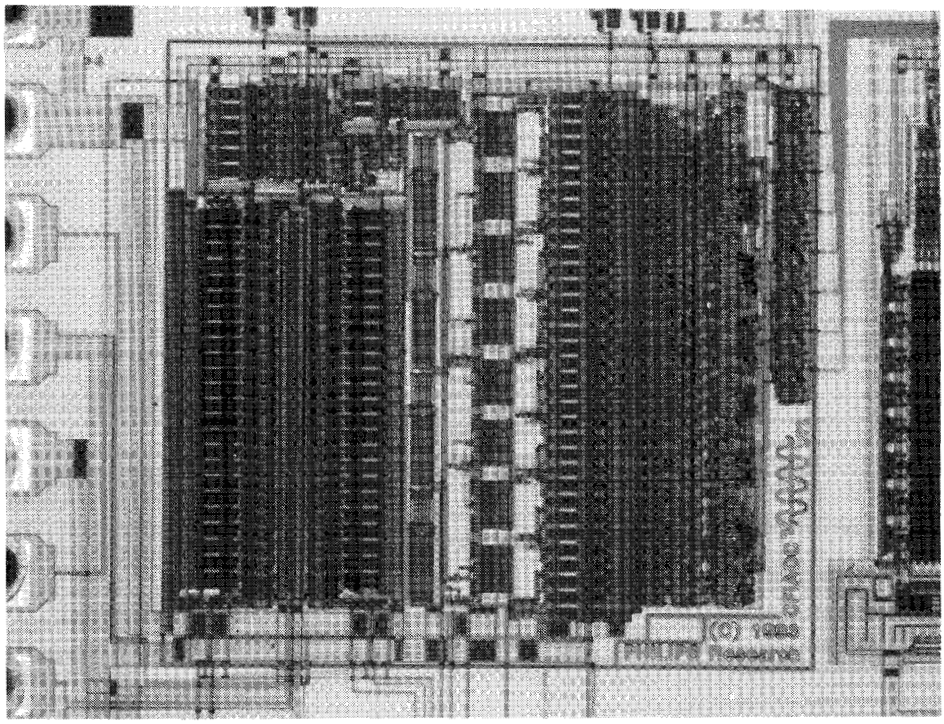

Figure 6: Chip micrograph. Active area is 0.8mm².

FA 16.4: 12b 40MSample/s Two-Step A/D Converter

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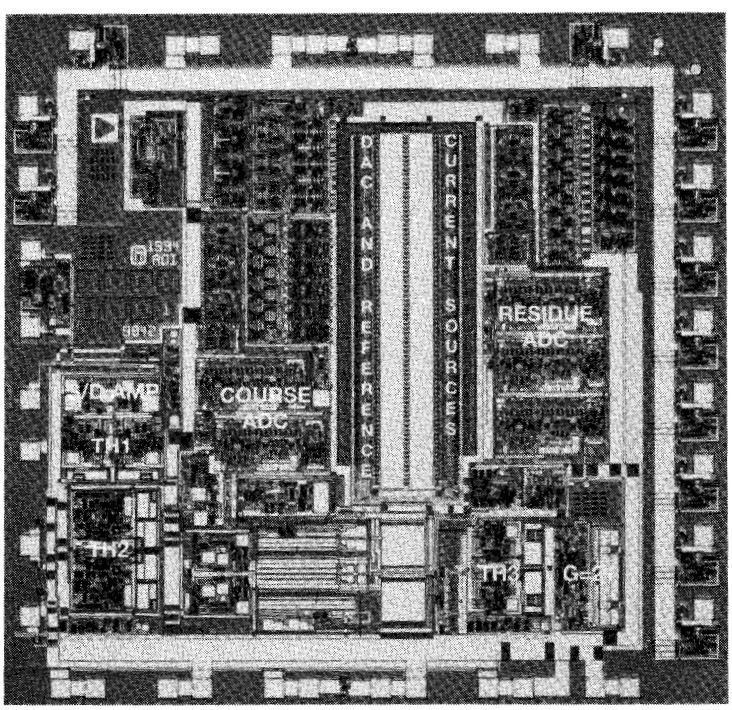

Figure 7: 12b 50MSample/s 2-stage A/D converter die micrograph.