Test-Signal Search for Mixed-Signal Cores in a System-on-Chip

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Abstract—**The well-known approach towards testing mixed-signal cores is functional testing and basically measuring key parameters of the core. However, especially if performance requirements increase, and embedded cores are considered, functional testing becomes technically and economically less attractive. A more cost-effective approach could be accomplished by a combination of reduced functional tests and added structural tests. In addition, it will also improve the debugging facilities of cores. Basic problem remains the large computational effort for analogue structural testing. In this paper, we introduce the concept of Testability Transfer Function for both analogue as well as digital parts in a mixed-signal core. This opens new possibilities for efficient structural testing of embedded mixed-signal cores, thereby adding to the quality of tests.**

Keywords—**Mixed-Signal Testing; Testability Transfer Function; Debugging; Data converter testing**

I. INTRODUCTION

The normal method of testing mixed-signal cores, like e.g. data converters, is via functional testing. The topology of the design, actual defects and associated fault models and debugging options are not of direct interest in this approach. However with the increase of performance of these devices, e.g. in the case of high-speed ADCs and especially if these cores are embedded, extensive functional testing becomes problematic in technical and economical sense. This can be a result of the limited bandwidth of the Test Access Mechanism (TAM) for e.g. the analogue part [1].

In addition, the (speed) restrictions of available ATE, and reluctance of buying expensive high-speed equipment can be an obstacle.

This has triggered the idea to perform a trade-off between functional tests and structural tests, to either increase the quality and debugging options of the mixed-signal cores, or just plainly reducing the test costs while maintaining the same quality of testing.

However, structural testing has not yet really taken off in industry. One of the reasons of this slow acceptance is the very high computational complexity, while performing fault simulation and test generation.

In references [2-4], the concept of the Testability Transfer Function (TTF) for analogue [2, 3] as well as digital [4] cores has been introduced and enhanced. This paper combines the TTFs of both worlds, thereby opening the road to relative low-cost mixed-signal testability-based ATPG, and increased debugging capability.

First, a short recapitulation on analogue TTFs is given, and then we introduce the TTF for digital cores. Next, a vehicle, a simple 3-bit ADC, is presented on which a number of experiments have been carried out to illustrate the approach.

II. TTF FOR ANALOGUE CORES

In a previous paper [3], a new expression for the TTF for analogue transistor-level circuits has been derived, overcoming previous [2] fundamental problems, like low sensitivity for low impedances and connections to power lines.

As a simple example of TTFs, imagine a resistor impedance with nodes “a” and “b”. Node “a” is fully *observable* from node “b” if the impedance is zero Ohms. Furthermore, node “b” is completely *uncontrollable* from node “a” if the impedance is

infinitely high. Our new definition of the TTF of an impedance Z(ω) is:

$$TTF(Z(\omega)) = (1 - \log_{OC} | Z(\omega)|)^a$$

where "a" denotes a user-defined parameter around 1 to change the sensitivity for high and low values of Z(ω), while OC (open circuit) indicates open circuit conditions. This (non-critical) condition is also user defined, but in our case always chosen to be 10MΩ.

Based on this definition, also the TTF of a transistor can be derived, and hence of complete transistor networks [3]. The details of these matrix calculations can be found in [3, 4].

The major advantage of using TTFs over e.g. sensitivity-based testability calculations is the major reduction in computational time, being currently the major obstacle in industrial applications.

In Figure 1, an example is depicted of a simple operational amplifier [3, 5], indicating nodes of interest. Using this scheme, a signal flow graph (SFG) can be constructed by calculations from lower elements like transistors, indicating the TTF relationships between nodes with, in our case, the *frequency* as parameter. The user can also make other choices in parameters, if required.

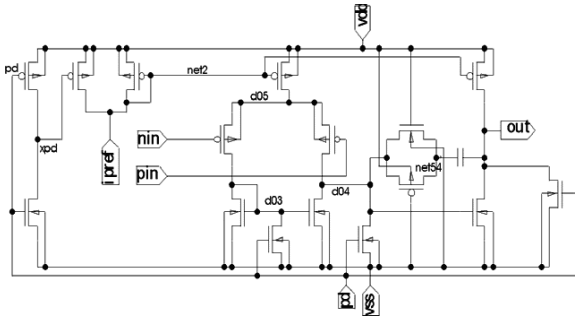

Figure 1*:* Transistor schematic of a simple CMOS operational amplifier [5].

This minimized SFG is shown in Figure 2, and forms the basis to calculate the observability, controllability and hence testability of these nodes. In Table 1, the results of these calculations have been listed. It is clear that e.g. node net2 has a serious controllabilty problem (italic), hence resulting in a poor testability value.

A reduction of a factor of 23 in CPU time has been achieved, as compared to conventional methods like sensitivity-analysis based on circuit (HSPICE) simulations for obtaining testability data.

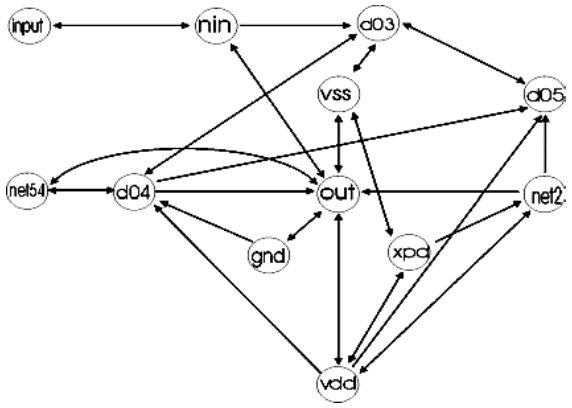

Figure 2: Signal flow graph of the CMOS operational amplifier.

The different values for the testability for nodes at different operating frequencies form the basis of our analogue test-vector selection, i.e. analogue ATPG.

Table 1: The testability measures of nodes at an input (single-tone) sine-wave signal frequency of 100 kHz.

node	C (node)	O (node)	T (node)
out	0.3954	1.0	0.6288
nin	1.0	0.3081	0.5551
net 54	0.4368	0.4545	0.4455
d03	0.5739	0.5214	0.5470
d04	0.5765	0.5945	0.5854
xpd	0.3063	0.5136	0.3966
net2	*0.2917*	0.5432	0.3981
d05	0.4572	0.5308	0.4927

III. TTF FOR DIGITAL CORES

In the past, many testability measures have been developed for digital circuits; some approaches are based on *cost* measures like SCOAP [6], while others are based on *probabilities* like TMEAS [7]. In, for instance, reference [8], observability and controllability transfer functions are used as being specific properties of nodes.

We have applied and extended the initial concept of TTF calculations to digital logic circuits, while introducing probabilities. Our approach has the advantage over the previous ones that they can distinguish between different input and output nodes. Basic drive behind our approach is to be able to apply TTFs and the subsequent structural testing selection to *true* mixed analogue-digital cores.

Let us assume as simple example, a logic OR gate with associated input (a, b) and output (c) node names. In Figure 3, the associated TTF graph is presented of the OR gate. Notice the similarity with figure 2 in the analogue case.

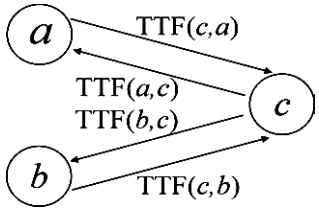

Figure 3: Derived signal flow graph indicating the possible TTFs in a simple OR logic gate.

A computer can derive the actual TTF values in a simple and straightforward manner. Key is the use of the truth table of the logic gate. Looking at the OR truth table, it is obvious that node "c" can be *fully controlled* by node "a", under the condition that input node "b" is equal to zero. The probability that this will be the case is 50%.

Node "a" can only be determined by node "c", in the case "c" is zero. The truth table shows that this probability is 25%, which is the same condition that input "a" as well as input "b" is both zero. The results of all TTFs of the OR gate are now listed below:

TTF (c,a) = p (b=0) = 0.5
TTF (c,b) = p (a=0) = 0.5
TTF (a,c) = p (c=0) = p (a=0 & b=0) = 0.25
TTF (b,c) = p (c=0) = p (a=0 & b=0) = 0.25

In these equations, for instance p (b=0) denotes the probability of the TTF under the condition that input b is logic zero. We have also carried out similar exercises with regard to other logic primitives and complex logic gates [4]. Figure 4 shows a more complex example, consisting of several logic primitives, being the scheme of a full-adder circuit.

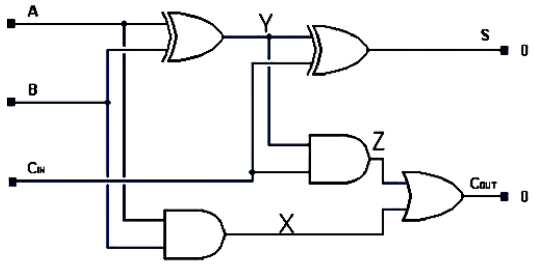

Figure 4: Logic scheme of the full-adder circuit

After combining the TTFs of the different logic primitives, the overall SFG of the full-adder circuit in Figure 5 results. The TTFs that represent the path from output to input nodes, necessary for observability calculations, are underlined.

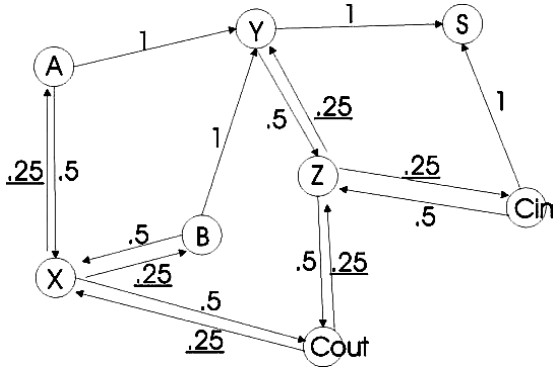

Figure 5: Signal flow graph of the full-adder circuit including TTF values.

In a similar way as indicated previously, the observabilities, controllabilities and testabilities of the different nodes have been calculated; the results of internal nodes are shown in Table 2. From this data, it is clear that the testability of node Y (italic) is the most problematic one, as result of its low observability.

Table 2: Testability of nodes of digital full adder

node	C (node)	O (node)	T (node)
X	0.54	0.25	0.3674
Y	1	*0.0625*	*0.25*
Z	0.54	0.25	0.3674

As one has now knowledge on all nodes, also the debugging of the circuit is now possible, in contrast to functional testing, which does not provide any information on internal nodes.

The testability data forms the basis for guidance with regard to the ATPG process. The limitations of the latter approach, such as sometimes resulting in incorrect results, are not different from other methods of obtaining testability data.

IV. COMBINING BOTH ANALOGUE AND DIGITAL TTFS

As the previous sections show, it is possible to define a TTF for analogue as well as digital parts. This opens the way to use the concept of TTF as guidance for test-vector *selection* of mixed-signal devices. Note that bridging faults form the basis of the analogue approach,

and that certain cases of bridging faults to Vdd and Gnd are equivalent to stuck-at faults.

For pure analogue and pure digital parts of a mixed-signal core, the distinction what model to choose is clear. In the case of a true mixed-signal component, like a comparator, it has to be treated as an analogue component.

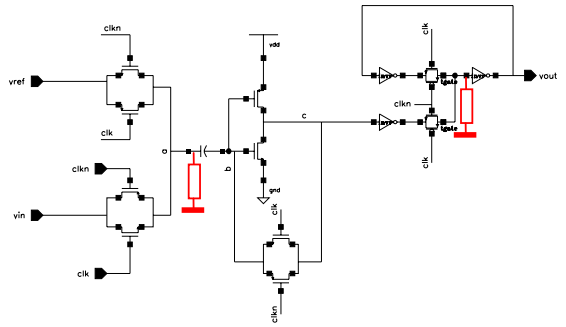

Figure 6: Basic MOS single-stage comparator for use in a full-flash ADC, and inserted example bridging faults.

Figures 6 and 7 depict our simple mixed-signal ADC core benchmark. Figure 6 shows a transmission-gate based single-stage comparator [9] including a positive-level latch [10].

The AMS 0.8 µm design kit from Europractice was the basis for this implementation. Except for the inverter in the middle, which has a Wn / Ln of 80µ/0.8µ and a Wp / Lp of 60µ/0.8µ, the W / L values for all NMOS and PMOS transistors are 10µ / 0.8µm. The storage capacitor has a value of 10pF and a power-supply voltage of 5V is used.

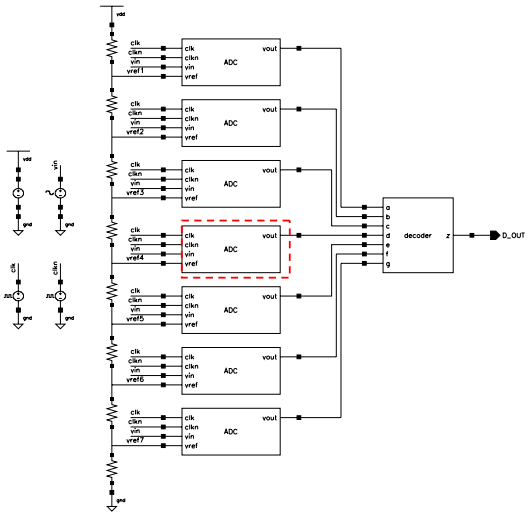

Figure 7: Top view of a 3-bit ADC consisting of the previous single-stage CMOS comparators.

The design has not been optimised for improved converter behaviour. Figure 7 shows the top-level scheme of a 3-bit ADC. The circuit was designed for applications in the audio frequency range. It employs the simple thermometer-to-binary encoder to provide the digital output signal D_OUT.

Now, the TTFs of the components and logic primitives in Figure 6 form the basis to construct an overall SFG of the complete converter. From this, the observabilities, controllabilities and testabilities of all nodes are constructed. This forms the basis for further test-vector selection. In the next section, we will assume a fault in the analogue as well as the digital part.

V. RESULTS

We have used the single bridging fault model as a basis. As examples, we have assumed a single bridging fault in the analogue part, from node “a” (left-hand resistor, Fig. 6) to ground, and a single bridging fault from the input of the last inverter to ground (right-hand resistor, Fig. 6) in the digital part. In accordance with previous publications [3, 4], the values of these shorting bridging faults are taken to be 500Ω. As an example, the faults are both located in the fourth comparator (dashed box) from below in figure 7.

After the transformation of figure 7 into the signal flow graph, TTF calculations for the bridging fault in the analogue part reveal that a sine wave of 8 kHz will be able to detect the analogue bridging fault in the comparator, and will translate into a faulty digital output. In other words, the 8 kHz single-tone sine-wave signal will provide the largest deviation in the output. The amplitude of the input sine-wave signal was 2.5V with an offset of - 2.5V.

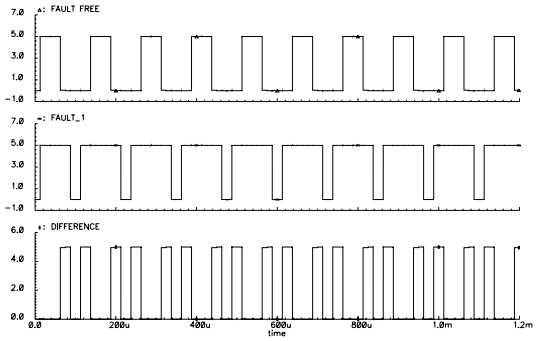

Figure 8: Fault-free, faulty (analogue bridging fault) and difference time response of the fourth comparator using an 8 kHz sine input signal (HSPICE).

To verify this data, we have carried out extensive circuit simulations using HSPICE in a Cadence environment using the AMS 0.8 µm design kit. Figure 8 shows the simulations in the time domain in the case an 8 kHz sine wave is applied to the input of the ADC. The signals are respectively the fault-free digital output of that comparator, the faulty one, and the difference between them. It is obvious that this fault will directly translate into the digital output of the complete converter.

Now, the digital signals have been converted to an analogue value, and are represented in the frequency domain in figure 9. It shows a significant difference in the response at 8 kHz and the second harmonic.

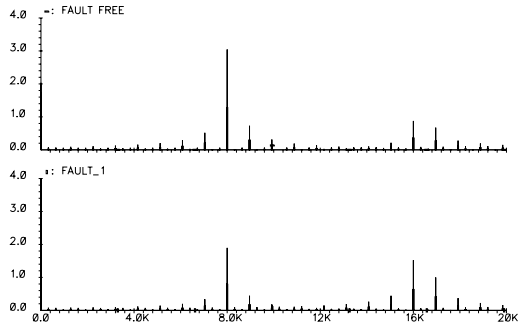

Figure 9: Fault-free and faulty (analogue bridging fault) output behaviour of the fourth comparator using an 8 kHz sine wave signal as input signal.

The same procedure was repeated for the bridging fault in the digital part of figure 6, which turned out to be effectively a stuck-at-zero fault for 500Ω. Figure 10 shows the faulty response of an 8 kHz sine wave, just to compare it with the fault-free response in figure 8. Actually, the frequency is not an issue here, but the peak-to-peak value. Hence, a DC input signal with sufficient value is also sufficient to detect this fault. It shows the output is stuck-to-one, which was to be expected.

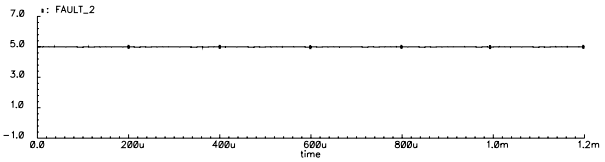

Figure 10: Faulty (digital bridging fault, effectively SA0) output behaviour of the fourth comparator using an 8 kHz sine-wave signal as input signal.

We have used the vast amount of analogue input and digital output simulation data as input for *Labview* simulations, in calculating key static and dynamic data parameters for data converters like e.g. offset, gain, INL, DNL and THD and SNR values. The figures 11 and 12 show the results for the fault-free and analogue fault example respectively.

The histogram calculations in the fault-free and analogue fault case show a definite difference in all static and dynamic key parameters of the converter (Table 3). In this sense, a test engineer both can justify a device rejection on the ground of a simple single-tone structural test as the more complex histogram tests for this fault.

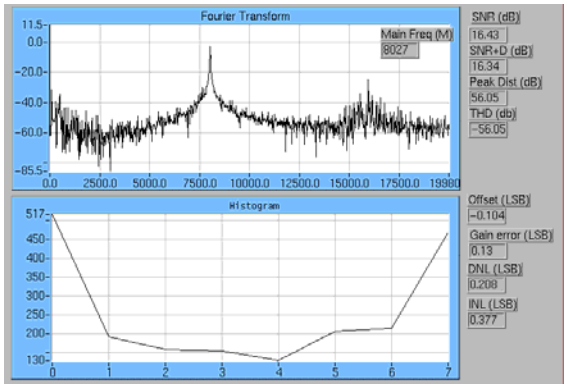

Figure 11: Results from Labview histogram calculations of the 3-bit ADC for key parameters in the fault-free case.

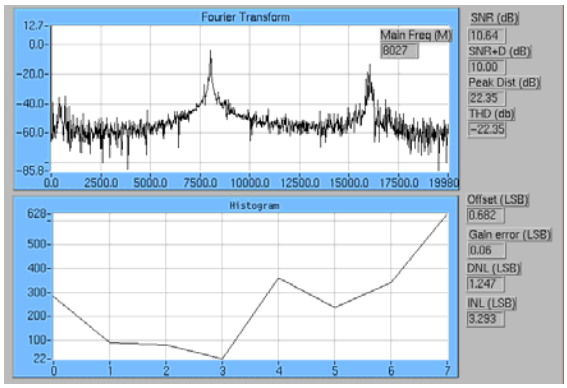

Figure 12: Results from Labview histogram calculations of the 3-bit ADC for key parameters in the case of the analogue bridging fault.

The resulting output signal from the faulty ADC is shown in figure 13. This signal can be easily evaluated in a simple test system for structural tests.

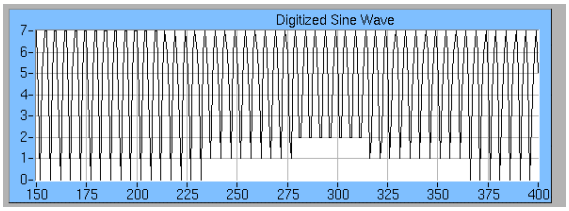

Figure 13: The reconstructed output signal resulting from the analogue bridging fault.

We carried out the same experiments for the digital fault. As figure 10 shows, the detection in the structural test case is very simple, as is the input signal. Again, histogram calculations were performed in the case of the digital bridging fault. Although the key parameters are not exactly the same, they are relatively close to the fault-free case. So for this particular fault, it seems the results of the structural test provides much stronger evidence for a fault than the histogram tests. In addition also diagnostic / debugging capabilities are available. From these examples, it is shown that structural tests can increase the quality and debugging possibilities, as compared to histogram measurements only. In some cases, the histogram approach will provide less concluding data on faults, which can subsequently be augmented by specific structural tests.

Table 3: Overview of static and dynamic parameters for the fault-free, analogue and digital fault ADC.

Parameter	Fault-free	Digital fault	Analogue fault
SNR (dB)	16.43	17.48	10.64
SNR +D (dB)	16.34	17.44	10.00
THD (dB)	*-56.05*	-55.31	*-22.35*
Offset error (LSB)	-0.10	0.422	0.682
Gain error (LSB)	0.13	0.10	0.06
DNL (LSB)	*0.208*	0.490	*1.247*
INL (LSB)	*0.377*	0.628	*3.293*

The next step is to see to what extend we can reduce functional tests, while simple structural tests are added to maintain test quality. Simulations prior to actual high-volume testing can provide information on that. In a future paper, we will evaluate all faults in the ADC.

VI. CONCLUSIONS

In this paper, testability analysis has been taken as guidance for the structural test-vector selection of mixed-signal cores. This requires a similar testability analysis approach for analogue as well as digital parts. This can be provided via the TTF concept, which provides significant gains in computational effort and hence CPU times. We have presented examples of TTF calculations of simple analogue as well as digital parts. Next, we have applied the concept to a simple 3-bit ADC. HSPICE simulations have confirmed these results; Labview simulations indicate that the (easy-) generated structural tests have the potential to either increase the quality of converter tests, or reduce the number of complex measurements under equal quality.

ACKNOWLEDGEMENTS

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