Defect-Oriented Testing of an RSFQ D-type Flip-Flop

Arun A. Joseph, Marcel H.H. Weusthof and Hans G. Kerkhoff

Testable Design and Test of Microsystems Group, MESA+ Institute for Nanotechnology,
University of Twente, 7500 AE Enschede, The Netherlands,
Phone: +31-53-489 4007; fax: +31-53-489 1034.
E-mail: {A.A.Joseph; M.H.H.Weusthof; H.G.Kerkhoff}@el.utwente.nl

Abstract—**Even though superconductor electronics is capable of handling the requirements for efficient high-speed devices in telecommunication and computing, the yield is very low compared to semiconductor processes. A structured test methodology has to be developed to improve the low yield in Superconductor Electronics (SCE). We have conducted studies on a Low-Temperature Superconductor (LTS) process and have developed test structures for the detection of random defects occurring in the process. We have implemented test-routines for semi-automatic testing of processed chips for structural defects at room temperature. In this paper, we present the details of the conducted tests on those test structures and associated measurement results. One of the defects, a crack in the superconducting wire is then further analysed to study its influence on an Rapid Single Flux Quantum (RSFQ) D-type Flip-Flop.**

Keywords— **LTS Devices, RSFQ Circuit Testing, Structural testing, Superconductor Electronics**

I. INTRODUCTION

The requirements of high-speed devices in electronic industry is increasing; e.g. in Software Defined Radio (SDR) [1], to the extent that semiconductor technologies are not able to supply the demands. Another application that requires ultra-high speed devices is the realisation of a petaflops scale computer [2]. Although in its infancy, superconductor technologies, especially the LTS RSFQ technology [3] is capable of realising these high-end products. An RSFQ T-Flip-Flop operating at 770 GHz is the fastest electronic device ever built [4].

SCE is a promising candidate for high-end applications due to the following inherent virtues. The theoretical speed limit of an SCE circuit is very high (~1 THz) and they work with the accuracy of a magnetic flux quantum (2.07 x 10e-15 Wb). Further more, they have a very low-power consumption (~1 pW/gate). Disadvantage of an SCE system is the requirement of cooling the device to superconducting temperatures. But the above-mentioned high-end applications require cooling even if semiconductor technologies are used. As an example, if we compare the power requirement of a petaflops scale computer, it will consume 10–15 MW of power if realised in the current semiconductor technologies while only 2.6 MW is required if realised in the current SCE technology [5]. Intense research is being carried out to bring the SCE systems to "high" temperatures by developing them in high-temperature superconductor (HTS) technology. An already proven application is HTS filters in wireless networks [6, 7]. In fact, unless there is a large volume of data to be processed or ultra-high speed switching is required per unit time, superconductor technologies will not be economic to maintain.

In the recent past, many devices have been developed in SCE. ADCs targeted towards SDR application [8, 9] and microprocessor chips [10, 11] are examples of such complex designs. Even though much effort is spent in the design of such devices, a systematic test methodology has yet to be developed. Current tests are restricted to functional verification and little information on the mechanism behind the failures is available.

Further more, the yield level in SCE is much lower than semiconductor technologies. This is due to the fact that much emphasis was given in the past towards complex system development. Testable design and structural test techniques were not yet considered in research. As a result of this, only little information on failure mechanisms and defect statistics is available leading to a very low yield in SCE technologies.

We have started research into probable structural defects and fault mechanism in SCE. A test chip has been developed for an SCE fabrication process. We have conducted measurements on the processed chips and statistical information for Inductive Fault Analysis (IFA), a defect-oriented test (DOT) methodology, is

obtained from it. This information is used to model faults in a circuit. This paper focuses on a crack in the Niobium (Nb) wiring layer and its influence on digital logic circuits.

The organisation of the paper is as follows. The SCE process under consideration is introduced in the following section. In section 3, the development of the IFA for SCE is described. Experimental analysis and measurement results on the processed test-chips are covered in section 4. Modelling and influence of a crucial defect in SCE digital logic follows in section 5. Conclusions are drawn in the final section.

II. AN SCE FABRICATION PROCESS

An SCE fabrication process is much similar to that of semiconductor process. In fact, an SCE process is much simpler due to the lower number of metal wiring layers. This is because complex systems can be implemented with less number of the basic building block, a Josephson junction (JJ), as compared to the number of transistors in semiconductors. For the study we considered the JeSEF (Jena Superconductor Electronics Foundry) LTS RSFQ fabrication process [12]. This is the foundry being developed for European SCE activities.
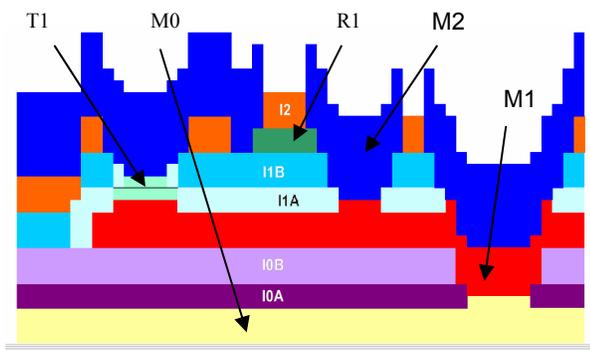
The JeSEF process has three metal layers including

Fig.1 Cross-section of the JeSEF LTS RSFQ fabrication process under consideration.

the ground plane (M0, M1 and M2) using Niobium (Nb) and a Mo-resistor layer R1. To reduce the probability of pinholes in the isolation layers leading to interlayer shorts between the conducting layers, the isolation is carried out in two separate steps – one by niobium oxide and the other by silicon oxide. M0 and M1 are separated by I0A and I0B, while M1 and R1 are isolated by I1A and I1B. The T1 layer defines a JJ, which is a tri-layer.

The tri-layer is created using a single mask. It actually consists of a sandwich of 3 layers, two Nb layers acting as the electrodes with the Al_2O_3 sandwich in-between. This is carried out so as to minimize the formation of

pinholes in the thin barrier. A cross-section of the process is shown in Fig. 1. The minimum dimensions for interconnection width and spacing are 5 μm. The critical current density J_c for the process is 1 kA/cm^2 and the sheet resistance of the Mo-resistor layer (R1) is 1 Ω/square. The junction capacitance for the process is 0.05 pF/μm^2.

III. DEVELOPMENT OF IFA FOR SCE

We have investigated the JeSEF LTS process as a part of our earlier research [13] and probable defects that can occur in the process were identified. They were identified using the information about the frequency of occurrence of weak-spots and the topography of defects. The classification of the defects is given in Table I. Shorts, opens or near opens (cracks) and contact resistance problems are the major causes of the defects. A number of test structures were developed in this process so as to get statistical information for conducting IFA in SCE.

TABLE I
DEFECTS IN AN LTS RSFQ PROCESS

Type of Defect	Nature of the Defect
Junction defects	Shorts, opens or excessive size and number of pin holes in the thin dielectric barrier
Metal layer defects	Opens or near opens due to thinning, bridges or shorts due to excessive material
Resistor layer defects	Opens or near opens in the metal-to-resistor contact, opens and near opens in the thin Mo resistor layer, bridges or shorts in Mo resistor layer
Isolation layer defects	Opens or near opens resulting in bridges, contact hole problems in via hole

A. Test methodology for the Process Analysis

The Tests for the above mentioned defects are performed by measuring an electrical parameter of the test structure under consideration. Certain deviations from a nominal parameter value are then indicative for the presence of a defect. However, the test parameter will have a certain natural variation inherent in the process. This is generally assumed to be a normal distribution. The amount of natural variation is a function of the amount of test objects in a segment.

The presence of defects will cause parameter changes that result in a different distribution for the parameter values. In the ideal case, the distributions of the parameter for the defect and defect-free cases are separate. But, in a real case, there is a possibility of an
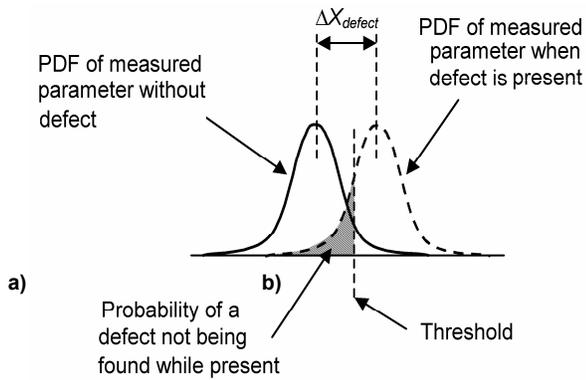
Fig. 2 Realistic probability distribution function (PDF) of measured parameters, when a defect is absent and present, showing possible overlap.

overlap of the distribution by which the presence of a defect will be obscured by the natural parameter variations (in case of marginal parameter changes). A defect causing a change ΔX_{defect} will result in a shifted distribution depicted in Fig. 2, but can be handled by careful design of the structures [14].

For the detection of shorts, opens or near opens, the ratio of resistance of a plain meander to that of the stepped meander can be used to compare any difference showing the presence of a defect. We have implemented the idea proposed in [15] called "van der Pol" structures for this purpose. Example of such a processed structure is shown in Fig. 3. This structure is to detect probable cracking in the wiring layer M2 when it crosses over layer M1. Details of the various developed structures are available in [14].
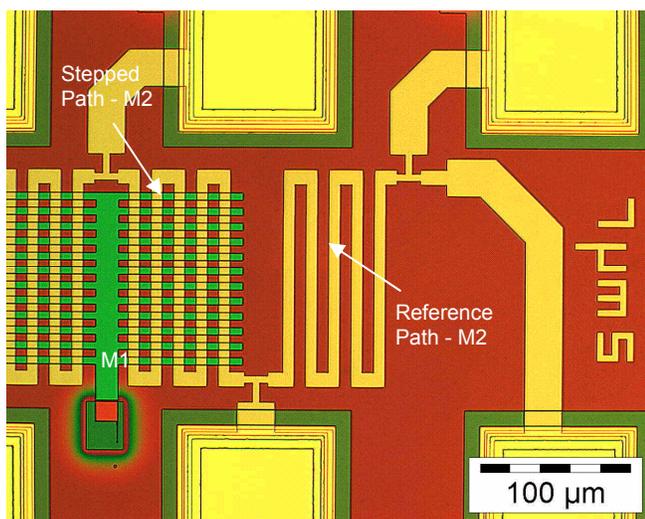
B. Test Implementation for JeSEF test-chip

Fig. 3. Photograph of the test-structure for detecting a crack in M2 layer implementing the v/d Pol structure.

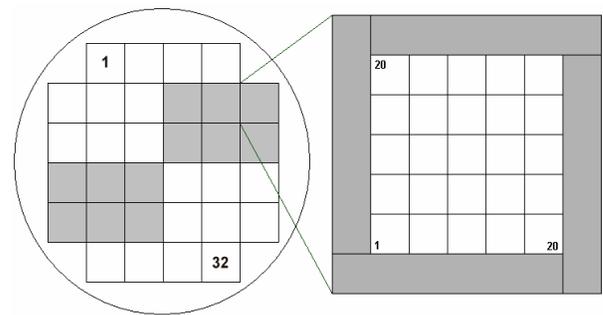The designed test-chip was processed at JeSEF. Fig. 4

Fig. 4. a) Diagram of a 6" SCE wafer showing the layout of chips. The shaded ones represent the test-chips to study the structural defects. b) The outline of the chip showing the arrangement of the structures.

shows the overview of the 6" wafer and the test-chip. There are 32 standard slots of 12.8 x 12.8 mm^2 available on the wafer. Twelve test-chips were placed in a wafer. In Fig. 4a, the shaded portion shows the position of the test chips. There are 100 test structures in each test-chip. In the test chip, the location of the test structures was divided into 5 blocks of 4 test structures each as shown in Fig. 4b.

All measurements are being performed on an Electroglass X2001 semi-automatic probe station. This measurement set-up is positioned in a light-tight box. The X2001 probe station has a 6" hot-chuck and a temperature controller Temptronic TP315 is available in the set-up. The TP315 has a temperature range of 0°C-200°C with resolution of 0.1°C. A 2 x 10 probe card is used for measurements. It is first manually positioned to the reference structure of the first chip to be tested on the wafer. After positioning, a program called Integrated Circuit Measurement System (ICMS) controls the automatic measurement. ICMS controls the positioning of the probe on the die as well as the type of test to be performed depending on the test-structure.

The electrical measurements are performed by an HP4141B Modular DC Source/Monitor and an HP3456A 6½ digit Digital Voltmeter. In combination with an HP4084B Switching Matrix Controller, the corresponding structure to be tested is selected. ICMS determines how the connections are made to different test structures via the switching Matrix connected to the probe card. The four-point measurement schemes of the test structures were implemented in ICMS. Measurements were carried out by injecting a fixed current to the structures. Depending on the sheet resistance of the material (Nb) and length of the wire, the expected resistance value is calculated. Based on the symmetry of the structures, each measurement results in the same resistance with an allowed parametric deviation (5% for metal layer resistances). A large deviation of the measured value from the expected value shows the
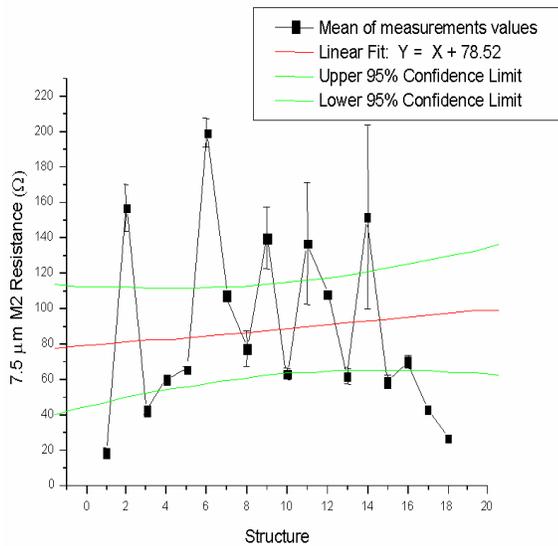
Fig. 5. Measurement results on the test-structure for detecting step-coverage problems in M2 layer showing the presence of huge parametric variation and structural defect.

presence of a defect.

IV. ANALYSIS AND MEASUREMENT RESULTS

The raw test data produced by the tester is sorted using a Unix shell script and is further analysed using MATLAB. The shell script separates data from the raw output file and groups them into similar ones. The MATLAB m-files for data analysis handle the data and perform statistical tests to identify the detected defects. The data is also graphically analysed using the Origin Graphics package for data analysis. In the future, all the above steps will be integrated into MATLAB m-files for convenient analysis.

Examples of such generated graph plots are shown in Fig. 5 and Fig. 6. They graphically show the measurement analysis of the meander structure shown in Fig. 3. Fig. 5 shows the measurement from a chip that suffered parametric variation. The central line gives the linear fit of the data and the upper and lower curves shows the area in which the probable good structures due to parametric variation can be found. The data points outside these curves shows the presence of the structural defect sites. Fig. 6 shows a classic example of the detection of a structural (random) defect using our test-structure. This is also the same type of structure as shown in Fig. 3, but from a parametrically good chip location. The defect location can be further analysed using SEM to verify the defect.

A summary of test results conducted on processed test-chips in the JeSEF process is given in table II. The first row shows the total number of structures tested in
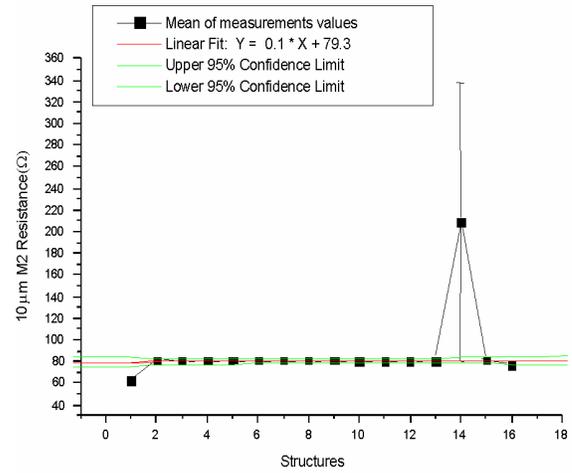

Fig. 6. Measurement results on the test-structure showing the presence of a structural defect – in this case a crack in wiring layer M2.

each category, followed by the number of detected defective structures. The third rows give the percentage of defective structures. Results from the M2 over M1 meander structures (Fig. 3) for 5 μm, 7.5 μm and 10 μm wire width of M2 are given in the second to fourth columns. The last column gives the statistics for the probability of an M2 wiring problem over a via. The results show that cracking of the metal wiring layer is a crucial problem in the SCE process.

V. THE INFLUENCE OF A CRACK IN LOGIC CIRCUITS

We are developing a DOT methodology for SCE circuits. As a part of the research, fault models have been developed and being used for IFA of digital

Table: II
Statistics on the test structures

Structures / Statistics	M2 over M1 Meander			M2 over via
	5 μ	7. 5 μ	10 μ	
No. of structures	3008	2256	2256	3008
No. of defective structures	476	375	412	2123
% of defective structures	15.82	16.62	18.26	70.58

circuits. Although fault models have been proposed, they are not yet verified. Our current study is on the verification of these fault models. Currently, faults are modelled as resistors to insert opens, near opens and shorts in the circuit. This is based on the fact that the resistance of a wiring layer changes if a defect is present.
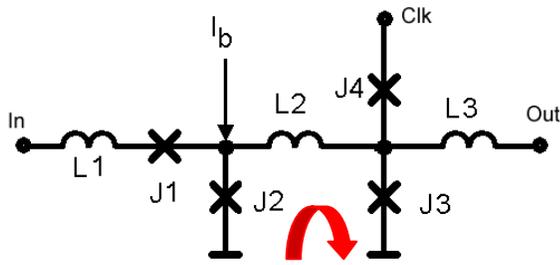
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Fig. 7. Schematic of an RSFQ D-type Flip-Flop in JeSEF technology that is used for the study of influence of cracks in SCE circuits.

This has been verified by our test structures.

In this paper, we present the study on the influence of a crack in a logic circuit. The circuit under test is a D-type Flip-Flop (DFF). We have presented an extensive study on DOT of an RSFQ DFF in [16]. The circuit diagram is shown in Fig. 7. It consists of 4 JJs (shown as 'X' in the schematic) and 3 inductances. One of the probable defects, a crack in the storage inductance will be discussed in detail.

From the layout of the JeSEF DFF, it can be seen that the wiring layer M2 crosses M1 twice in storage inductance L2. Due to its relative large area in the layout, it is realistic to assume a defect in L2. As the primary concern is cracking in a wiring layer, we concentrate on such a defect. The influence of a crack in the L2 is analysed by simulations. This has to be verified by the actual implementation of a defective device.

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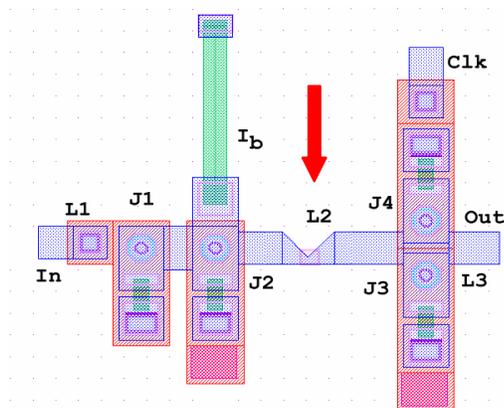

Fig. 8. Layout of DFF circuit designed in JeSEF process showing the induced defect to emulate a crack in the wiring layer.

by the actual implementation of a defective device.

The implementation of a defective device is achieved by insertion of the defect in the layout. A crack introduces a resistance in the flow of current in the circuit. This is achieved by reducing the wire-width at the point of interest as shown in Fig. 8. The line-width of M2 for L2 is 11μm. It is reduced to 2.5 μm, half of the minimum width for M2. The isolation under the smallest dimension area is removed to intensify the effect. The expected simulated behaviour of the circuit is shown in Fig. 9.

The bottom plot in Fig. 9. shows the fault-free operation of an RSFQ DFF. The other plot refer to the change in output as the severity of the defect increases. At the threshold of the defect, when the resistance effect from the crack is 318.5 mΩ, the output is delayed by about 40 ps shown by "Out2" in Fig. 9. Further increase in the resistance will ultimately lead to the wiring to go into the resistive state from superconducting state, thereby making the DFF to stop functioning, shown in "Out4" of Fig. 9. A test chip is being developed in which the defect-induced DFF will be processed. The correctness of our fault modelling will be known after the experimental analysis on the processed chips.
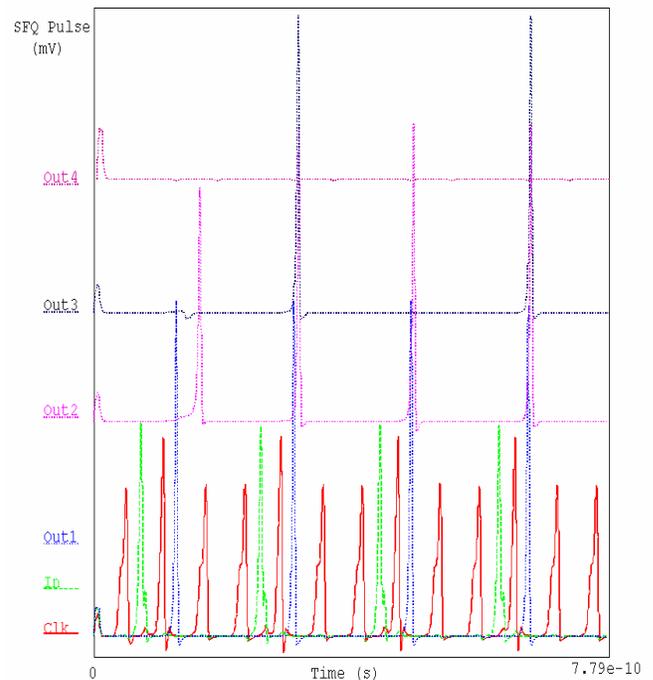

Fig. 9. Expected behaviour of the DFF circuit with the induced defect (crack in M2 wiring layer – storage inductor).

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VI. CONCLUSION

We have developed a DOT methodology for IFA in SCE circuits. The statistical information from the developed test-structures proved that they are capable of extracting defect information for SCE circuits being processed at JeSEF. Information about yield in the JeSEF process is available from these results. The measurement results also showed that a crack in the wiring layer is a highly probable defect in the process. Further research showed that such a crack in the wiring layer has major impact on logic circuits.

We have also started research into the correctness of our fault-models. This is achieved by processing circuits with deliberately inserted defects in them. A test chip is being developed for this purpose. Verification of these fault-models will be carried out after the chip is processed. Further studies on verification and experimental results from the test-chips are subject of a future paper.

ACKNOWLEDGMENT

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