

A 110MHz CMOS TRANSCONDUCTANCE-C LOW-PASS FILTER

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ABSTRACT

A CMOS third order elliptic low-pass filter with a 110MHz cut-off frequency realized in a $3\mu\text{m}$ -process is presented. The filter consists of differential transconductance elements and capacitors. The transconductance element has good linearity properties and an excellent high frequency behaviour thanks to the *absence of internal nodes*. Both the cut-off frequency and the Q-factors can be tuned.

INTRODUCTION

The integrator forms the main building block of active filters. In this paper the integrator is implemented by a transconductance element loaded with a capacitor. One of the major problems in high-frequency active filters is the phase error of the integrators [1]. This requires a sufficiently high dc-gain and parasitic poles located at much higher frequencies than the cut-off frequency of the filter. For the filter presented here this implies roughly a dc-gain of minimal 40dB and parasitic poles located a factor 100 beyond the cut-off frequency. Recently several CMOS filters for video frequencies (4MHz) have been presented [2,3]. This paper presents a filter for a much higher frequency (110MHz). It was possible to achieve this frequency by using a linear transconductance element *without internal nodes* [4].

THE TRANSCONDUCTOR

The transconductor schematic is given in figure 1a. It consists of six CMOS inverters, which are for the moment all assumed to be equal ($V_{dd} = V_{dd}'$). The basic V-I conversion is performed by two CMOS inverters Inv1 and Inv2. If these inverters are driven by a differential input voltage V_{id} , balanced around the common mode level V_C (see fig. 1b), the differential output current will be linear with the differential input voltage. This can be shown as follows: If the drain currents of an n-channel and a p-channel enhancement MOS transistor in strong inversion and saturation are written as:

$$I_{dn} = \frac{\beta_n}{2} (V_{gs} - V_{tn})^2 \quad \text{and} \quad I_{dp} = \frac{\beta_p}{2} (V_{gs} - V_{tp})^2, \quad (1)$$

the differential output current of the two inverters can be manipulated into the form:

$$I_{od} = I_{o2} - I_{o1} = V_{id} (V_{dd} - V_{tn} - |V_{tp}|) \sqrt{\beta_n \cdot \beta_p} = V_{id} \cdot g_{md}. \quad (2)$$

Hence the differential transconductance (g_{md}) is linear, *even with nonlinear inverters*, i.e. if $\beta_n \neq \beta_p$. However closely matched β_n and β_p is attractive because this reduces the common mode output currents. The transconductance can be tuned by means of V_{dd} .

The common mode level of the output voltages V_{o2} and V_{o1} is controlled by the four inverters Inv3-Inv6. Inv4 and Inv5 are shunted as resistors $1/g_{m4}$ and $1/g_{m5}$. The output currents of Inv3 and Inv6, $g_{m3}(V_C - V_{o1})$ and $g_{m6}(V_C - V_{o2})$ respectively, are injected into these resistors. The result for common signals is that the " V_{o1} " node is loaded with a resistor $1/(g_{m5} + g_{m6})$ and the " V_{o2} " node with a resistor $1/(g_{m3} + g_{m4})$. For differential signals the " V_{o1} " node is loaded with a resistor $1/(g_{m5} - g_{m6})$ and the " V_{o2} " node is loaded with a resistor $1/(g_{m4} - g_{m3})$. If the inverters have the same supply voltage and geometry, all the g_m 's will ideally be equal. Thus the network Inv3-Inv6 forms a low-ohmic load for common signals and a high-ohmic load for differential signals, resulting in a controlled common mode voltage level of the outputs.

The DC-gain of the transconductor-C integrator has been increased by loading the differential inverters with a negative resistance for differential signals. By choosing $gm_3 > gm_4$, $gm_5 = gm_4$ and $gm_6 = gm_3$ this negative resistance, $1/\Delta gm = 1/(gm_4 - gm_3) = 1/(gm_5 - gm_6)$, is simply implemented, without adding extra nodes to the circuit. The width of the transistors in Inv4 and Inv5 is designed slightly smaller than those of Inv3 and Inv6. In order to obtain a more exact filter response, the DC-gain of the integrators is fine-tuned during operation (Q-tuning) with a separate supply voltage V_{dd}' for Inv4 and Inv5. Thanks to the feedback loops in the filter the integrator will remain stable, even if the net output resistance of the transconductance element becomes negative.

The W/L ratios of the n-channel devices in the transconductor are $24\mu\text{m}/3\mu\text{m}$ for Inv1, Inv2, Inv3, Inv6 and $21\mu\text{m}/3\mu\text{m}$ for Inv4 and Inv5. The width of the p-channel devices are in all cases a factor three larger. This transconductor circuit has a large bandwidth thanks to the absence of internal nodes. The effective parasitic poles are due to the finite transit-time of carriers in the MOS channel and are located in the gigahertz region.

A 110MHz CONTINUOUS-TIME FILTER

The transconductance element described above was used to realize a third order elliptic low-pass filter. The normalized passive prototype circuit of this filter is given in figure 2. The active implementation is given in figure 3. The inductance is simulated by a gyrator (G3-G6) loaded with a capacitor (C_2, C_2'). The resistors are implemented also with transconductances (G2 and G7). The capacitances are chosen in such a way that C_1 and C_1' are completely constructed by the parasitic capacitances at the nodes 1 and 1'. The other capacitances are designed by adding small capacitors to the parasitic capacitances at the nodes. The parasitic capacitances at the nodes of fig. 3 however consist for 70% of gate oxide capacitances and are quite linear. The time-constants of the filter can be written in the form $\tau = C/gm$ where gm is linear with C_{ox} and C is almost linear with C_{ox} . The spread in τ due to spread in C_{ox} is therefore small, resulting in quite accurate fabricated time constants. The cut-off frequency of the filter is manually tuned by means of V_{dd} and the Q-factors are -also manually- tuned with V_{dd}' . The cut-off frequency was simulated as 80MHz for $V_{dd} = 5V$. The filter was processed in a $3\mu\text{m}$ BICMOS process using only the CMOS part. The threshold voltages are $V_{tn} = 0.75V$ and $V_{tp} = -0.80V$. The chip area required for the filter is 0.63mm^2 . The chip photograph is given in figure 7.

EXPERIMENTAL RESULTS

The measured transconductance of the transconductor of figure 1 is given in figure 4. The nonlinearities are mainly due to mobility reduction. For $V_{dd} = 10V$ 1% error in transconductance occurs at $V_{id} = 1.0V$. For $V_{dd} = 5V$ the filter cut-off frequency was measured as 71 MHz, this value is within 11% of the predicted frequency. If V_{dd} is increased to 10V the cut-off frequency becomes 110MHz as predicted by simulation. The measured filter transfer function for $V_{dd} = 10V$ and the ideal response of the passive prototype are given in figure 5. The passband ripple is 0.8dB (0.28dB for the passive prototype) The notch in the stopband was also measured, which implies a good phase behaviour of the transconductor up to 380 MHz. The notch frequency, however, is too high. This is due to the capacitors C_4 and C_4' which have been fabricated too small. The cut-off frequency varied from 108 to 117 MHz over 15 chips ($\pm 4\%$ spread). The experimental results for $V_{dd} = 5V$ and $V_{dd} = 10V$ are summarized in table 1. The Total Harmonic Distortion (THD) of the complete filter for input signals at 1kHz is given in figure 6.

CONCLUSIONS

A 110 MHz CMOS continuous-time low-pass filter realized in a $3\mu\text{m}$ -process is presented. The filter is constructed with transconductance elements and capacitors. The transconductance element has parasitic poles in the gigahertz region *thanks to the absence of internal nodes*. The linearity of the transconductance element is good (1% deviation from transconductance at 1.0V input voltage). The measured filter has a frequency response close to the theoretical response. The cut-off frequency and the Q-factors can be tuned by means of two supply voltages. Future research will focus on frequency- and Q-tuning circuits suitable for these frequencies, including a power-supply circuit, for automatically tuning V_{dd} and V_{dd}' .

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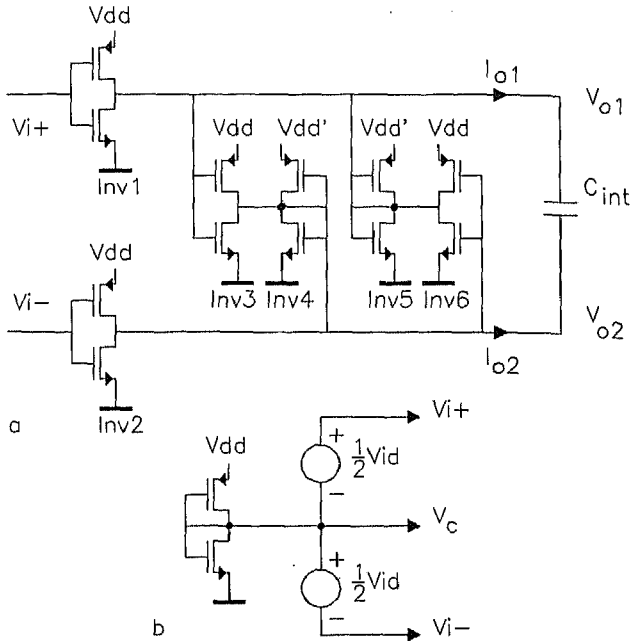


fig.1 a) transconductance element
b) definition of input signals

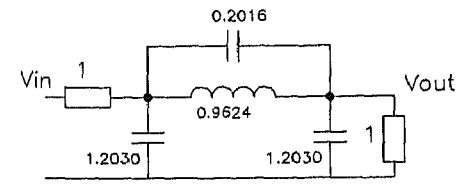


fig. 2 Normalized passive prototype of the third order elliptic filter

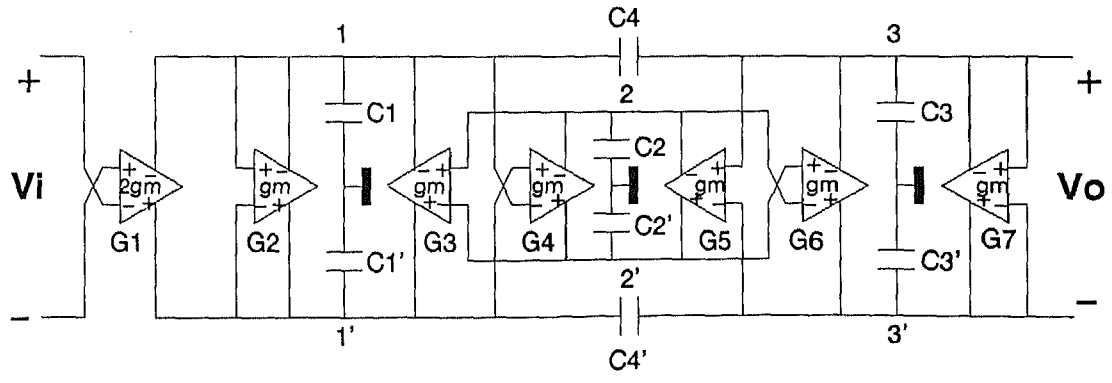


fig.3 Active implementation of the filter

- C1 = C1' = 2.448pF
- C2 = C2' = 1.958pF
- C3 = C3' = 2.448pF
- C4 = C4' = 0.410pF

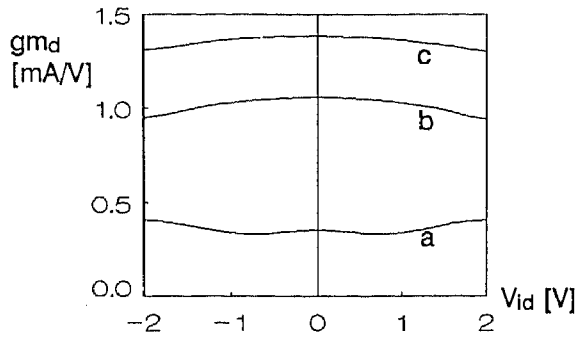


fig. 4 Measured transconductance for:
a) $V_{dd} = 2.5V$ b) $V_{dd} = 5V$ c) $V_{dd} = 10V$

Parameter	$V_{dd} = 5V$	$V_{dd} = 10V$
cut off frequency	71 MHz	110 MHz
passband ripple	0.6 dB	0.8 dB
V_{dd}'	4.66 V	8.16 V
total passband input noise	$81 \mu V_{RMS}$	$96 \mu V_{RMS}$
dyn. range	73 dB	78 dB
CMRR-passband	40 dB	40 dB
power dissipation	77 mW	670 mW

Table 1. experimental results

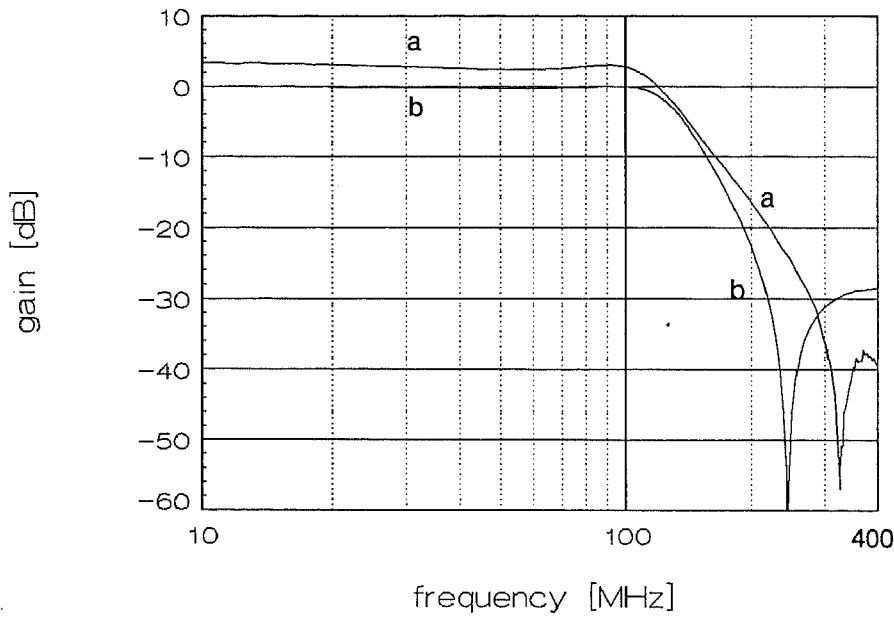


fig. 5

a) measured filter response ($V_{dd} = 10V$)

b) ideal response

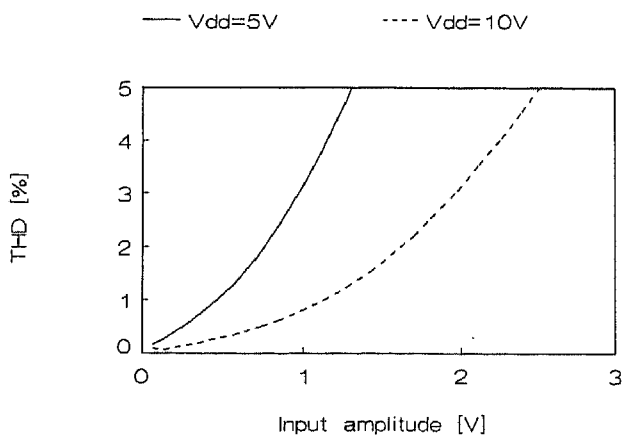


fig. 6 THD of the filter for 1kHz input signals

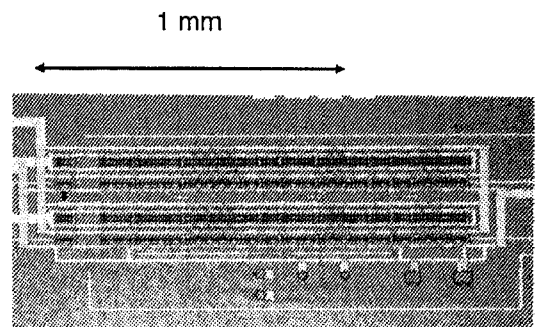


fig. 7 Chip microphotograph