Evaluation of Transmission Line Model Structures for Silicide-to-Silicon Specific Contact Resistance Extraction

Natalie Stavitski, *Student Member, IEEE*, Mark J. H. van Dal, Anne Lauwers, Christa Vrancken, Alexey Y. Kovalgin, and Rob A. M. Wolters

***Abstract*—In order to measure silicide-to-silicon specific contact resistance ρ_c, transmission line model (TLM) structures were proposed as attractive candidates for embedding in CMOS processes. We optimized TLM structures for nickel silicide and platinum silicide and evaluated them for various doping levels of n- and p-type Si. The measurement limitations and accuracy of the specific contact resistance extraction from the optimized TLM structures are discussed in this paper.**

***Index Terms*—Nickel silicide (NiSi), platinum silicide (PtSi), silicide, specific contact resistance, transmission line model (TLM).**

I. Introduction

LOW-RESISTANCE "ohmic" contacts to silicon have been of considerable technological interest for the past few decades [1]–[3]. The field of low-resistance contacts to semiconductors comprises two main areas: 1) materials science aspects for choosing the appropriate materials and related processing and 2) the electrical characterization, which includes a proper definition of contact resistance and its measurement techniques. The self-aligned silicide (SALICIDE) process is commonly used to reduce the source, drain, and gate resistances in submicrometer metal–oxide–semiconductor (MOS) devices [1], [4]. Nickel silicide (NiSi) is being used as the silicide of choice for complementary MOS (CMOS) devices in the 90-nm technology node and beyond [5]. NiSi has several advantages over titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$). These advantages include low sheet resistance on narrow lines and low silicon consumption [6]–[11]. The latter is important for the formation of contacts to ultrashallow source/drain junctions.

As device dimensions are shrinking with technology nodes, contact resistance values increase. The contact and metallization processes have to scale accordingly and, therefore, become increasingly important [1], [3]. For the contact process, the specific contact resistance is a crucial parameter. A well-defined method for extraction of its value is required.

Several methods for contact resistance measurement, such as the cross-bridge Kelvin resistor (CBKR) [12], [13], the circular transmission line model (TLM) [14], the transfer length method [15], and the two-terminal resistor structures [15], were introduced in the past.

In recent years, there has been a trend toward using TLM structures as they can more easily be embedded in the standard SALICIDE CMOS process. The advantage of the TLM structure over the CBKR structure is that, in TLM structures, the silicide segments and the contact pads are made in one single silicide process step. An attractive method for the direct contact resistance measurement of silicide-to-silicon contacts and the extraction of the specific contact resistance was proposed by Scott *et al.* [16]. This method was extensively evaluated for $TiSi_2$, demonstrating its advantages, including the relative simple processing of the test structures [16]. However, until now, very little attention has been paid to the evaluation of these structures for NiSi and the other important silicides [e.g., platinum silicide (PtSi), which was used in the fabrication of Schottky barrier devices [17]]. Furthermore, issues such as short contact (silicide) lengths, n- or p-type Si, and a wide range of dopant concentrations were not discussed.

For these reasons, a set of optimized TLM test structures was designed and realized with NiSi and PtSi contacts to silicon. The electrical characterization and evaluation of these structures for various doping concentrations of n- and p-type Si at different measurement temperatures were performed.

II. Test Structure Optimization

Silicide-to-silicon contact resistance is investigated using a set of optimized test structures. Each TLM structure consists of fragments with silicided segments of varying lengths and the reference fragment, which is not interrupted by silicide segments. The optimization is done in terms of the silicide lengths and the number of segments. The measurement technique involves forcing a current through the reference fragment. In the same manner, the current is forced through the fragments interrupted by n silicided segments, and the voltage drop across each fragment is measured. As the fragments have been

Manuscript received December 13, 2007; revised February 1, 2008. This work was supported by NXP Research Leuven. The review of this paper was arranged by Editor C.-Y. Lu.

N. Stavitski and A. Y. Kovalgin are with the MESA+ Institute for Nanotechnology, Chair of Semiconductor Components, University of Twente, 7500 Enschede, The Netherlands (e-mail: n.stavitski@utwente.nl).

M. J. H. van Dal is with NXP/Taiwan Semiconductor Manufacturing Company Research Center, Leuven, 3001 Leuven, Belgium.

A. Lauwers and C. Vrancken are with the Interuniversity Microelectronics Center, 3001 Leuven, Belgium.

R. A. M. Wolters is with the MESA+ Institute for Nanotechnology, Chair of Semiconductor Components, University of Twente, 7500 Enschede, The Netherlands, and also with NXP Research Eindhoven, 5656 Eindhoven, The Netherlands.

Digital Object Identifier 10.1109/TED.2008.918658

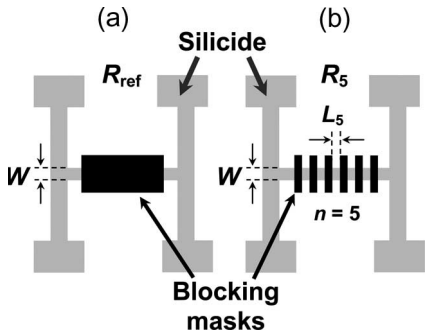

Fig. 1. (a) Reference fragment of the TLM structure (i.e., to measure $R_{\rm ref}$), not interrupted by silicide segments. (b) Example of one fragment of the TLM structure interrupted by five silicide segments, where L_5 is the segment length, and R_5 is the measured resistance of this fragment.

designed to have equal silicided and nonsilicided segment lengths, the difference between the reference resistance and the other resistances is attributed to the contact resistance contribution [16] and can be expressed as

$$R_c W = \left(\frac{R_n - R_{\rm ref}}{n}\right) W \tag{1}$$

where R_n is the resistance of the fragment interrupted by n silicided segments, $R_{\rm ref}$ is the resistance of the reference fragment, and W is the silicide width (Fig. 1).

The theoretical expression of the silicide-to-silicon contact resistance for the test structure, as stated by Scott *et al.* [16], is given by

$$R_c = \frac{2\sqrt{\rho_c R_s}\tanh(L/2L_{\rm c})}{W} \tag{2}$$

where R_s is the sheet resistance under the silicide, W is the structure width, and L is the length of the silicided segment. L_c is the transfer length.

Equation (2) for $L \gg L_c$ reduces to

$$R_c = \frac{2\sqrt{\rho_c R_s}}{W} = R_0 \tag{3}$$

where R_0 is the saturation resistance level [16].

The specific contact resistance can then be extracted from

$$\rho_c = L_c R_0 W/2. \tag{4}$$

A known accuracy problem of this method, while measuring low values of contact resistance, is the relatively small difference between $R_{\rm ref}$ and R_n in (1) that might result in a low $(R_n - R_{\rm ref})$ value and, hence, an increased calculation error. This error might be reduced by increasing the number of silicide segments n per each fragment of the TLM structure, which would cause higher R_n values, reducing the relative error during the R_c calculation. To optimize the TLM structures, we increased the number of silicide segments per fragment from $n = 1, 2, 6, 12, \ldots, 60$ for the old structures [18] to $n = 5, 10, 15, 30, \ldots, 150$. The design is chosen such that the total amount of metal for silicide formation is the same for each fragment.

Another factor that affects the accuracy of ρ_c extraction is the nonuniform distribution of the points on the $R_c W(L)$ graph in (2). Based on our previous experience [18], we adjusted the lengths of the silicide segments L to improve this uniformity. In addition, our TLM structures had two different silicide widths W. The values of R_c should be related to the corresponding silicide width in (2) according to

$$R_{\rm c1} W_1 = R_{\rm c2} W_2. \tag{5}$$

Therefore, by varying W, the measurement results can be verified, and more statistical data can be provided to make a better fit.

Another complication of the data analysis is that the actual silicide lengths always deviate from the blocking mask dimensions. In our previous paper [18], two different techniques, i.e., i-line and e-beam lithographies, were used to define the feature dimensions. The present optimized structures were realized by using only deep ultraviolet (DUV) lithography to minimize the size mismatch caused by the two different techniques.

Summarizing the above considerations, the optimized TLM structures are comprised of areas with two different silicide widths W of 2 and 8 μm and silicide lengths L ranging from 0.1 to 3 μm. Thus, each TLM structure consisted of a reference fragment without silicide segments and a number of fragments where each fragment is composed of n silicided segments of length L. The numbers of segments n were 5, 10, 15, 30, 60, 75, 100, and 150.

III. Test Structure Fabrication

The (100) p-type Si wafers were used as a starting material for the contact resistance study. The active areas were defined by shallow trench isolation, and the implanted regions were defined by i-line lithography. Doping concentrations were achieved by low-dose well implantations of B (180 keV) or P (420 keV) for the p- or n-well, respectively. Arsenic (As) and B implantations, followed by spike annealing at 1100 °C, were carried out for n-type highly doped drain (NHDD) and p-type highly doped drain (PHDD) areas. The doses and energies were adjusted to cover the $10^{17}-10^{20}$ cm^{-3} doping concentration range. In order to verify the actual concentrations, the same implantation recipes were applied to blanket wafers, and the total doping concentration and the concentration of electrically active impurities were determined by secondary ion mass spectrometry and the spreading resistance probe technique, respectively. The relevant active concentrations used in this paper were taken at the depth of 20–30 nm, as the upper silicon layer was consumed during the silicide formation. Deep junctions were chosen in order to enable an accurate measurement of the doping profiles and, therefore, to minimize errors during the extraction of the specific contact resistance. Moreover, the sheet resistance of deeper junctions is less sensitive to changes due to the silicon consumption during silicide formation and to the variations of the doping profile in the area of silicide/silicon junction.

For the TLM structures, a silicide-blocking layer (SiO_2/Si_3N_4), representing the standard Si protection in the

SALICIDE process, was deposited and patterned on the NHDD and PHDD areas using DUV lithography. Finally, a 10-nm-thick Ni layer or a 13-nm-thick Pt layer was deposited, and the silicide was formed by either two-step annealing (300 °C for 43 s, followed by 470 °C for 43 s) for NiSi or one-step annealing (500 °C for 30 s) for PtSi. In both cases, the unreacted metal was selectively removed by wet etching.

IV. Results and Discussion

The actual silicide lengths and the shape of the silicide/silicon interface for NiSi and PtSi were verified by transmission electron microscopy (TEM) analysis using an FEI Tecnai F30ST TEM operated at 300 kV. The samples were prepared by a combination of mechanical polishing and the FIB200 technique (focused ion beam). A low-temperature plasma-enhanced chemical vapor deposition silicon nitride layer and a sputtered Pt layer were deposited prior to the sample preparation for a better image contrast and to avoid charging.

Both silicides revealed good quality in terms of uniform silicide formation within the segments [Fig. 2(a)]. The silicide segment lengths were always larger than the corresponding blocking mask dimensions due to the lateral growth of the silicide [Fig. 2(b)]. This growth (ΔL) varied from 0.025 to 0.035 μm for NiSi and from 0.035 to 0.05 μm for PtSi on each side of the segment. The actual silicide length was independent of the doping type and concentration. For the smallest segments, the lateral growth of PtSi became comparable with the designed spacing between the silicides. In some cases, this led to a short circuit or a complete merge of the silicide segments [Fig. 2(c)]. As a result, these fragments showed a much lower R_c and were therefore taken out of the analysis. Although this problem did not compromise the data analysis, in the next generation of TLM structures with similar dimensions, for silicides with a relatively large lateral growth, spacing between the smallest segments should be at least twice the expected lateral growth $(2\Delta L)$. For example, if the smallest spacing is 0.1 μm with an expected $\Delta L_{\max}$ of 0.05 μm, the contribution to the total growth is the same $(2 \times \Delta L_{\max} = 0.1\ \mu\text{m})$. To yield valid fragments, the spacing should then be preferably twice the total growth, i.e., $2 \times 2\Delta L_{\max} = 0.2\ \mu$m. An additional method for reducing this effect could be the reduction of the silicide segment width W (Fig. 1).

In our case, the amount of such abnormal fragments for PtSi for $W = 2\ \mu$m was much smaller than that for $W = 8\ \mu$m, obviously reducing the probability of the merge effects.

PtSi segments were equally thick, independent of the segment length or the doping type [Fig. 2(a)]. However, in the case of NiSi segments, homogeneous thickness distribution was confirmed for the PHDD area only, whereas for the NHDD area, silicide segment thickness deviations of 20%–30% were observed [Fig. 2(d)].

It should be noted that it was not possible to perform a valid fit of the measured data by the Scott method without knowing the exact silicide lengths for the small segments. This underlines the importance of the profile verification by TEM.

The measurements of each TLM fragment (with a given n and L) resulted in two sets of I–V curves: $W = 2\ \mu$m and $W = 8\ \mu$m. In Fig. 3, the I–V curves for identical fragments, measured at 18 different locations on the wafer, are presented.

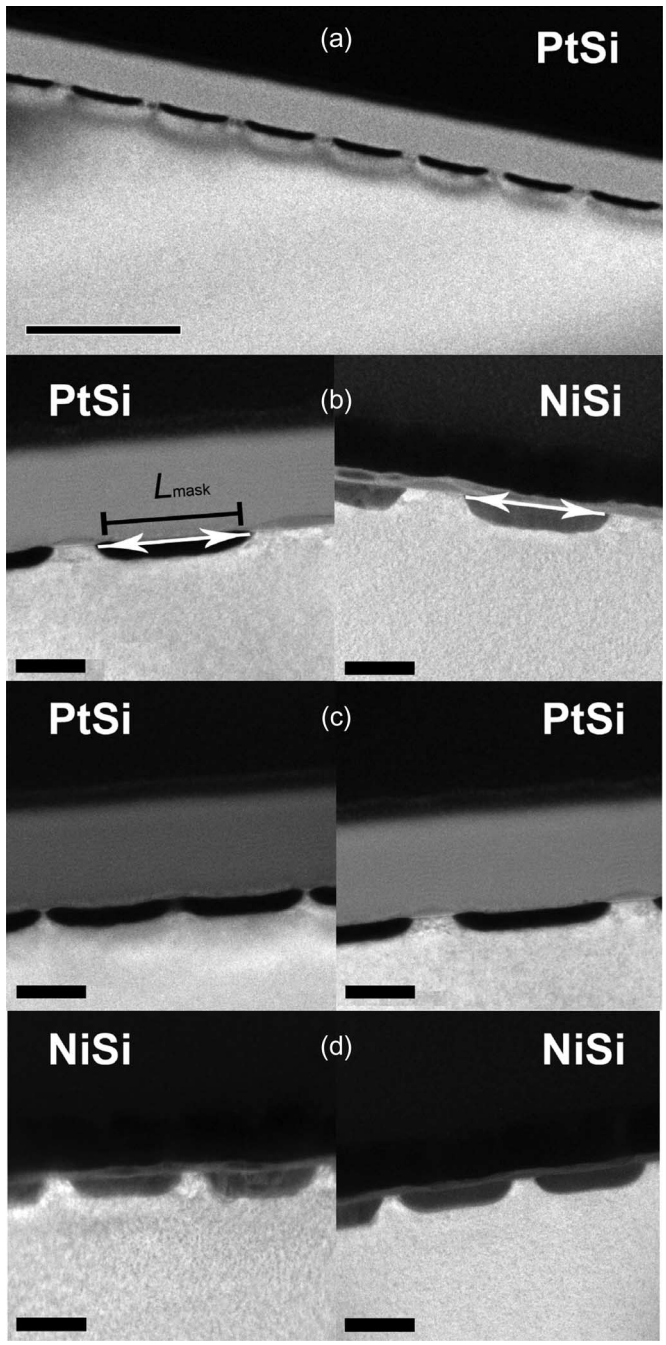

Fig. 2. (a) TEM cross section of PtSi on NHDD for $n = 100$. (b) Arrows represent PtSi and NiSi (PHDD, $L_{\text{mask}} = 0.2\ \mu$m) actual silicide lengths and show the lateral expansion. The arrows depict the location where the length was measured. (c) PtSi merged segments for $n = 150$ (left) and nonmerged segments for $n = 100$ (right). (d) NiSi segments for $n = 150$, nonequally thick on NHDD (left) and equally thick on PHDD (right). Scale bar equals 0.5 μm (a) and 0.1 μm (b, c, and d).

The resistance values (i.e., R_{ref} and R_n) of all the fragments were extracted from such I–V curves, and the R_c values were calculated using (1). The R_cW product (i.e., the R_c values normalized to the silicide width) versus the silicide length was plotted for different W's to verify the validity of (5) and to extract the specific contact resistance. The fits for the NiSi and

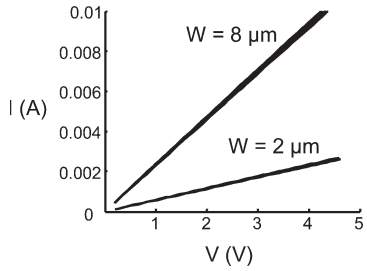

Fig. 3. Two sets of I–V curves for NiSi on a PHHD ($N_a = 1.4 \cdot 10^{20}$ cm^{-3}) fragment with $n = 30$. Each set corresponds to a given silicide width, i.e., $W = 2$ μm and $W = 8$ μm.

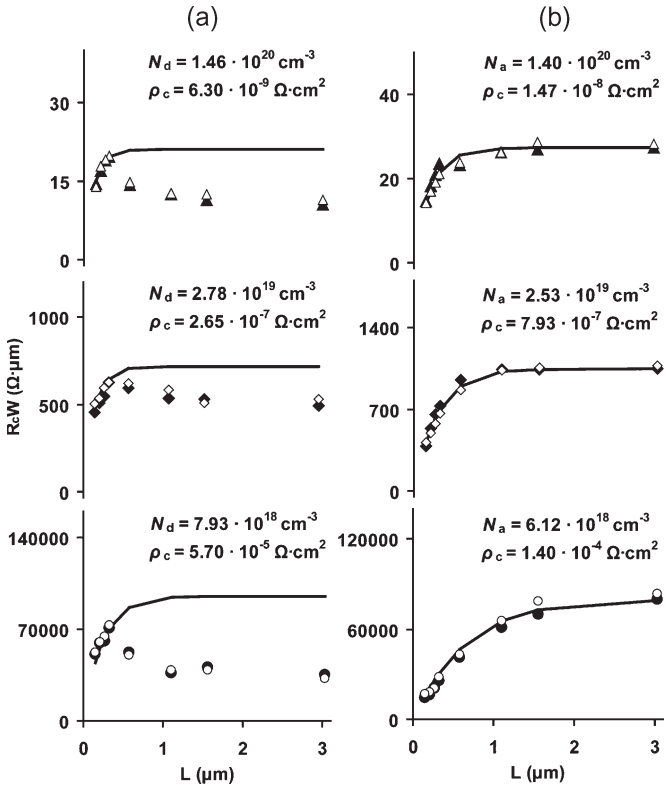

Fig. 4. Contact resistance values for NiSi contacts to (a) NHDD and (b) PHDD areas for different doping levels (N_a and N_d). Solid symbols represent measured data for silicide width $W = 2$ μm, and open symbols are for $W = 8$ μm. Each symbol type corresponds to a certain doping level. Lines are fits, obtained by the Scott method from which ρ_c is extracted.

PtSi contacts to the NHDD and PHDD areas were evaluated for different doping levels (Figs. 4 and 5). The two Scott regimes, i.e., for L comparable with L_c in (2) and for $L \gg L_c$ in (3), were observed. For PtSi-to-PHDD contacts, the R_cW was constant for $L > 1$ μm according to (3), whereas for $L < 1$ μm, the R_cW was L dependent according to (2) [Fig. 5(b)]. The L_c values for PtSi ranged from 0.08 to 0.122 μm, depending on the PHDD doping level. The R_cW values obtained for the two different silicide widths matched very well for both silicides and for different doping types, indicating their validity. These values and the extracted ρ_c increased with decreasing doping concentration, as demonstrated in Figs. 4 and 5, in accordance with theory [3].

The measured data for NiSi-to-PHDD contacts agreed very well with the fit, obtained by the Scott method [Fig. 4(b)],

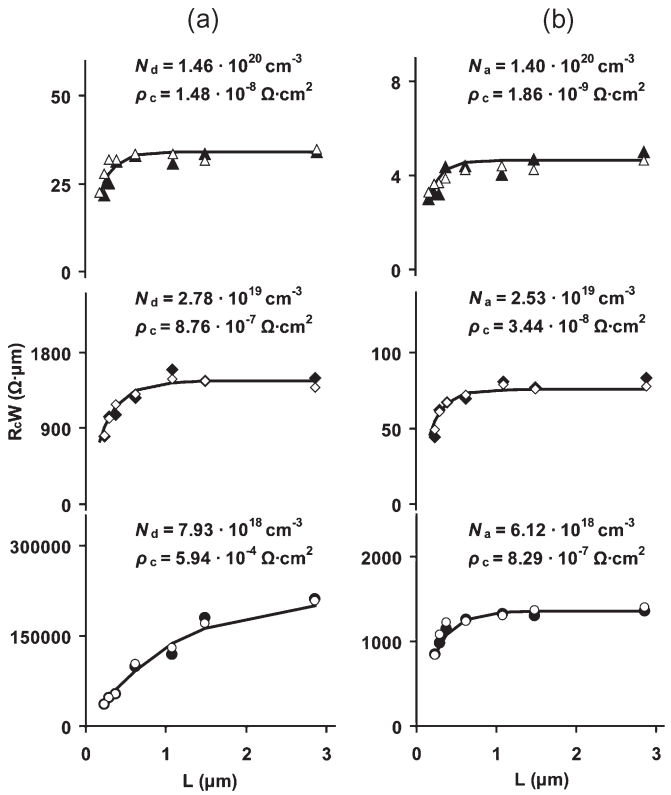

Fig. 5. Contact resistance values for PtSi contacts to (a) NHDD and (b) PHDD areas for different doping levels (N_a and N_d). Solid symbols represent measured data for silicide width $W = 2$ μm, and open are symbols for $W = 8$ μm. Each symbol type corresponds to a given doping level. Lines are fits, obtained by the Scott method from which ρ_c is extracted.

whereas in the case of NiSi-to-NHDD contacts, the agreement with the model was obtained for small silicide lengths L only. Starting from $L = 0.5$ μm, a disagreement appeared, and a deviation from the model was observed [Fig. 4(a)]. The results for PtSi to NHDD and P-HDD were both in agreement with the theoretical fit (Fig. 5). In these cases, the distribution of the measurement points on the theoretical fit is much more uniform, compared to our previous results [18], providing a better fit and a higher accuracy.

A number of factors can be considered to explain the deviation of the NiSi-to-NHDD contact resistance data from the Scott fit [see Fig. 4(a)]: the HDD doping type, the barrier height between silicide and Si, and the differences in silicide formation at the Ni–Si interface. As PtSi-to-NHDD contacts revealed good agreement with the model, the possibility of processing problems related to the NHDD must be excluded. Edge effects due to the patterning and cleaning process of the blocking mask and layout errors can be excluded as well because both the NHDD and PHDD areas were processed on the same wafers with the same DUV mask. The Schottky barrier between NiSi and NHDD cannot cause this deviation either, because for PtSi-to-NHDD contacts, a higher Schottky barrier is expected [17], and in this case, the deviation was not observed [Fig. 5(a)]. The fact that this deviation for NiSi-to-NHDD contacts was observed at all of the studied doping concentrations [Fig. 4(a)] indicated that the contact resistance value itself should not play a role in this case. Moreover, as expected from theory

and as experimentally proven in this paper, increasing the barrier height for a given doping concentration (or alternatively lowering the doping level for a given barrier height) would lead to a higher specific contact resistance. In terms of the Scott method, this would mean a higher saturation value for R_0 (3) but not the deviation from the theoretical fit, as shown in Fig. 4(a).

The most probable explanation for this deviation is the difficulty of silicide formation caused by the presence of As, as stated by Davari [19]. The Scott method is based on the assumption that all the segments are identical in terms of the silicide thickness. As shown in Fig. 2(d), a difference in NiSi thickness between NiSi segments on the same fragment was observed only for the NiSi formation on NHDD. From segment to segment, the NiSi thickness was not the same for $L = 0.1$ μm [see Fig. 2(d)]. Here, and for other small silicide lengths, the corresponding "electrical" silicide thickness would then be averaged over the large number of segments. The obstruction of silicide formation on n-type Si, caused by the presence of As [19], could lead to a distribution of areas with enhanced and retarded silicide formation (Ni diffusion) on a 0.1-μm length scale. In this case, for larger L ($>\sim 0.5$ μm), there is a larger effective area and, hence, a higher probability for silicide formation. This would lead to the formation of a thicker NiSi and, consequently, to a lower sheet silicide resistance for the larger segments. Then, a comparison of the fragments with the short and large L would result in a lower R_cW, as shown in Fig. 4(a). This effect was enhanced in our experiments by the low sheet resistance of the NiSi (7–8 $\Omega/\square$) compared to PtSi (25–26 $\Omega/\square$). The deviation from the theoretical fit was not observed for NiSi-to-PHDD and PtSi-to-NHDD/PHDD contacts because these silicide segments were uniformly grown.

A uniform formation of a silicide is a prerequisite for the reliable application of the TLM structures by the Scott method. Fortunately, for process development, this effect may serve as an indication of improper silicide growth in submicrometer structures.

The measurements were performed in the doping range of $10^{17}-10^{20}$ cm^{-3}. For the high doping concentrations, the I–V curves were perfectly linear, as the contacts exhibited ohmic behavior (see Fig. 3). In the mid doping range, however, the I–V curves were not perfectly linear. The observed nonlinearity was in agreement with the difference in the barrier heights between the silicides and Si. For the PtSi-to-NHDD contacts, the nonlinearity was observed for doping concentrations N_d less than $1 \cdot 10^{19}$ cm^{-3}, whereas for the PtSi-to-PHDD contacts, the nonlinearity was observed for $N_a < 5 \cdot 10^{18}$ cm^{-3}. In order to better verify the doping limits, the I–V curves were measured at 75 °C and 100 °C for the wafers falling in the mid doping range. The linear fit coefficients (R^2) were calculated for the I–V curves of all measured TLM fragments, showing an improved linearity as the temperature increased (Fig. 6).

For the mid range doping concentrations on the order of 10^{18} cm^{-3}, the contact resistances, defined as the reciprocal derivative of current density with respect to the voltage [3], were obtained from the I–V curves at room and higher temperatures, making it possible to apply the Scott method. As the temperature increased, the R_c values decreased, and the

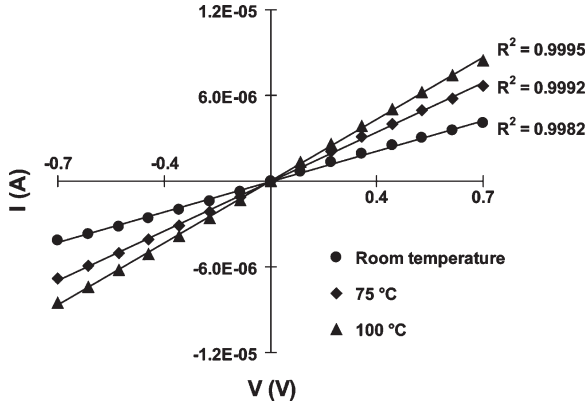

Fig. 6. I–V curves for NiSi on a PHHD ($N_a = 7.9 \cdot 10^{18}$ cm^{-3}) fragment with $n = 30$ silicide segments and a silicide width of $W = 8$ μm.

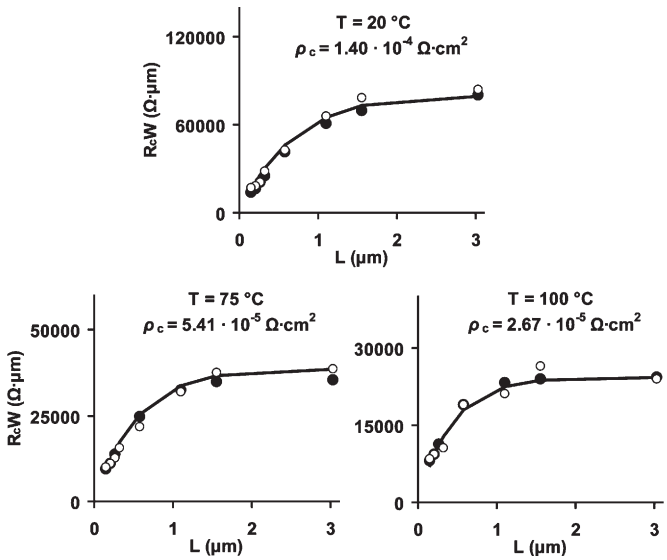

Fig. 7. Contact resistance values for PtSi-to-PHDD contacts at room temperature, 75 °C, and 100 °C with a doping concentration of $N_a = 7.9 \cdot 10^{18}$ cm^{-3}. Solid symbols represent measured data for $W = 2$ μm, and open symbols are for $W = 8$ μm. The lines are the fits obtained by (2).

fitting of the R_cW values could successfully be done. A good agreement for the two silicide widths was again demonstrated (Fig. 7). The extracted specific contact resistance values decreased with increasing temperature (Fig. 7), as expected from theory [3].

In addition, for the wafers with low doping levels, the linear fit coefficients R^2 increased, and the corresponding $R_{\rm ref}$ and R_n values decreased with increasing temperature. However, the calculated R_c values could not be used to extract the specific contact resistance because the R_n resistances obtained for different TLM fragments were identical to $R_{\rm ref}$. This result indicated that the current did not enter the silicide segments because of the Schottky barrier and only flowed through the HDD areas. Ultimately, this resulted in the same resistance value for the TLM fragments with n silicide segments and $R_{\rm ref}$, obtained from the fragment without silicide. Therefore, the lowest doping limits for obtaining ρ_c from the TLM structures can be determined.

Obviously, these limits are related to the corresponding Schottky barriers between silicide and silicon [17]. The limits are $4-5 \cdot 10^{18}$ and $2-3 \cdot 10^{18}$ cm^{-3} for NiSi grown on NHDD and PHDD silicon areas, respectively. For PtSi-to-NHDD contacts, this is $7-8 \cdot 10^{18}$ cm^{-3}. As expected, due to the lower Schottky barrier between PtSi and P-HDD silicon [17], the limit is also lower, i.e., $1-2 \cdot 10^{18}$ cm^{-3}.

V. Conclusion

Improved TLM test structures have been fabricated and characterized. The structures have been designed to provide a better fit and a higher accuracy using the Scott method and to verify the measurement data. The TLM structures have been evaluated for NiSi- and PtSi-to-silicon contacts in a broad range of doping concentrations. The ρ_c extraction method and the measurement drawbacks have been discussed in terms of the necessity of applying a TEM analysis and a uniform silicide formation. The TLM structures have been evaluated at different temperatures. The observed decrease in the ρ_c values with increasing temperature was in agreement with theory. The lowest doping concentrations of p- and n-type silicon, enabling the measurement of NiSi- and PtSi-to-silicon contact resistances, have been determined and found to be in agreement with theory.

This paper has provided an important reference for further use of TLM structures, which is also applicable to other silicides. It has contributed to the development of test structures and has outlined the requirements to characterize NiSi- and PtSi-to-silicon contacts by the TLM method.

Acknowledgment

The authors would like to thank the Interuniversity Microelectronics Center (IMEC) P-line for processing the wafers and the IMEC Silicides, Litho, and Etch Groups for the special care and time they invested in the process development. The authors would also like to thank M. Kaiser of Philips Research Eindhoven for the TEM work.

References

[1] D. K. Schroeder, *Semiconductor Material and Device Characterization*, 3rd ed. New York: Wiley-Interscience, 2006.

[2] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era*, vol. 2. Sunset Beach, NC: Lattice Press, 1986.

[3] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 1981, pp. 304–307.

[4] M. J. H. van Dal, D. Jawarani, J. G. M. van Berkum, M. Kaiser, J. A. Kittl, C. Vrancken, M. de Potter, A. Lauwers, and K. Maex, "The relation between phase transformation and onset of thermal degradation in nanoscale $CoSi_2$-polycrystalline silicon structures," *J. Appl. Phys.*, vol. 96, no. 12, pp. 7568–7573, Dec. 2004.

[5] *The International Technology Roadmap for Semiconductors*, 2006. [Online]. Available: http://www.itrs.net/Links/2006Update

[6] A. Lauwers, A. Steegen, M. de Potter, R. Lindsay, A. Satta, H. Bender, and K. Maex, "Materials aspects, electrical performance, and scalability of Ni silicide towards sub-0.13 μm technologies," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 19, no. 6, pp. 2026–2037, Nov./Dec. 2001.

[7] H. Iwai, T. Ohguro, and S. Ohmi, "NiSi salicide technology for scaled CMOS," *Microelectron. Eng.*, vol. 60, no. 1, pp. 157–169, Jan. 2002.

[8] A. Lauwers, J. A. Kittl, M. J. H. van Dal, O. Chamirian, M. A. Pawlak, M. de Potter, R. Lindsay, T. Rayrnakers, X. Pages, B. Mebarki, T. Mandrekar, and K. Maex, "Ni based silicides for 45 nm CMOS and beyond," *Mater. Sci. Eng. B, Solid-State Mater. Adv. Technol.*, vol. 114/115, pp. 29–41, Dec. 2004.

[9] M. C. Poon, M. Chan, W. Q. Zhang, F. Deng, and S. S. Lau, "Stability of NiSi in boron-doped polysilicon lines," *Microelectron. Reliab.*, vol. 38, no. 9, pp. 1499–1502, Sep. 1998.

[10] D. Z. Chi, D. Mangelinck, A. S. Zuruzi, A. S. W. Wong, and S. K. Lahiri, "Nickel silicide as a contact material for submicron CMOS devices," *J. Electron. Mater.*, vol. 30, no. 12, pp. 1483–1488, Dec. 2001.

[11] A. Lauwers, M. de Potter, O. Chamirian, R. Lindsay, C. Demeurisse, C. Vrancken, and K. Maex, "Silicides for the 100-nm node and beyond: Co-silicide, Co(Ni)-silicide and Ni-silicide," *Microelectron. Eng.*, vol. 64, no. 1–4, pp. 131–142, Oct. 2002.

[12] S. J. Proctor and L. W. Linholm, "A direct measurement of interfacial contact resistance," *IEEE Electron Device Lett.*, vol. EDL-3, no. 10, pp. 294–296, Oct. 1982.

[13] T. A. Schreyer and K. C. Saraswat, "A two-dimensional analytical model of the cross-bridge Kelvin resistor," *IEEE Electron Device Lett.*, vol. EDL-7, no. 12, pp. 661–663, Dec. 1986.

[14] G. K. Reeves, "Specific contact resistance using a circular transmission-line model," *Solid State Electron.*, vol. 23, no. 5, pp. 487–490, May 1980.

[15] S. S. Cohen, "Contact resistance and methods for its determination," *Thin Solid Films*, vol. 104, no. 3/4, pp. 361–379, Jun. 1983.

[16] D. B. Scott, R. A. Chapman, C. C. Wei, S. S. Mahantshetti, R. A. Haken, and T. C. Holloway, "Titanium disilicide contact resistivity and its impact on 1-μm CMOS circuit performance," *IEEE Trans. Electron Devices*, vol. ED-34, no. 3, pp. 562–574, Mar. 1987.

[17] E. H. Rhoderick and R. H. Williams, *Metal–Semiconductor Contacts (Electrical & Electronic Engineering Monographs)*, 2nd ed. Oxford, U.K.: Oxford Univ. Press, 1988.

[18] N. Stavitski, M. J. H. van Dal, R. A. M. Wolters, A. Y. Kovalgin, and J. Schmitz, "Specific contact resistance measurements of metal–semiconductor junctions," in *Proc. IEEE ICMTS*, Austin, TX, 2006, pp. 13–17.

[19] B. Davari, "Shallow junctions, silicide requirements and process technologies for sub 0.5 μm CMOS," *Microelectron. Eng.*, vol. 19, no. 1–4, pp. 649–656, Sep. 1992.

Natalie Stavitski (S'07) received the B.Sc. degree in chemistry from the Hebrew University of Jerusalem, Jerusalem, Israel, in 2000 and the M.Sc. degree in materials chemistry from the Weizmann Institute of Science, Rehovot, Israel, in 2003. She is currently working toward the Ph.D. degree at the University of Twente, Enschede, The Netherlands.

From 2002 to 2005, she was a member of Engineering Staff of Intel Corporation, Israel, where she worked in the area of photolithography processes. Her current research is focused on the conduction mechanism in metal–semiconductor junctions and the development of dedicated test structures for the characterization.

Mark J. H. van Dal received the M.S. degree in chemical engineering and the Ph.D. degree dealing with solid-state diffusion and the Kirkendall effect, in 2001 from Eindhoven University of Technology, Eindhoven, The Netherlands.

In 2002, he was with Philips Research, Leuven, Belgium, where he was a member of the Front-End CMOS Technology Team. He actively participated in the research on silicides and, in 2004, on metal gate integration for advanced CMOS technologies. He is currently with NXP/Taiwan Semiconductor Manufacturing Company Research Center, Leuven, where he is responsible for FinFET integration. He is the author or a coauthor of over 25 journal papers. He is the holder of several patents.

Anne Lauwers received the M.S. degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1990 and 1995, respectively.

Since 1995, she has been with the Interuniversity Microelectronics Center, Leuven, where she is active in the research and development of silicides for advanced CMOS technologies. She is the author or a coauthor of more than 100 publications.

Christa Vrancken received the Bachelor degree in biotechnology from Group T, Leuven, Belgium.

Since 1989, she has been with the Interuniversity Microelectronics Center, Leuven, where she was a Process Assistant in the Lithography Group (1989–1998) and the Silicide Group (1998–2004). She is currently a Process Assistant for SiGe and SiC S/D technology.

Alexey Y. Kovalgin received the M.Sc. degree in physics from St. Petersburg State University, St. Petersburg, Russia, in 1988 and the Ph.D. degree in electronic materials technology from the St. Petersburg State Polytechnical University, St. Petersburg, in 1995.

In 1997, he was with the University of Twente, Enschede, The Netherlands, as a Postdoctoral Researcher. Since 2001, he has been an Assistant Professor with the MESA+ Institute for Nanotechnology, Chair of Semiconductor Components, University of Twente, where he is involved in thin-film-deposition technologies (CVD, ALD, plasma processing, modeling, thin-film characterization), design, and realization and characterization of novel silicon devices. He contributed to over 90 reviewed international journals and conference papers.

Rob A. M. Wolters received the M.Sc. degree in inorganic chemistry from the University of Twente, Enschede, The Netherlands, in 1974 and the Ph.D. degree based on the work on uranium carbonitrides from the Reactor Centrum Nederland, Petten, The Netherlands, in 1978.

He has been with Philips Research (currently at NXP Research), Eindhoven, The Netherlands, where he covers a large number of subjects related to the processing of Si integrated circuits. He has been involved in the introduction of chlorine-based plasma etching processes for gates and interconnects. He has vast knowledge of the application of silicides, barrier materials, and metals in the Si technology area. Since 2004, he has been a part-time Professor with MESA+ Institute for Nanotechnology, Chair of Semiconductor Components, University of Twente.