Software Defined Radio Receivers exploiting Noise Cancelling: A Tutorial Review

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Abstract: Traditional radio receivers were dedicated to a single frequency band, whereas Software Defined Radios target a flexibly programmable frequency, while maintaining high dynamic range. The Noise Cancelling circuit technique has proven useful to achieve this target, as it breaks the traditional trade-off between low noise and broadband impedance matching. Different variants exist, with noise cancellation in the voltage or current domain, either at RF or after frequency translation to baseband. This article reviews the development of the noise cancelling technique and its role in recent software defined radio receiver architectures.

Introduction

Radio is often still associated with broadcast radio, but radio frequency (RF) communication is now predominantly used for other wireless communication applications. Especially the enormous growth in ownership of mobile devices like smartphones, laptops and tablets has led to huge wireless data streams, especially for internet access and more recently Cloud services. It is well know that this wireless revolution has been enabled by Moore's Law which provides ever more computing power on cost effective CMOS chips. What is perhaps less known, is that changes in radio architecture have also fuelled the wireless consumer revolution, by enabling fully integrated CMOS radio transceivers. To understand how fundamental this change in architecture is, it is illustrative to compare a traditional super-heterodyne radio receiver, invented almost a century ago, with a modern CMOS radio receiver, as shown in Figure 1.

The first striking difference between the two is that radio waves are no longer converted to analog sound, but to digital bits. However, not only the final output is digital, but also a lot of the radio signal processing that realizes channel selectivity and demodulation. Actually, it has been proposed to convert the antenna signal directly to digital to realize a true "Software Radio" [1]. This is attractive as it allows for ultimate flexibility and fits to Moore's law that makes ever more digital processing possible. Unfortunately, for most applications this puts unrealistic demands on the analog to digital converter. As RF signals can easily vary from well below $1\mu V_{rms}$ to almost 1V, around 20bits resolution would be required at sample rates well above 12GS/s to cover the frequency bands up to 6GHz. Such A/D converters are still far from feasible and if feasible would require hundreds of Watts [1]. Hence a modern CMOS radio receiver down-converters the RF signal to baseband, where A/D conversion is feasible and power efficient. As antenna signals can be very weak, amplification with very low noise is clearly wanted before A/D conversion. Furthermore, anti-alias filtering is crucial to avoid strong out-of-band signals to alias on top of the wanted signal and overwhelm it. *It is this low noise amplification combined with frequency selectivity* that is the core functionality of a radio receiver. In the super-heterodyne receiver this selectivity is realized by extensive use of LC-tanks or other resonators. An LC tank with high quality factor Q operating close to its resonance frequency behaves like a very selective band-pass filter. High Q LC-tanks also have low loss and hardly add noise. This has made the super-heterodyne receiver the architecture of choice for most of the last century, and it still is used in many applications. However, if low cost is crucial, full integration on a CMOS chip is wanted, and other

solutions are needed for several reasons. One reason is the poor quality factor of CMOS coils in the low GHz range, due to the high metal resistance of thin metal layers in nanometer CMOS technologies. Moreover, a single coil may take as much chip area as a complete microprocessor core. Hence, inductor-less receivers are highly wanted and alternatives for the super-heterodyne radio receivers have been pursued during the last decades.

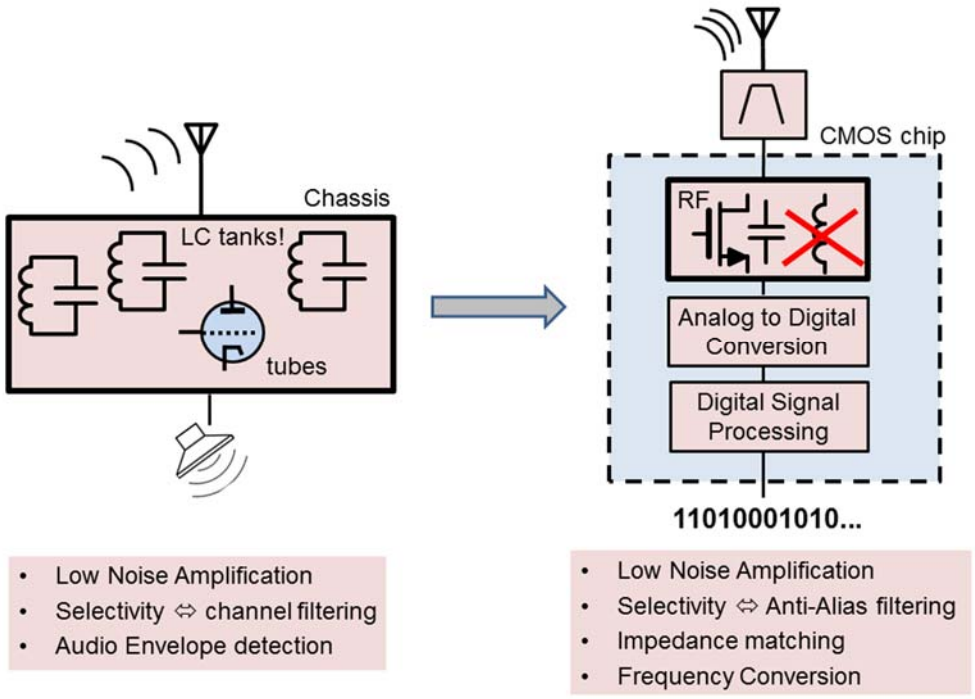

Figure 1: Historical Development of Radio Frequency (RF) receivers during the last century

Fully integrated CMOS radio architectures now usually rely on a homodyne architecture which directly down-converts the RF-signal to baseband, around 0 Hz ("zero-IF" architecture). At baseband, simple low-pass filtering can be used for anti-alias filtering and high dynamic range A/D conversion is feasible at 10-100 mW power level. However, a very challenging RF frontend design problem remains: *how to realize low noise amplification and frequency conversion with high dynamic range, to cope with strong interferers ("blockers"), without using on-chip inductors*. In most mobile phones, external RF band-filters are used, realized exploiting Surface Acoustic Waves ("SAW filters"). However, attempts are made to realize SAW-less receivers, to reduce both the cost and size on external components. Moreover, for dynamic spectrum access with cognitive or software define radios, more flexibility is wanted. Fixed frequency filters limit the flexibility and hence new radio receiver architectures are being explored. These have been published under different names like multi-band receiver, reconfigurable receiver, SAW-less receiver, wideband receiver, software defined receiver and cognitive radio receiver. What they have in common is increased flexibility in receive frequency realized without relying on inductors. This article will review changes in radio receiver architecture, focusing on architectures that exploit noise cancellation, a technique allowing for broadband impedance matching without paying a noise penalty. This noise cancelling technique was originally discovered [2] and improved [3, 4] in the IC Design group at the University of Twente and developed further by many other research groups and companies. Especially after the publication in [4], this technique has received many citations and is now included in RF textbooks [5]. A recent publication

[6] clearly demonstrates its impact on integration in CMOS: only 0.42 mm^2 chip area is needed in 40nm CMOS to realize 7 inductor-less noise cancelling receivers that support triple-mode and six-band TDD cellular bands in a modern phone. In the next section we will first briefly review classical inductor-less broadband radio receiver techniques and then introduce the noise cancellation technique and some of its later variants like frequency translated noise cancellation.

Classical Broadband Receiver Techniques

If we decide not to use inductors and essentially realize a wideband receiver, the classical solution is a broadband Low Noise Amplifier (LNA) followed by a mixer for frequency conversion, driven by a Local Oscillator (LO). Passive hard switching mixers (e.g. diode mixers or MOSFET switches) are preferred for their linearity and high dynamic range, but introduce conversion loss and high noise figure due to losses and noise folding. A preceding LNA hence realizes low noise pre-amplification, while also isolating the mixer from the antenna to suppress LO-radiation. Moreover, it realizes impedance matching to terminate an (external) filter or transmission line from the antenna with a "matching resistance". Usually this is 50ohm, compatibility with most antennas, SAW-filters and RF measurement equipment.

To understand the broadband LNA design problem better, it is illustrative to have a look at Figure 2, which shows the main classical broadband LNA solutions realizing impedance matching and low noise amplification. The circuit in Figure 2a is known as "Common Source" stage, as the source terminal of MOSFET (arrow side) is grounded and shared by the input and output port. The MOSFET realizes V-I conversion from gate-voltage to drain-current with transconductance g_m, while resistor R_L realizes I-V conversion, so that the voltage gain is $-g_mR_L$. To realize impedance matching to 50ohm, a resistor R_i of 50Ω is added. As this resistance generates the same amount of thermal noise as the noise available from a 50ohm antenna or passive filter, noise power is doubled and hence Signal to Noise ratio is degraded by 3dB, so that the theoretical minimum noise figure is 3dB. The MOSFET and R_L exacerbate noise, so that typically a Noise Figure of 5-6dB results. The popular "Common Gate" circuit in Figure 2b is slightly better, as it needs less noisy components: it reuses the same MOSFET not only to realize V-I conversion (g_m) but also input impedance matching ($=1/g_m$). Now we get a non-inverting voltage gain g_mR_L, at somewhat lower noise figure, e.g. about 4dB.

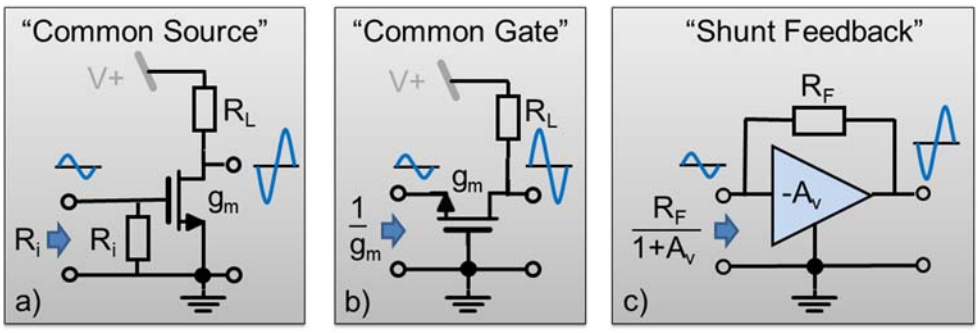

Figure 2: Classical broadband amplifier stages with impedance matching: (a) Common Source with resistor; (b) Common Gate; (c) Shunt feedback stage which can achieve a noise figure <3dB.

These noise figure values compare poorly to the 1-2dB achieved with inductor based LNAs used in early generations of mobile phones. For inductorless receivers to compete with such noise performance, we would like to achieve a noise figure well below 3dB. Although 1 dB might not seem

much at first sight, compensating for 1dB extra noise figure will require about 26% more transmit power, which is a lot if the transmit power is already in the order of 1-2W (GSM).

To achieve <3dB Noise Figure, a classical solution is the "shunt-feedback" stage (Figure 2c). The input impedance is lowered by negative feedback, so that, seen at the input, shunt resistance R_F gets divided by a factor $(1+A_v)$. As R_F can now be a resistance much higher than 50ohm with much lower current noise than 50ohm, <3dB Noise Figure can now be achieved. However, at GHz frequencies it is difficult to realize enough gain and with low loop gain negative feedback loses many of its benefits. More problematically, multi-stage amplifiers have stability issues, which are exacerbated by the fact that the antenna impedance may vary significantly over frequency. Noise cancelling is an open loop amplifier technique and hence doesn't have such stability risks.

Noise Cancellation

Figure 3 shows one of the simplest Noise Cancelling LNA implementations, consisting of a parallel operating Common Gate and Common Source stage with equal gains. This doubles the overall gain and produces a balanced differential output from a single-ended (non-balanced) input. The signal coming from an antenna or other signal source is modelled as a voltage source with series resistance R_s, usually 50ohm. Bias voltages and a bias current block ensure transistors operate in the right operating region to realize a transconductance g_m (not further discussed here for simplicity). The Common Gate stage realizes impedance matching and non-inverting voltage gain. The Common Source amplifier senses the input voltage and produces an inverting amplification with the same gain. The noise cancellation property is illustrated in Figure 3b. The noise current of the Common Gate transistor i_n flows through both R_L and R_s, producing two *fully correlated opposite polarity* voltages on its input (R_s) and output (R_L). The Common source stage senses the input voltage and amplifies it with inverting gain. Overall two fully correlated common mode noise voltages result, which cancel at the differential output.

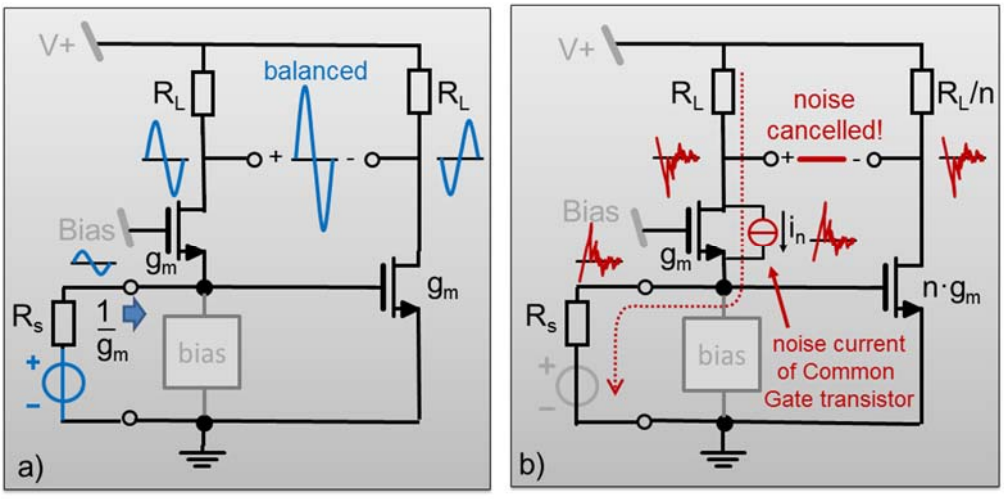

Figure 3: Noise Cancelling Topology with parallel Common Gate and Common Source amplifiers: (a) signals (in blue) are amplified to a balanced differential output; (b) Noise (in red) of the impedance matching Common-Gate transistor produces two correlated noise contributions that cancel at the differential output.

Note that the signal source in Figure 3a produces two anti-phase output signals that add to each other if the output is sensed differentially by the next circuit. In this way, a single ended input to a filter or

antenna is supported, while a differential output signal results, i.e. on chip single-to-differential conversion of "balancing" is realized ("BALUN" functionality). Hence, no external BALUN is needed, which would otherwise introduce 1-2dB signal loss, directly adding to the noise figure. Moreover, the distortion of the Common Gate matching transistor, which can be modelled as a parallel current source, is also cancelled just as the noise. Hence simultaneous balancing, noise cancelling and distortion cancellation is achieved. In essence this technique *decouples* noise and input impedance matching so that broadband resistive impedance matching is realized, *without* paying a price in term of noise figure. Note however, that only the noise and distortion of the Common Gate matching device is cancelled. It is critical that the common source stage is low noise and very linear, as it will now dominate noise and distortion [7]. Fortunately, the transconductance of the Common Source transistor can be increased without affecting the matching resistance. Hence, the Common Source stage is usually scaled up in transconductance to $n*g_m$, while its load resistance is lowered to R_L/n to maintain equal gain for the two parallel stages [7].

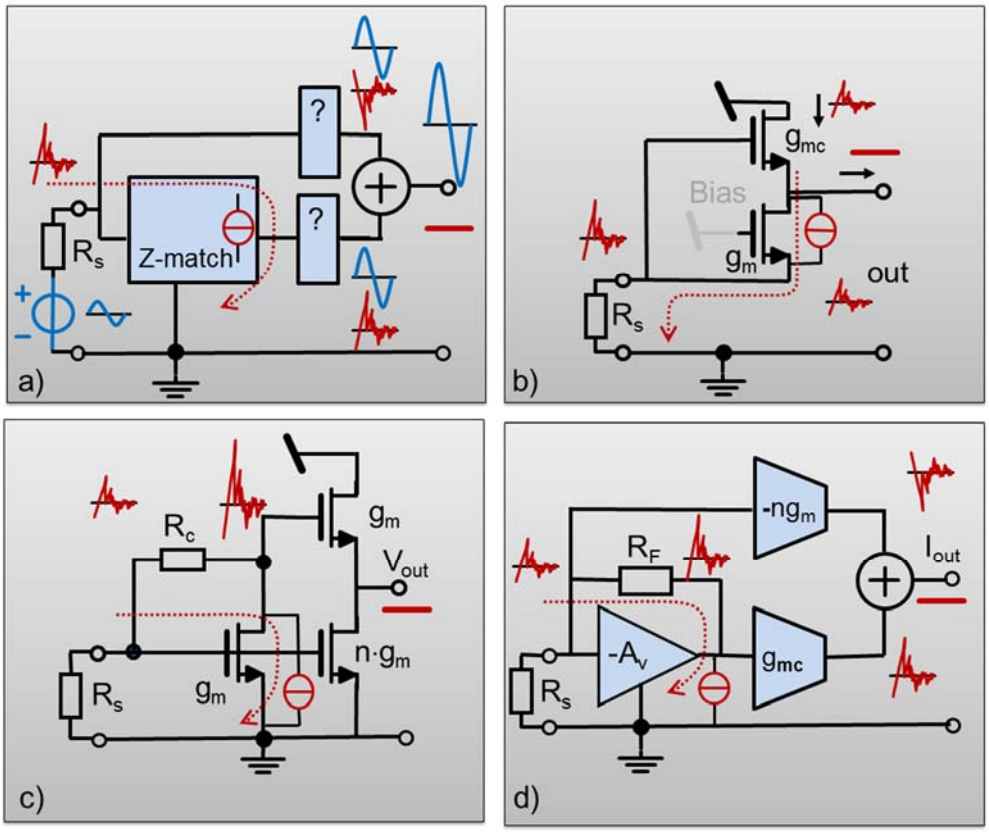

Figure 4: Different Noise Cancelling Circuit Topologies: (a) General concept (b) Original topology discovered by systematic circuit graph generation [2, 3]; (c) First Noise Cancelling LNA with noise figure <3dB [4]; (d) Current-output noise cancelling [6].

Several variants of the noise cancellation receivers have been proposed over time. Figure 4 shows a few, along with the general concept in Figure 4a. In all cases there is a block "Z-match" that matches the input impedance to R_s of the antenna or input signal source. The noise of this matching device generates a noise voltage across source resistance R_s, which is sensed together with the input signal by the upper signal paths to the output. The lower signal path to the output senses both the noise and signal at another terminal of the matching device. Note that in all cases: 1) there are two fully correlated noise contributions, both originating from the same matching device, that cancel at the

output; 2) the wanted signal is injected in another way than the noise of the matching device, so that signal contributions add, while noise cancels. As indicated by the blocks with question marks, there are many different ways to implement the signals path to the output. This is not only because different circuit implementations exist, but also because the output can be in the voltage or current domain, at the same frequency or at another frequency (see the next section on frequency translated noise cancellation). A few implementations will be discussed briefly below. Bias network details are largely left out for simplicity.

Figure 4b shows a simple 2-transistor implementation of the original noise cancellation circuit topology [2]. It was discovered by systematically generating all possible circuit topologies exploiting two transconductance devices using graph theory [2, 3]. The lower transistor acts as Common Gate device for input impedance matching, while the upper transistor senses and cancels the noise via transconductance g_{mc}. Although this circuit has some attractive properties like a gain independent noise figure and high linearity at low power consumption [3], it does NOT have a noise figure lower than 3dB. This is because the upper transistor needs to have $g_{mc}=g_m$ to cancel the noise of the matching device. Unfortunately, for this "equal g_m" condition, the upper device adds about the same noise than a Common Gate stage would without noise cancelling. Hence an extra degree of freedom is wanted to allow for scaling up the auxiliary noise cancelling path.

The circuit in Figure 4c offers this extra degree of freedom, and was the first published noise cancellation topology published at ISSCC 2002, achieving a Noise Figure below 3dB [4]. Actually broadband noise figure <2dB was achieved from 250MHz to 1GHz, competitive to narrowband LC-based receivers. Here a common source amplifier with unity current feedback via resistor R_c realizes an input impedance of $1/g_m=R_s$, while also realizing a voltage gain $1-g_mR_c$. Note that this is direct local feedback across one transconductor g_m without stability risks, in contrast to the shunt feedback over a voltage amplifier in Figure 2c. The transistor with transconductance $n*g_m$ senses the noise at the input and cancels the noise coming via the upper signal path if $R_c=(n-1)R_s$ [4]. Due to the voltage gain in the matching stage and due to the scaled up sensing transistor, noise figure can now be lowered to well below 3dB, albeit at the cost of extra power consumption (n times g_m also scales the bias current by n times). A worry may be what happens with noise figure if the antenna impedance varies and the cancellation is no longer perfect. It can be shown that $\pm$20% variation is antenna impedance raises NF from 1.8dB to 2dB [4].

As a last example consider the circuit in Figure 4c, which is used in the chip containing 7 noise cancelling LNAs [6]. Again an impedance matching stage is used with two paths to the output, but now the addition is done in the current domain. Overall we realize now low noise V-I conversion, i.e. a Low Noise Transconductance Amplifier. This can have significant benefits for linearity and blocker handling, especially when this is combined with high linearity current mixers and frequency translated filtering as will be discussed next.

Frequency Translated Noise Cancellation

Although the noise cancelling LNAs with voltage gain have many attractive properties, there are also challenges, especially if we need to handle strong blockers up to 0dBm (1mW) power, as commonly is wanted for out-of-band blockers for GSM and 2G-3G-4G standards. Note that 1mW in 50ohm corresponds to a peak-to-peak voltage of about 600mV. This is significant voltage swing for a CMOS chip operating at a standard 1Volt voltage supply for device reliability reasons. Even a very low voltage

amplification of 2x (6dB) would already clip the output of a voltage amplifier to the 1 Volt supply. Another problem occurs when we aim to realize high bandwidth in the presence of significant capacitive loading at the output. It is then critical to use low resistance levels as bandwidth is inversely proportional to the RC time-constant. One option is to use a low-Q inductor in series with R_L to enhance the bandwidth by "inductive broadbanding" or "inductive peaking" [8, 9], but this takes significant chip area. A more attractive alternative way is to *avoid voltage gain at RF*, and move it to baseband. This is the purpose of the BLIXER (Balun-LNA-mIXER) circuit shown in Figure 5a [10]. Here a current domain mixer is inserted between the transistor core of Figure 3 and the Resistive load. Now at RF only V-I conversion takes place, followed by a frequency down-conversion mixer and then I-V conversion in baseband. The noise cancelling still occurs, but now after frequency translation. Later this has been named frequency translated noise cancelling in another implementation [11]. As the gain is now realized in baseband instead of RF, load capacitance that would otherwise limit the (RF-)bandwidth of the I-V conversion, is no longer a problem. Even stronger, we usually *want* a large capacitance at the output, to suppress out-of-band blockers. As filtering reduces the amplitude of blockers, we can then allow for much more gain without clipping to the low supply voltage. If we use down-conversion to 0 ("zero-IF"), we can use simple low-pass filtering for anti-alias filtering and relax ADC dynamic range and sampling rate requirements. If we prefer to realize channel selectivity before the ADC this is also feasible by adding extra OPAMP-RC filter stages. Note that this is not possible at RF, as the required Q for a band-pass filter with center frequency f_{center} and -3dB bandwidth BW is f_{center}/BW. Even for a wideband radio standard like WCDMA with 20MHz bandwidth around 2GHz center frequency, a Q of 100 would be required, which in infeasible (inductor Q values are typically <15 for on chip inductors at a few GHz).

Figure 5a shows the first published frequency translational noise cancelling receiver [10], which can easily be extended to an I/Q zero-IF receiver (not shown for simplicity), exploiting two mixers and LO-signals with 25% duty cycle. In this BLIXER topology, the mixers were realized as active mixers, like in the well-known Gilbert Mixer [5]. The mixer core is realized as a differential pair driven at the gate by steep square-wave signals at the LO-frequency f_{LO}. Note that such square-wave signals are nicely compatible with digital generation, allowing for flexibly programmable digital frequency synthesizers compatible with software defined radio. The hard-switching of the differential pair activates one of the two transistors that passes the current applied to the input of the mixer to one of the two output terminals. Note that, although the transistor are hard switched, they ideally act not as low-ohmic transparent switches, but rather as a Common Gate stage in Figure 2a. Such a Common Gate stage has a low input impedance of $1/g_m$, but a high output impedance. Hence it acts as a so called "cascode transistor", improving the output impedance and hence the voltage gain of the active mixer, while also improving reverse isolation (output signal changes don't affect the input). Due to the low input impedance, the signal swing at the RF side of the mixer is low and the RF bandwidth can be extended to beyond 10GHz in 65nm, without using inductors [10].

We have now relaxed a bandwidth problem, but perhaps even more importantly, we have improved interference robustness of a receiver by realizing a Low Noise Transconductance Amplification ("LNTA") instead of the traditional voltage amplifying Low Noise Amplifier (LNA). A key reason why moving to the current domain helps, is the limited voltage swing that is available on a CMOS chip with a standard supply voltage of about 1Volt. As there is no hard limit on current, we can cope with strong interferers in the current domain. The key to interference robustness is threefold [12]: 1) a *high*

linearity LNTA followed by 2) *high linearity current mixing* and 3) *simultaneous channel filtering and I-V conversion in baseband*.

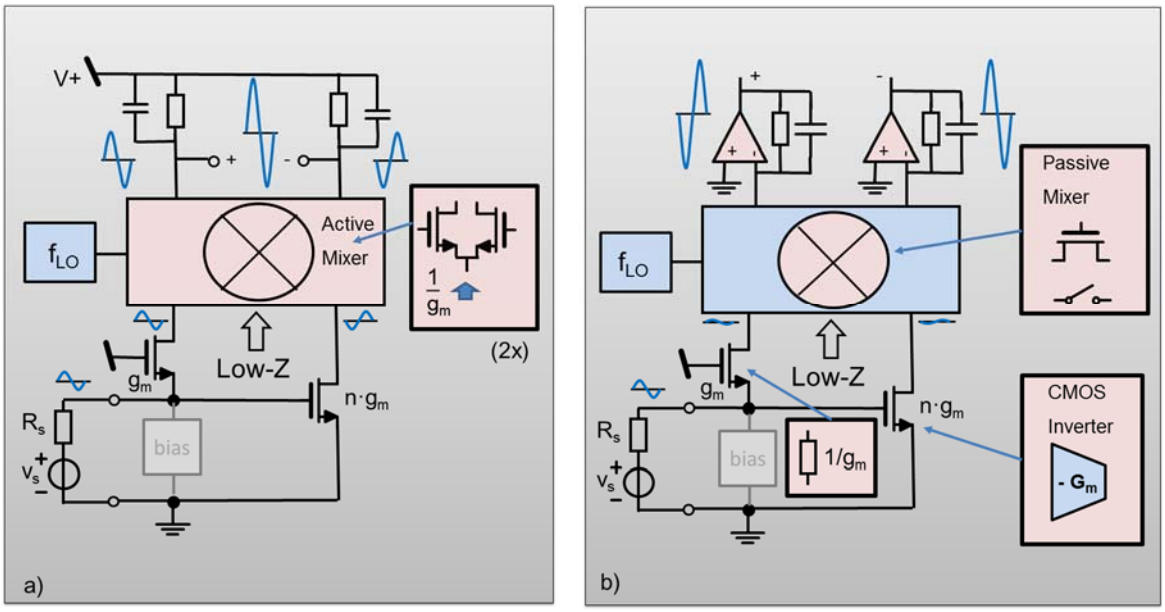

Figure 5: Frequency Translational Noise Cancellation concept: at RF only V-I conversion occurs followed by current-mixing, while I-V conversion is combined with low-pass baseband channel filtering[10]. (b) Interference robust implementation exploiting highly linear passive mixers and OPAMP-RC amplifiers [11].

Improving Interference Robustness

As shown in [11], the Frequency Translated Noise Cancellation concept can be taken a few steps further in terms of interference robustness by the steps illustrated in Figure 5b, resulting in the circuit of Figure 6a. Passive MOSFET mixers exploiting MOSFETs as switches are known for their excellent linearity and low frequency 1/f noise especially when combined with an LNTA [11-13], and are hence preferred over active mixers for zero-IF receivers. By using OPAMP-RC transimpedance amplifiers at baseband, a virtual ground node is created at the OPAMP input, which is a convenient low ohmic current-summing point. As a result, the common gate stage can now be replaced by a simple 50ohm resistor that combines impedance matching with very high linearity V-I conversion of the RF-voltage to current. To realize noise cancelling of the noise of the resistor, an auxiliary noise sensing and cancelling path is needed. The linearity of this V-I converter is now crucial for the overall achievable linearity. CMOS inverters can be used as linear V-I converters [14]. They have favorable class-AB large signal behavior which avoids hard-clipping and renders very high Signal to Noise Ratio Normalized to Power Consumption, not far from the theoretical maximum of 165dB [15]. When designed carefully for high linearity, exploiting “derivative superposition” high IIP3 values above 10dBm are possible [11, 12]. However, this high linearity is sensitive to Process, Voltage and Temperature variations, and calibration is likely needed to guarantee such high linearity over different operating conditions.

To illustrate the interference robustness further Figure 6b shows the frequency spectrum at 4 nodes of the main receiver path. With voltage gain the strong interferer (red) would clip the voltage to the supplies and/or cause strong intermodulation and cross-modulation distortion that would corrupt the weak wanted signal (blue). The resistor and switch handle the very strong signal with very high

linearity, while the OPAMPs in baseband can also be very linear and can realize a very low ohmic virtual ground node at its input. For higher baseband frequencies, where the achievable gain of the OPAMP drops, the virtual ground node is made low ohmic by adding a capacitor C_i to ground (Figure 6b). Very effective filtering can now be realized by the RC network across the OPAMP, which strongly attenuates to interferer and improves Signal to Interference ratio.

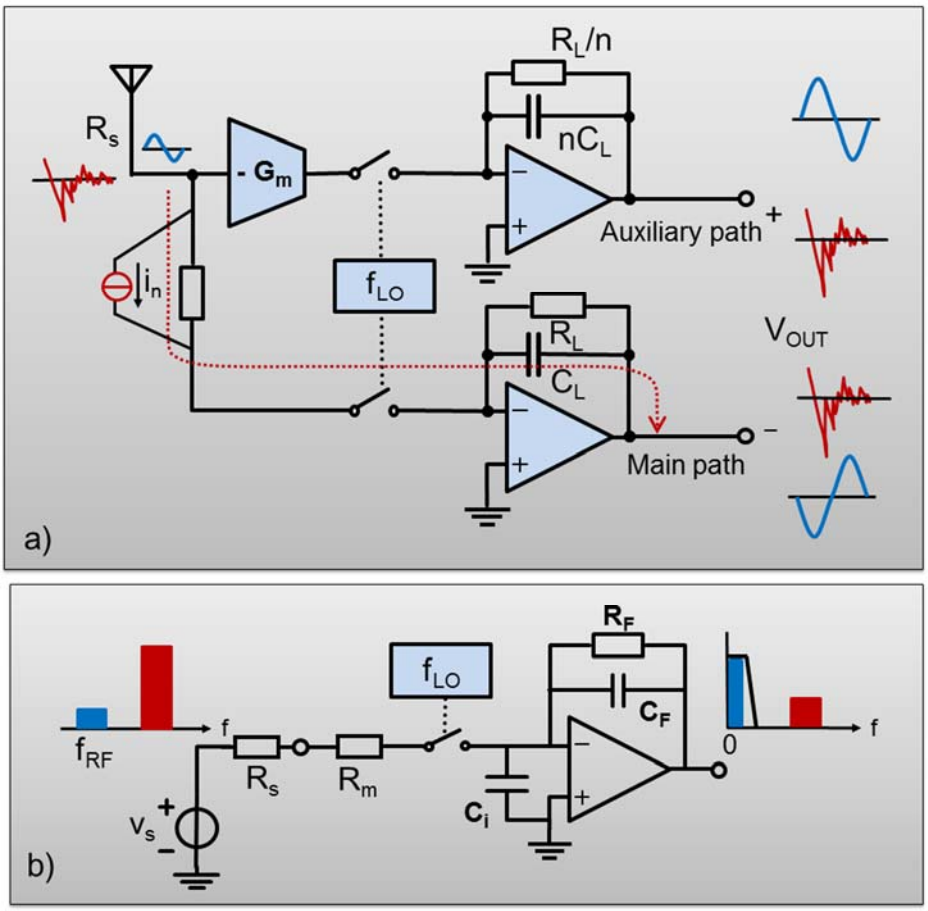

Figure 6: Interference Robust Frequency Translational Noise Cancellation receiver: a) Complete Circuit with main and auxiliary noise cancelling path; (b) Signal spectrum along the main receiver chain

Conclusion

This article has reviewed the origin and development of the noise cancelling technique and its impact on realizing fully integrated software defined radio receivers to realize low noise figure and high interference robustness. The noise cancellation technique essentially allows for wideband impedance matching without a noise penalty, as the noise of the matching device is cancelled. This allows for noise figures well below 3dB without inductors. Simultaneous balancing, noise cancellation and distortion cancellation is also possible. Different implementations exist with cancelling in the voltage or current domain, either at the RF frequency or after frequency translation to baseband. When the cancellation is implemented in the current domain very high signal swings can be handled without voltage clipping to the low standard voltage supply of nanometer CMOS processes. When combined with a highly linear passive current mixer, interference robustness can be improved further by moving the I-V conversion to baseband, where it can be combined with channel filtering. Overall, this enables compact software defined multi-band terminals to be realized at low cost.

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