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CHARGE LOSS EXPERIMENTS IN SURFACE CHANNEL CCD's EXPLAINED BY THE McWHORTER INTERFACE STATES MODEL

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On the basis of the McWhorter interface states model the CCD charge loss is derived as a function of bias charge, signal charge and channel width. As opposed to existing models, the charge loss is now attributed to interface states in the entire gate area, even for high bias charge levels. Experimental confirmation of the novel model is presented.

1. INTRODUCTION

If a step signal is applied to a surface channel CCD, the leading pulses at the output are attenuated. The sum of the charge deficits in the leading pulses, the so-called charge loss[1], is a function of the step signal and of the bias charge and is caused by incomplete charge transfer due to interface states.

Recently we showed that the small-signal charge transfer inefficiency (SCTI) can be fully understood[2] if use is made of the McWhorter interface states or oxide trap model[3]. In this model a spectrum of capture cross sections is associated with interface states at each energy level in the band gap. This feature is also responsible for the succes of the McWhorter interface states model in relation to 1/f noise in MOST's[3]. Here it will be shown, that the same interface states model can be applied to the charge loss in CCD's.

The organization of this paper is as follows. The occupancy of interface states in a two-phase CCD is discussed first, and an expression is derived for the incremental remaining charge, which is the charge loss per storage gate. Then experimental data are presented, followed by a discussion of the obtained results.

We will confine ourselves to n-channel CCD's, but an extension of the model to p-channel devices is straightforward.

2. THEORY OF THE INCREMENTAL REMAINING CHARGE

In the McWhorter interface states model[3] a distribution of states in a thin SiO_2 layer on top of the Si is assumed. A tunneling mechanism provides the interaction of interface states with free electrons in the Si. The effect of a spatial distribution of interface states on their dynamical behaviour is described by a position dependent capture cross section $\sigma_n(x)$, which decreases with the depth x of the state in the oxide[4]:

$$\sigma_n(x) = \sigma_n \, e^{-x/x_o} \qquad (1)$$

with x_o the penetration depth of an electron in the SiO_2 and σ_n the capture cross section at the interface.

Substitution of (1) in the Shockley-Read-Hall rate equations results in a position dependent differential equation for the interface states occupation function g(E,t,x):

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$$\frac{dg(E,t,x)}{dt} = \sigma_n v_{th} e^{-x/x_o} [1 - g(E,t,x)] n_s - \sigma_n v_{th} e^{-x/x_o} N_c e^{-E/kT} g(E,t,x) \quad (2)$$

where v_{th}, N_c and kT have their usual meaning, n_s is the volume concentration of electrons at the Si/SiO_2 interface and E the energy, measured downwards with respect to E_c. g(E,t,x) can be conceived as the probability that an interface state at energy E, position x and time t is occupied by an electron.

The steady-state solution of (2), achieved if n_s is kept infinitely long at the interface, is obtained from dg(E,t,x)/dt = 0. It is a Fermi-Dirac distribution function, independent of the position x, with an associated quasi-Fermi level $E_Q(n_s)$:

$$E_Q(n_s) = kT \ln \frac{N_c}{n_s} \quad (3)$$

In the steady-state situation $E_Q(n_s)$ forms the boundary of the filled interface states.

Now consider a two-phase CCD operated with a clock frequency $f_c = 1/T_c$ and with constant charge packets $Q_b + Q_s$, corresponding to a volume charge carrier density n_s. Below a particular storage gate the carrier density n_s is present in the storage mode, during a time $T_c/2$, while in the remaining part of the clock period the mobile charge density is equal to zero.

The occupancy of interface states during a clock cycle is the result of two competing mechanisms. First, from solution of (2) it follows that in the storage mode a net capture of charges occurs, which forces the interface states occupancy to converge to the steady-state situation with a time constant $\tau_{eff}(E,x)$:

$$\tau_{eff}(E,x) = \left[\sigma_n v_{th} e^{-x/x_o} [n_s + N_c e^{-E/kT}]\right]^{-1} \quad (4)$$

Secondly, in the time interval that no mobile charge is present below the gate, net emission takes place, which tends to empty all interface states with an emission time constant:

$$\tau_{em}(E,x) = [\sigma_n v_{th} e^{-x/x_o} N_c e^{-E/kT}]^{-1} \quad (5)$$

Because in a two-phase CCD both these mechanisms are effective during half a clock period, the mechanism with the shortest time constant (the net capture), will finally dominate.

It follows that the occupation function at the end of the storage of one of an infinitely long string of charge packets $Q_b + Q_s$, is approximately equal to the steady-state occupation function. Consequently, the filled interface states obey:

$$E > E_Q(n_s) \quad \text{for all } x \quad (6)$$

A schematical representation of (6) is shown in fig. 1.

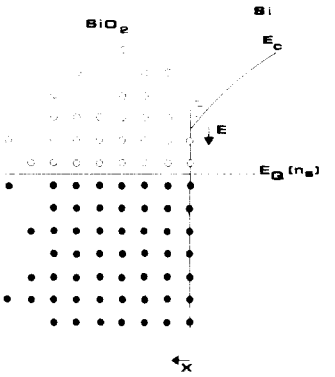

FIGURE 1
Interface states occupancy described by (6). Open and black dots indicate empty and filled interface states.

Upon transfer of $Q_b + Q_s$ to the adjacent storage gate, net emission starts and after the transfer has been enabled during a time t', all interface states with emission time constants

$\tau_{em}(E,x) < t'$ have been released their charge, while states with $\tau_{em}(E,x) > t'$ remain filled. The emission line $x_e(t',E)$[2,5], which connects interface states of equal emission time constants t', can be considered then as the boundary between filled and empty states. From (5) it follows that $x_e(t',E)$ is given by:

$$\frac{x}{x_o} + \frac{E}{kT} = \ln\left[\sigma_n v_{th} N_c t'\right]. \qquad (7)$$

Taking into account the interface states occupancy at the end of the storage mode, the filled interface states after the transfer of the charge packet during a time t' obey:

$$E > E_Q \quad \text{and}$$

$$\frac{x}{x_o} + \frac{E}{kT} > \ln\left[\sigma_n v_{th} N_c t'\right] \qquad (8)$$

which is depicted in fig. 2.

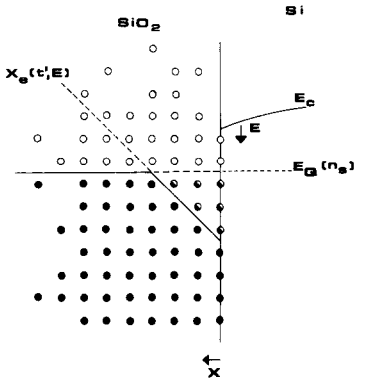

FIGURE 2
Interface states occupancy after transfer of $Q_b + Q_s$ is enabled during a time t'. Half filled dots denote interface states which emitted their charge in $[0,t']$.

The relations (6) and (8) describe the occupancy of McWhorter interface states in a CCD operated with a duty cycle 1/2. They can be derived more rigourously by solving (2) during an entire clock cycle, making use of the periodic nature of the CCD.

The quasi-Fermi level and the emission line will be used now to calculate the charge loss per storage gate after a step of the input signal.

Consider a large number of charge packets $Q_b + Q_s$, followed by m bias charge packets Q_b with volume charge density n_b. At the end of the storage of the last charge $Q_b + Q_s$ the occupancy is described by (6) while after transfer during a time interval $[0,t']$ it is governed by (8).

During the subsequent storage of the bias charge Q_b the occupancy of states with $E > E_Q(n_b)$ is updated, while for states above the quasi-Fermi level associated with Q_b, that is $E < E_Q(n_b)$, the emission process continues. After transfer of the $m^{\underline{th}}$ bias charge, the emission process for states with $E < E_Q(n_b)$ has been effective for a time $mT_c + t'$, and in this energy range the emission line $x_e(mT_c + t', E)$ describes the occupancy. For states with $E > E_Q(n_b)$ the emission has only been effective for a time t', and the emission line $x_e(t',E)$ is appropriate. It follows that after transfer of the $m^{\underline{th}}$ bias charge during a time t' the filled states obey:

$$E_Q(n_s) < E < E_Q(n_b) \quad \text{and}$$

$$\frac{x}{x_o} + \frac{E}{kT} > \ln\left[\sigma_n v_{th} N_c \left[mT_c + t'\right]\right]$$

or

$$E > E_Q(n_b) \quad \text{and}$$

$$\frac{x}{x_o} + \frac{E}{kT} > \ln\left[\sigma_n v_{th} N_c t'\right] \qquad (9)$$

The interface states occupancy described by (9) is depicted in fig. 3.

In case again a step signal $Q_b + Q_s$ is applied to the CCD, the occupancy as described in (8) is reached again and an amount of charge, corresponding to the dotted area in fig. 3 is lost. Assuming a density of interface states

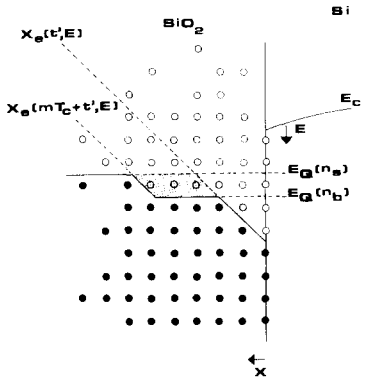

FIGURE 3
Interface states occupancy after transfer of the mth bias charge. For $E < E_Q(n_b)$ emission continued even in the storage mode. Interface states in the dotted area are refilled by a new string $Q_b + Q_s$.

D_{ox} [eV^{-1} cm^{-3}], uniformly distributed in energy and position and using the expressions for the quasi-Fermi level and emission line, this incremental remaining charge (IRC) can be calculated to be:

$$\Delta Q_R = -q\,kT\,A\,x_o\,D_{ox}\ln\left(1+\frac{Q_s}{Q_b}\right).\ln\frac{t'}{t'+mT_c} \quad (10)$$

with A the storage gate area and t' the transfer time. ΔQ_R is the incremental charge which remains captured in interface states below a single storage gate, in case after m bias charges, charge packets $Q_b + Q_s$ are transferred. Experimentally, ΔQ_R can be determined from charge loss measurements.

3. EXPERIMENTAL VERIFICATION

In fig. 4 the CCD response on a step signal $Q_b + Q_s$ alternated with m bias charge packets Q_b is depicted. The charge loss Δ, which is the total charge deficit in the leading pulses of the step signal[1], is equal to the incremental remaining charge below all individual gates in the entire CCD. Using a modified pseudo-one-phase clocking scheme[2], the time which is available for charge transfer from the DC-storage gate to the pulsed storage gate, the transfer time t', can be varied independently. Measuring Δ as a function of t', the observed

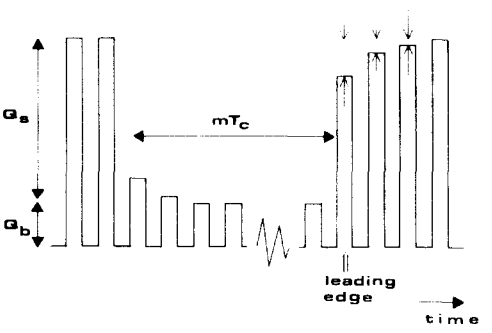

FIGURE 4
Representation of the CCD step response.

variation in Δ can be ascribed then to the incremental remaining charge associated with the DC-storage gates and ΔQ_R can be calculated.

The test devices used for the experiments were n-channel SCCD's with double level polysilicon gates, fabricated on <100> Si with $N_a = 8 \times 10^{14}$ cm^{-3}. Devices with channel widths W = 50 μm, 150 μm and 300 μm, but otherwise identical have been used.

In fig. 5, ΔQ_R data are presented as a function of Q_s, with Q_b as a parameter. In order to enable comparison with data from other devices, all parameters are expressed as surface charge carrier densities. The solid curves were calculated according to (10) with $x_o D_{ox} = 4.3 \times 10^9$ eV^{-1} cm^{-2}, which was obtained from independent SCTI measurements[2]. It is emphasized that no parameter matching has been used to obtain the theoretical curves. The figure shows that the predicted dependences on Q_s and Q_b fit very well with the experimental data.

It is a striking feature of (10) that the IRC per unit area, $\Delta Q_R/qA$ is independent of the channel width. This is confirmed by the experimental data in fig. 6, where $\Delta Q_R/qA$ is plotted as a function of the size of the step signal with the channel width as a parameter. Again the solid line is calculated according to (10) with $x_o D_{ox} = 4.3 \times 10^9$ eV^{-1} cm^{-2}, without matching of parameters.

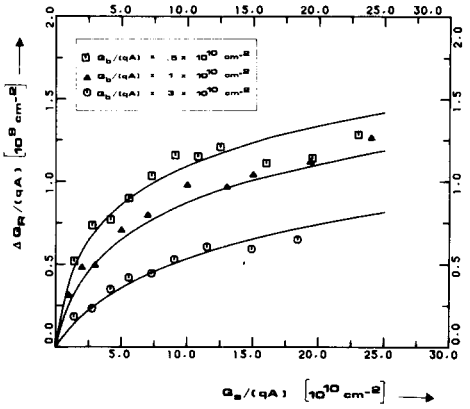

FIGURE 5
$\Delta Q_R/qA$ as a function of Q_S/qA with bias charge as parameter. $T_c = 10$ μs, $t' = 4$ μs and $m = 10$.

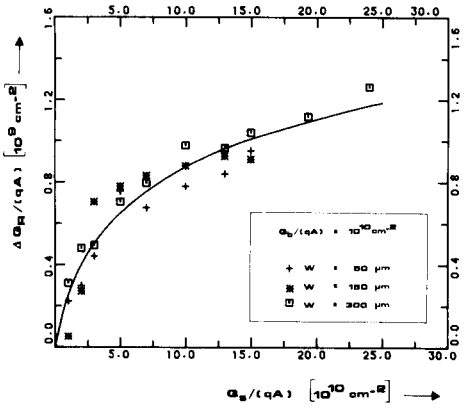

FIGURE 6
$\Delta Q_R/qA$ as a function of Q_S/qA with the channel width W as parameter T_c, t' and m as in fig. 5.

4. DISCUSSION

The existing theory concerning the charge loss[1] is based upon the so-called fixed loss and proportional loss, which describes the action of interface states in the central storage gate area and along the channel edges. The proportional loss is expected to be dominant for large bias charge Q_b[1], leading to a channel width independent charge loss. Expressed in charge carriers per unit area, this results in a charge loss which is inversely proportional to the channel width W. As the data in fig. 6 do not reveal such a dependence, the concepts fixed and proportional loss have to be reconsidered.

Apart from the theory of 1/f noise in MOST[3], the oxide trap or McWhorter interface states model is not frequently used to describe the action of interface states in MOS devices. However, its applicability is supported by the strong observed correlation between the CCD transfer inefficiency and 1/f noise of on-chip MOS transistors[6].

5. CONCLUSION

Application of the Mc Whorter interface states model provides a quantitative description of the charge loss associated with a single storage gate as a function of bias charge, signal charge and channel width. The description is also consistent with experimental data of the small-signal charge transfer inefficiency in CCD's[2].

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