HTS Pulse-Stretcher and Second Order Modulator: Design and First Results

A. Roussy, S. Karthikeyan, I. Oomen, Th. Ortlepp, E. H. Sujiono, A. Brinkman, and H. Rogalla

***Abstract*—One of the remaining challenges in the application of superconducting electronics is the interfacing between superconducting and semiconducting environments. The voltage and speed mismatch between RSFQ pulses and semiconducting read-out electronics makes it necessary to amplify as well as stretch the RSFQ pulses. Moreover, circuits based on HTS (High Temperature Superconductor) technology are very attractive since they can operate under considerably relaxed cooling effort, which is one of the main problems with LTS (Low Temperature Superconductor) circuits.**

Within the European project SuperADC, a HTS second order sigma delta modulator and a pulse stretcher, used as an interface between the modulator and the first semi-conducting amplifier stage, have been designed at Twente University and will be presented here.

***Index Terms*—HTS superconductors, Josephson junctions, rapid single flux quantum, superconducting/semiconducting interface circuits.**

I. Introduction

RESEARCHERS have been interested for a long time in superconducting digital electronics. During the past few years, a rapid development of Josephson junction digital circuit has happened especially since the invention of the rapid single-flux quantum (RSFQ) logic. Circuits of this family store binary information in the form of single quanta of magnetic flux, $\Phi_0 = \mathrm{h}/2e \approx 2 \times 10^{-15}$ Wb. The process and the transfer of these single quanta are achieved in the form of some picoseconds voltage pulses with quantized area $\int V(t)dt = \Phi_0$. Circuits from classical superconductors can operate at some hundred GHz and the ones from high-$\mathrm{T_c}$ superconductor at frequencies above 1 THz [1]. The power dissipated in a device per clock cycle is many orders of magnitude lower than that of similar semiconductor circuits. The Josephson junction fabrication technology for high-$\mathrm{T_c}$ materials is not as well established as that for low-$\mathrm{T_c}$ materials, thus there have not been many reports about the successful operation of high-$\mathrm{T_c}$ SFQ logic circuits at high temperature and high speed. The HTS ramp edge Josephson junction technology allows for circuits with a maximum of 20–50 junctions [2]. Analog-to-digital conversion is an ideal application for RSFQ circuits because of the extremely high switching speed of the Josephson junctions and the achievable linearity, due to the intrinsically quantized operation which can give a big advantage over the state of the art semiconductor circuits [3], [4]. It is necessary to underline that, in any practical systems, superconducting circuits have to be combined with conventional semiconductor devices, to transfer, process and store the data. Considerable progress still has to be made in addressing the interface problem between semi-conducting and superconducting systems.

The European 'SuperADC'-project [5] tries to apply the state of the art of the superconductor and semiconductor world by combining a high-$\mathrm{T_c}$ $\Sigma\Delta$-modulator and a high-speed semiconductor decimation filter. Within this European project a sigma-delta second order modulator has been designed at Twente University. A pulse stretcher in HTS technology has also been designed to interface the modulator output with the first semiconductor amplifier stage. In this paper, the design of a pulse stretcher, as well as two possible models for its implementation in the general device will be described and finally, the design of the second order sigma-delta modulator will be explained.

II. Pulse-Stretcher

The modulator output is generating single SFQ (Single Flux Quantum) pulses. They have to be stretched in time to make them detectable for the amplifier. This can be done by a pulse-stretcher using a flip-flop and a delay line. A first pulse stretcher without the additional circuitry has been designed and fabricated to test the fabrication feasibility with the HTS Twente technology. After some successful experiments, a new pulse stretcher has been designed, simulated and optimized.

A. Description of the Pulse Stretcher Behavior

The RS flip-flop [6] circuit works as follows (Fig. 1): when a SFQ pulse is applied to the set input, junction J2 switches. The loop containing junctions J2 and J4 has a large enough inductance $(\mathrm{L2} + \mathrm{L3} + \mathrm{L4} + \mathrm{L5})$ to trap the generated flux quantum. If we now apply a reset pulse so that junction J4 switches, a flux quantum will be injected in the loop and is resetting the flip-flop. The escape junctions J1 and J3 shield the SFQ pulse sources from the back reaction in the case of a double set or reset pulse. The pulse stretcher is based on the same concept but now a dc-squid containing junctions J5 and J6 is coupled to the flip-flop [7], [8]. When a signal is applied to the set input, the flip-flop switches to state 1 and the junction J6 is providing a finite dc voltage at the output. When a pulse arrives from the reset input, the flip-flop switches to its initial state 0 and the output

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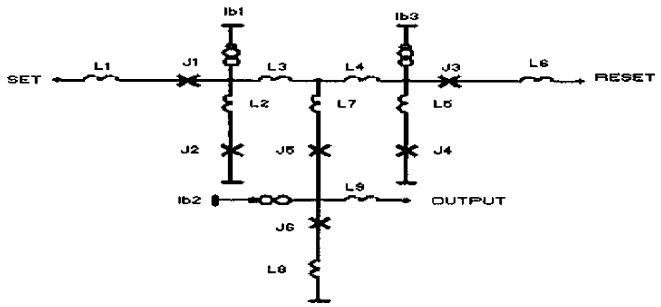

Fig. 1. Pulse-stretcher schematic with parameters: $\mathrm{Ic}_1 = \mathrm{Ic}_3 = 180\ \mu\mathrm{A}$, $\mathrm{Ic}_2 = 225 = \mu\mathrm{A}$, $\mathrm{Ic}_4 = 405\ \mu\mathrm{A}$, $\mathrm{Ic}_5 = 120\ \mu\mathrm{A}$, $\mathrm{Ic}_6 = 205\ \mu\mathrm{A}$, $\mathrm{L}_1 = 1.94\ \mathrm{pH}$, $\mathrm{L}_2 = 1.2\ \mathrm{pH}$, $\mathrm{L}_3 = 4.37\ \mathrm{pH}$, $\mathrm{L}_4 = 1.51\ \mathrm{pH}$, $\mathrm{L}_5 = 1.2\ \mathrm{pH}$, $\mathrm{L}_6 = 1.76\ \mathrm{pH}$, $\mathrm{L}_7 = 1.5\ \mathrm{pH}$, $\mathrm{L}_8 = 1\ \mathrm{pH}$, $\mathrm{L}_9 = 1\ \mathrm{pH}$, $\mathrm{Ib}_1 = 220\ \mu\mathrm{A}$, $\mathrm{Ib}_3 = 50\ \mu\mathrm{A}$, $\mathrm{Ib}_2 = 217\ \mu\mathrm{A}$.

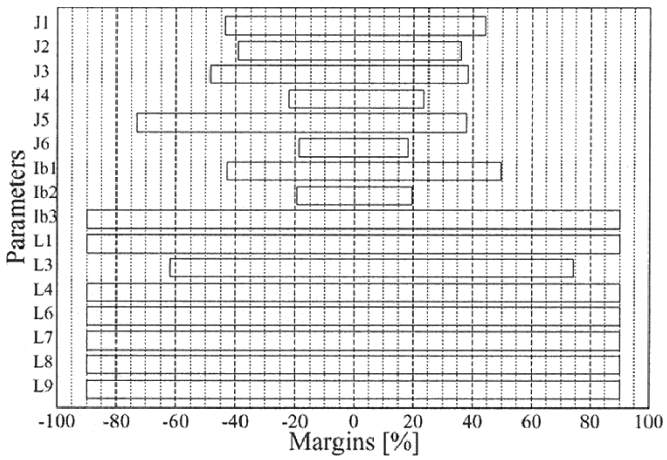

Fig. 2. Pulse-stretcher margins.

voltage drops back to 0. The output signal, with an average amplitude of several hundred microvolts, should be sufficient to be transferred to a semiconductor amplifier.

B. Design

The pulse stretcher has been simulated and optimized with the aim to achieve better margins and to present a set of parameters, which allows for a maximum fabrication yield. This circuit has been designed for the HTS ramp edge junction technology with a characteristic voltage $\mathrm{I_C R_N}$ of 600 μV [9]. The simulation, optimization and inductance calculations have been done with software such as Jsim, XOPT and Lmeter [10]–[12]. Simulation results show relatively large operating margins (Fig. 2) of the pulse stretcher. The optimized circuit correctly operates within $\pm 18\%$ deviation of the critical currents of the Josephson junctions and at $\pm 20\%$ deviation of the bias current. The fabrication yield has been obtained for 5000 Monte-Carlo runs for each assumed parameter spread value shown. Its value is 97% for 5% spread, 69% for 10%, 37% for 15% and decreases to 18% for 20% spread. The optimized pulse stretcher is applicable for fabrication and the margins should allow its implementation in a more complex circuit without a larger decrease of the margins. The output voltage is about 260 μV, which is a bit less than expected.

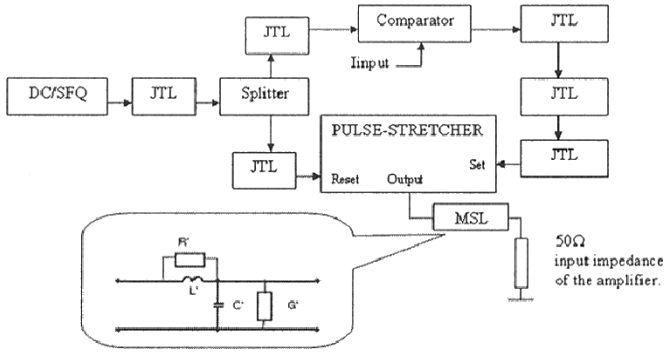

Fig. 3. Pulse-stretcher output load schematic (based on the internally set and reset first model). The parameters are the inductance L′, the capacitance C′, the surface resistance R′ and the insulation losses G′.

C. Load Connection

Interfacing superconducting electronics to semiconducting electronics is difficult because of the high speed (several gigahertz) and the low signal level (few millivolts) of the Josephson circuit devices. Therefore one needs circuits that at least provide a significant increase in the voltage level and reduce the speed, if possible. Impedance mismatch is also an important issue to be considered. A number of possible solutions have been developed and tested in niobium technology. SFQ-to-latch converters, voltage multipliers, SQUID amplifiers and SFQ-to-DC converters are some of the interesting circuits, that could in principle be applied to the problem A careful analysis has to be made for the case of HTS. SFQ-DC converters can be used because of the small number of junctions offering a significant yield even with large spread in the critical current. On the other hand, the output voltage is limited by the IcRn product of the output junction (around 1 mV). So an ultra-low noise, wide band, low input impedance semiconducting amplifier will be needed. At first we have studied the transmission of pulses from an HTS-circuit (a pulse stretcher) via a micro-strip line (MSL) to a load. We also studied the stability of the function of the pulse stretcher due to reflections caused by terminating MSL, applying different loads. The schematic of the circuit is shown in Fig. 3. We applied impedances of about 6.8, 8.4 ohms for 5 um, 4 um wide micro strip line, corresponding to parameters of the present HTS ramp type technology we are using. Jsim simulation results of the test circuit are shown with loads of 10 and 50 ohms. An increase in mismatch causes an increase in the voltage of the reflected pulses. We have found that the pulse stretcher was stable for a load range of 10 to 50 ohms and for frequencies up to 15 GHz, applying a 4 um wide MSL.

III. SET/RESET PULSE STRETCHER MODELS

The length of the output pulses is determined by the delay, which is equal to the time difference between the set and the reset input signals. This length should be large enough to be easily detected by the amplifier input and the set and reset signals should be generated internally at the circuit. A Josephson Transmission Line (JTL) could be used as delay line, but for long pulses this implies that a JTL with many junctions has to be used. It complicates the circuit and risk of incorrect operation. So, this option has been given up and two others models

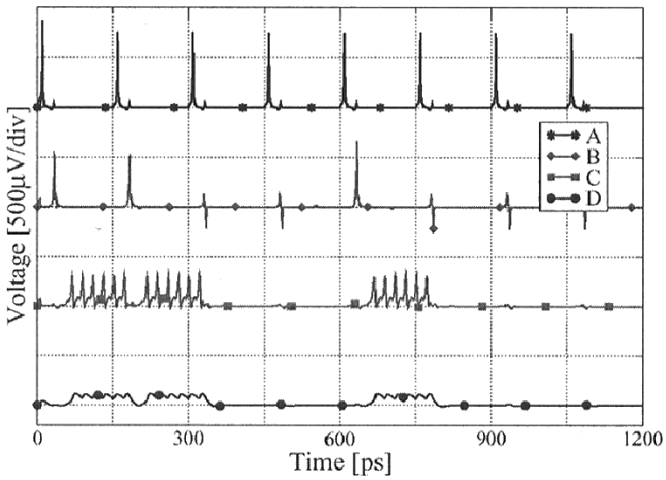

Fig. 4. Simulation of the first model of internally set and reset Pulse stretcher (clock frequency: 6 GHz). The output signal corresponds to a bit stream of 11 001 000. Curve (A) represents the DC/SFQ output, (B) the comparator output, (C) the pulse-stretcher junction J6 and (D) the pulse stretcher output.

of delay lines with internally generated set and reset pulses not making use of JTL delays have been studied. The two models are based on RSFQ cells such as DC/SFQ converter, Josephson transmission line, splitter and comparator which have been simulated and optimized for our HTS technology [13].

A. First Model

This model includes one DC/SFQ converter, one splitter, Josephson transmission lines and one comparator shown in Fig. 3. The model works as follows. From the DC/SFQ converter, SFQ pulses propagate through a JTL with the aim to improve the signal quality for driving a splitter. Its output signals are going in two directions. The one through a JTL will reach the pulse stretcher reset input. In parallel the other one will go through a comparator. If the input current is higher or lower than a certain threshold value, either the lower or upper junction of the comparator switches in response to the sampling pulse. The output signal of the lower junction will be provided through a longer JTL to the pulse stretcher set input.

Fig. 4 shows the operation of the first model. Correct behavior of first model has been achieved. Optimization of this circuit yields critical margins of $\pm$10–15%. This model is very interesting because everything is fixed by the design itself: the delay between set and reset signals but also the timing characteristics of the comparator. All these parameters are fixed by the clock input frequency. This circuit includes 28 junctions but only a few of them are critical. The reset pulse should arrive at the pulse stretcher before the set pulse. We calculate a timing jitter of $\sigma = 0.46$ ps per junction. By counting 6 junctions in the path JTL+splitter+JTL it yields a timing window $5\sigma = \pm 5.63$ ps [14]. This demands a set pulse arriving approximately 6 ps after the reset pulse. The output voltage of the pulse-stretcher is too low (only 150 μV) for being detected by the first amplifier stage with sufficient SNR, a superconducting amplifier stage should be added to further increase the output voltage.

B. Second Model

As an alternative design a second clock signal could be used as reset signal and so the delay can be placed outside the HTS

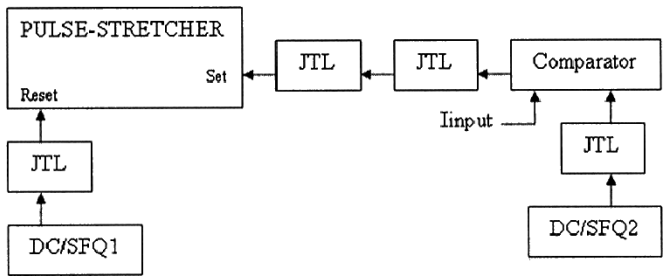

Fig. 5. Second model concept.

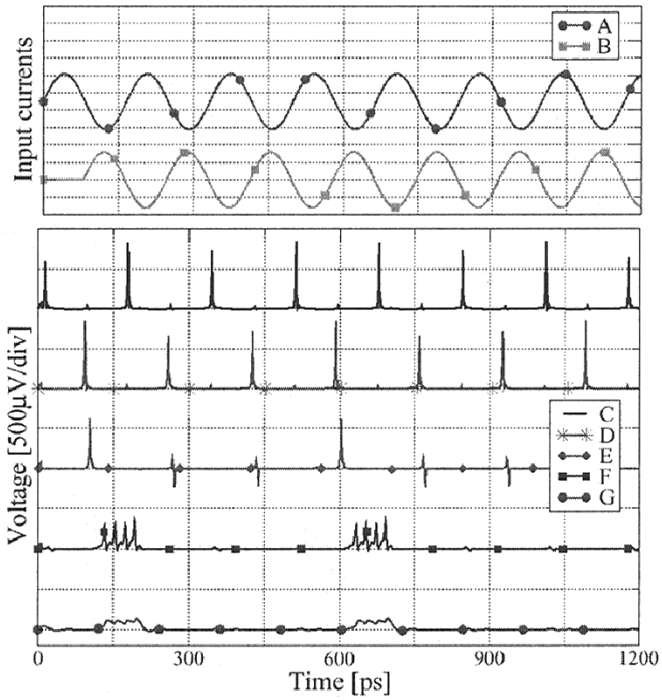

Fig. 6. Simulations of the second set reset Pulse stretcher model (6 GHz). The output signal corresponds to a bit stream of 1 001 000. Curve (A) represents the DC/SFQ1 input, (B) the DC/SFQ2 input, (C) the DC/SFQ1 output, (D) the DC/SFQ2 output, (E) the comparator output, (F) the pulse-stretcher junction J6 and (G) the pulse-stretcher output.

chip decreasing the number of junctions. The model includes two DC/SFQ converters, Josephson transmission lines, a comparator and the pulse-stretcher. The two DC/SFQ converters are fed by a sinusoidal input signal with a phase different of 180 degree (Fig. 5).

The output signal from the DC/SFQ1 output reaches the reset port of the pulse-stretcher input through a JTL. Half a period later, the signal from the DC/SFQ2 output reaches the comparator stage. As previously explained, depending on the comparator output, its output signal will be set the pulse-stretcher output. Fig. 6 shows the operation of the second model. The optimization of this circuit yields the lowest margin requirements with $\pm$15%. The circuit includes 24 junctions. To conclude, the operation of the second model is simpler than that of the first model on the cost of a not totally internal set and reset circuit. In terms of energy losses and performance a better behavior is expected from the first model. Although its fabrication will be more critical than the fabrication of the second model, in the

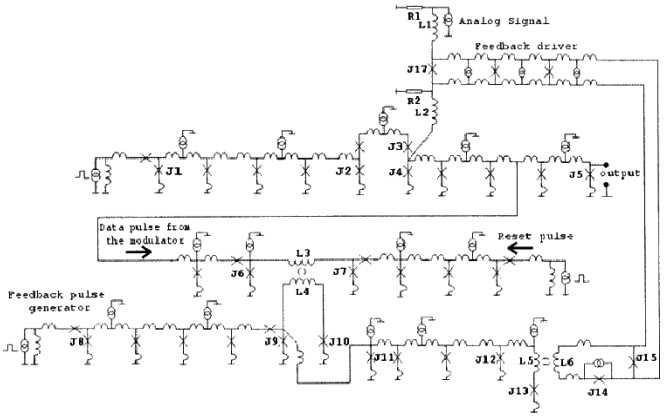

Fig. 7. Second order $\Sigma\Delta$ modulator schematic.

case of a practical implementation in the global circuit, the first model is the better choice.

IV. Second Order $\Sigma\Delta$-Modulator

Sigma-delta modulators are very attractive because of their high dynamic range and noise shaping property [15]. First order modulators need a very high sampling rate to achieve a high-resolution digital output. Lack of high-speed digital processing circuits limit the use of first order superconducting delta-sigma modulators at a high sampling rate. Improvement in the dynamic range is obtained by adding feedback loops. Higher order modulators can obtain high SNR at much smaller sampling rates. A second order modulator uses two integrators with double feedback paths, which make the circuit more complicated than the first order modulator. We have studied the possibility of realizing a second order modulator in HTS technology. The designed circuit is shown in Fig. 7. The analog signal is integrated by two successive integrators and then sampled by the comparator circuit. The output of the comparator is fed to a splitter. One of the splitter ports is sent to a JTL and taken as output. The other port sets the RS-flipflop comprising J6, J7 and L3. The flipflop will be reset by a clock signal of such a frequency that the duration between the set and reset pulse is less than the time period of the sampling clock. Setting and resetting the flipflop will change the direction of the current in the inductor L4, which is mutually coupled to L3. So the flux quantum pulses generated by the junction J8 will be transferred to J11 during the time the flipflop is in the 'on'-state. The pulses across J11 will be applied to the first integrator via a DC isolator, a feed back driver and J17. The number m of pulses feedback to the first integrator will depend on the frequency of the pulses generated across J8 and the time, for which the flipflop is in the 'on'-state. The pulses across J11 will be applied to the first integrator via a DC isolator, a feedback driver and J17. The number m of pulses feedback to the first integrator will depend on the frequency of the pulses generated across J8 and the time, for which the flipflop is in the 'on'-state. The number of feed back pulses will be controlled by carefully choosing the frequency of the clock pulse of the feedback pulse generator, and the reset pulse generator. The circuit was simulated for $\mathrm{m} = 4$ and 6. For $\mathrm{m} = 6$, the fast Fourier transform of the modulator output shows the characteristic noise shaping property giving a dynamic range of 86 dB for a 40 MHz signal at 10 GHz sampling rate. Its realization in HTS technology is strongly limited by the large spread in circuit parameters.

V. Conclusion

A design of a HTS pulse-stretcher is first discussed in this paper including two internally set and reset models. Their design should not involve large fabrication problems using the Twente HTS ramp edge technology. The fabrication is in progress and we plan to include these pulse stretchers as an output stage in the described second order $\Sigma\Delta$-modulator device. The reliability of the data transfer between the superconducting modulator and the semiconducting amplifier depends strongly on the voltage amplitude of the pulse stretcher. We plan to further improve the circuit design by including the rf-properties of the interconnect and of the semiconducting amplifier in the pulse stretcher design.

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