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Platinum Patterning by a Modified Lift-Off Technique and Its Application in a Silicon Load Cell

H. D. Tong*, R. A. F. Zwijze, J. W. Berenschot, R. J. Wiegerink, G. J. M. Krijnen and M. C. Elwenspoek

MESA+ Research Institute, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands

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In micro-electromechanical systems (MEMS) and micro-electronic devices there has been a strong demand for electrode materials which can survive in highly oxidizing and high-temperature environments. Platinum (Pt) is a good candidate for this, because it combines several attractive properties: low electrical resistance, high melting point and high chemical stability. However, the chemical stability is a problem for patterning Pt by wet chemical or dry etching. Standard lift-off seems to be a solution to this problem. A big problem in using standard lift-off is that platinum particles or wing tips (ears) may remain at the edges after lift-off. These wing tips protrude from the surface and may cause short circuits with an opposite electrode placed within 1 μm. Some authors reported briefly on a modified lift-off technique to overcome this problem. Before deposition, a resist is patterned on an insulator to define openings where the metal is to be deposited. Afterwards, a small cavity is etched in the insulator, which is mostly SiO_2. The cavity facilitates the separation of the metal on the resist and the metal in the cavity. In this study the effect of cavity depth and sputtered metal thickness on wing tip formation is investigated. In addition, surface roughness, resistance and hillock formation of the as-deposited metals are measured. The modified lift-off technique has succesfully been applied in a silicon load cell with Ti/Pt electrodes.

*Corresponding author, e-mail address: T.Hien@el.utwente.nl

1. Introduction

1.1 *General Introduction*

Many micro-electromechanical systems and micro-electronic devices require metallizations that can withstand high temperatures. For example, a microfabricated chemical reactor system needs thin metal films for heating and temperature sensing that are able to withstand prolonged exposure to 1,000°C.[1] Moreover, in MEMS, very often the metal has to survive cleaning procedures and pretreatment of wafers in an oxygen-rich environment before wafer bonding.[2] Most metals are affected if subjected to one or more of these conditions. However, platinum (Pt) does not have (or hardly has) any of these problems while having a resistance that is only four times higher than the resistance of aluminum. With a melting point of 1,772°C and inertness to many chemicals such as HNO_3 and Piranha,[3] it has been widely used. For instance, in refs 1, 4 and 5 Pt is used as electrode material or sensing elements in MEMS devices. It is also often applied as electrode material for advanced memory chips such as dynamic random access memories (DRAMs),[6] nonvolatile ferroelectric random access memories (FRAMs),[7] opto-electronic devices[8] and many other applications in sensor technology.

Capacitive load cells have been studied and developed in our research group,[9-11] and Pt has been a candidate for use in a capacitive silicon load cell.[11] The mechanical analysis and measurements are presented in ref. 11. The technological aspects with respect to the Pt electrodes are discussed in the present paper. A schematic drawing of the load cell is shown in Fig. 1. The design consists of two bonded silicon wafers. The top wafer contains poles that bear the load. The bottom wafer contains an electrode pattern, deposited on SiO_2, and forming an array of capacitors with the top wafer as a common electrode. The gap distance between the capacitors is about 1μm. Upon application of a load, the bearing poles are compressed and the distance between the metal electrodes and capacitor poles decreases, thereby increasing the capacitance. The change in height of each pole due to the applied load can be expressed (assuming that the force distribution is homogeneous on the surface of a single pole) as

$$\Delta l = \frac{l_{\mathrm{pole}}}{EA_{\mathrm{pole}}} F_{pole}, \tag{1}$$

where l_{pole} and A_{pole} are the height and surface area of a pole, respectively, E is Young's modulus and F_{pole} is the force acting on a pole. For each capacitor, the capacitance is given by

$$C = \frac{\varepsilon_{\mathrm{air}} A_{\mathrm{cap}}}{d_0 - \Delta l}, \tag{2}$$

where $\varepsilon_{\mathrm{air}}$ is the dielectric constant of air, A_{cap} the surface area of each capacitor and d_0 the distance between the capacitor plates with no load applied.

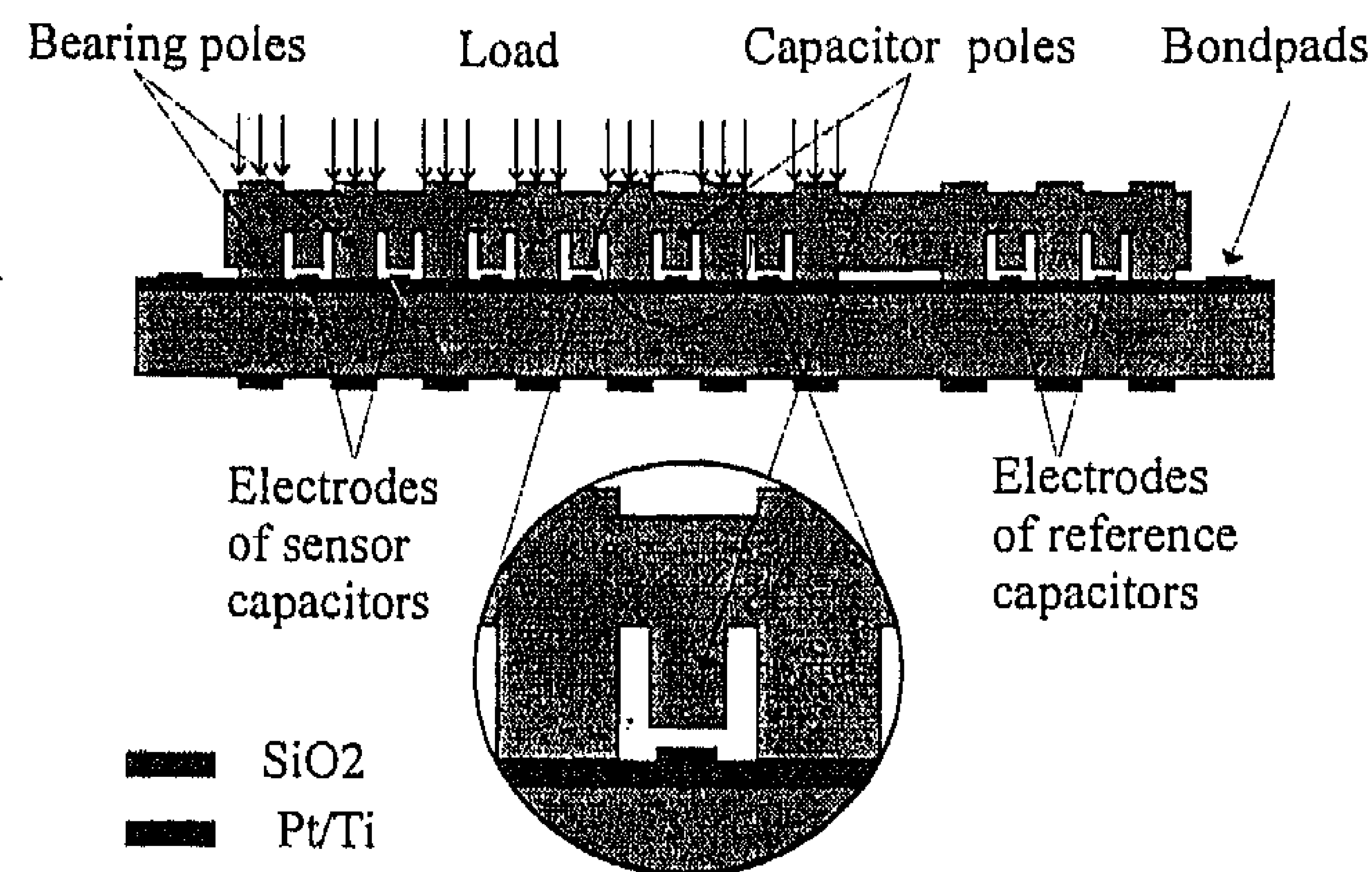


Fig. 1. Cross section of the capacitive silicon load cell sensor.[11]

For the load cell the electrode material must fulfil the following criteria:

· The metal must adhere well to the SiO_2 layer.

· The metal must survive the wafer cleaning step prior to the bonding and annealing steps to increase the bond strength between the two wafers.

· Hillock formation (spikes on the metal surface) due to annealing may not cause electrical short circuits with the opposite electrode.

· The Pt layer must by patterned in such a way that wing tip formation is prevented, that there is no redeposition of the metals and that the underlying insulating layer is not damaged.

These aspects are dealt with in the next three sections.

1.2 *Adhesion*

The adhesion of Pt to SiO_2 is very poor. Therefore an intermediate layer is needed. Al-Shareef *et al.*[12] reported that neither ZrO_2 nor TiO_2 is as effective as Ti in promoting Pt adhesion. Kondo *et al.* also reported on the good adhesion properties of Ti.[13]

1.3 *Wafer cleaning before bonding*

For the cleaning step just before bonding, both wafers are put in a Piranha mixture (H_2SO_4: $H_2O_2 = 3:1$) at 100°C for 20 min. Tests with Ti/Pt layers showed that these layers survive this step.

1.4 *Hillock formation*

Hillock formation in Ti/Pt films is a subject that should also be addressed. Eichorst and Baron[14] reported that hillocks may be avoided using relatively thin layers (Ti<10 nm, Pt<80 nm) or by deposition at elevated temperatures (200–600°C). However, these thin layers may lead to pinholes in the Ti,[14] which means that there is locally a poor adhesion of the Pt to the SiO_2. Hren *et al.*[15] reported on the appearance of hillocks in thicker Ti/Pt

bilayers deposited on oxidized silicon wafers. Platinum films of 250 to 300 nm were deposited on a 70 nm Ti film by ion beam sputtering at temperatures of 25°C and 300°C. The wafers were then heated to 600°C in flowing argon, held 1 h at 600°C and cooled to room temperature while the wafer curvature (and hence the film stress) was measured with a laser beam deflection technique. At 600°C, compressive stresses of 0.1 to 0.4 GPa developed in the metal films due to thermal expansion mismatch. The platinum surface, initially flat, showed strong hillocking after annealing. Cross-sectional TEM revealed that severe Ti/Pt interdiffusion occurred, in one case leading to a Ti layer on the top surface.

To determine the influence of the thickness of the Ti layer and annealing temperature, several experiments were performed in our clean room where AFM was used to measure the maximum heights of hillock. The results after 2 h annealing are shown in Fig. 2. From this data it is concluded that, independent of the Ti thickness, the height of hillock is smaller than 70 nm for annealing temperatures below 600°C. This height is much less than the electrode distance of 1 μm. The Ti (40nm)/Pt (300nm) layer appears to have the lowest hillocks. The annealing temperature of 600°C was sufficiently high to increase the bond strength between both wafers.

1.5 *Patterning*

The problem of Pt metallization is that it is difficult to pattern because of the high chemical stability. Although many methods such as wet etching,[16] dry etching[17] and a combination of wet and dry etching[18] have been developed to etch Pt, some problems remain. For example, Pt redeposition during dry etching is still not very well controlled.[17] This causes difficulties in direct wafer bonding, because the bonding surface is contami-

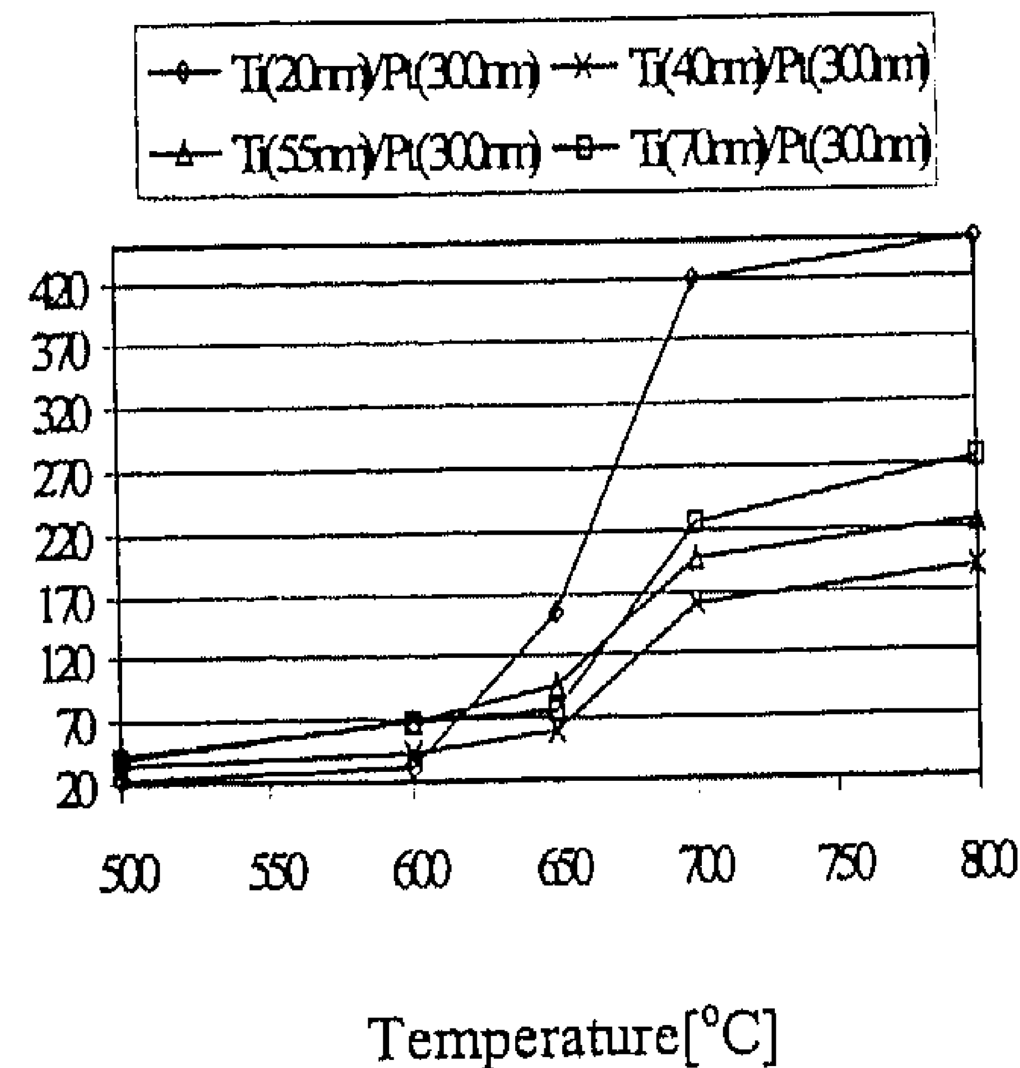


Fig. 2. Maximum height of hillock for different Pt/Ti layers annealed for 2 h at different temperatures.

nated by metal. In addition, etching can attack silicon and SiO_2, making the bonding surface too rough for direct wafer bonding.

Lift-off of Pt seems to be an attractive solution to these problems. In this method, a patterned layer of photoresist is used. After Pt is deposited, the resist layer is removed by acetone in an ultrasonic bath. In this way, the Pt layer remains in the areas where it is intended.

Using lift-off, the profile of the deposited metal depends mainly on the profile of the patterned resist since the resist wall separates the deposited metal from the undesirable metal. The resist profiles, which depend on resist types and mainly on lithography conditions, were described thoroughly by Moreau.[19] For instance, suitable types for lift-off are vertical and overcut resist profiles, which are normally achieved with ion-beam and X-ray (non-scattering) exposure. But with e-beam, X-ray or ion-beam exposure, the resist sensitivity and thermal stability are critical requirements. In addition, the costs are relatively high. Presoaking of some specific resists in suitable solutions can help to create the desired resist profiles. However, the resist still needs to be exposed to e-beam or deep-UV.

For these reasons, the resist is conventionally exposed to photon sources. However, in this case the resist slopes at the edges are smaller than 75° due to diffraction, multiple reflection or light oversteps, variable resist thickness from nonplanarization.[19] An example is shown in Fig. 3 for an Olin 907/17 positive photoresist.

Due to the positive slope of the photoresist, a thin sheet of metal is deposited on the side wall itself. Then, when the deposited metal is relatively flexible, or when the ratio between metal structure size and photoresist thickness is too small, lift-off removes all photoresist, but not the metal that is deposited on the side wall.[20] This phenomenon is called wing tip or ear formation. An example of a wing tips is shown in Fig. 4. In this case, the thicknesses of the Olin 907/17 resist and the Ti/Pt layer are 1.7 μm and 310 nm, respectively.

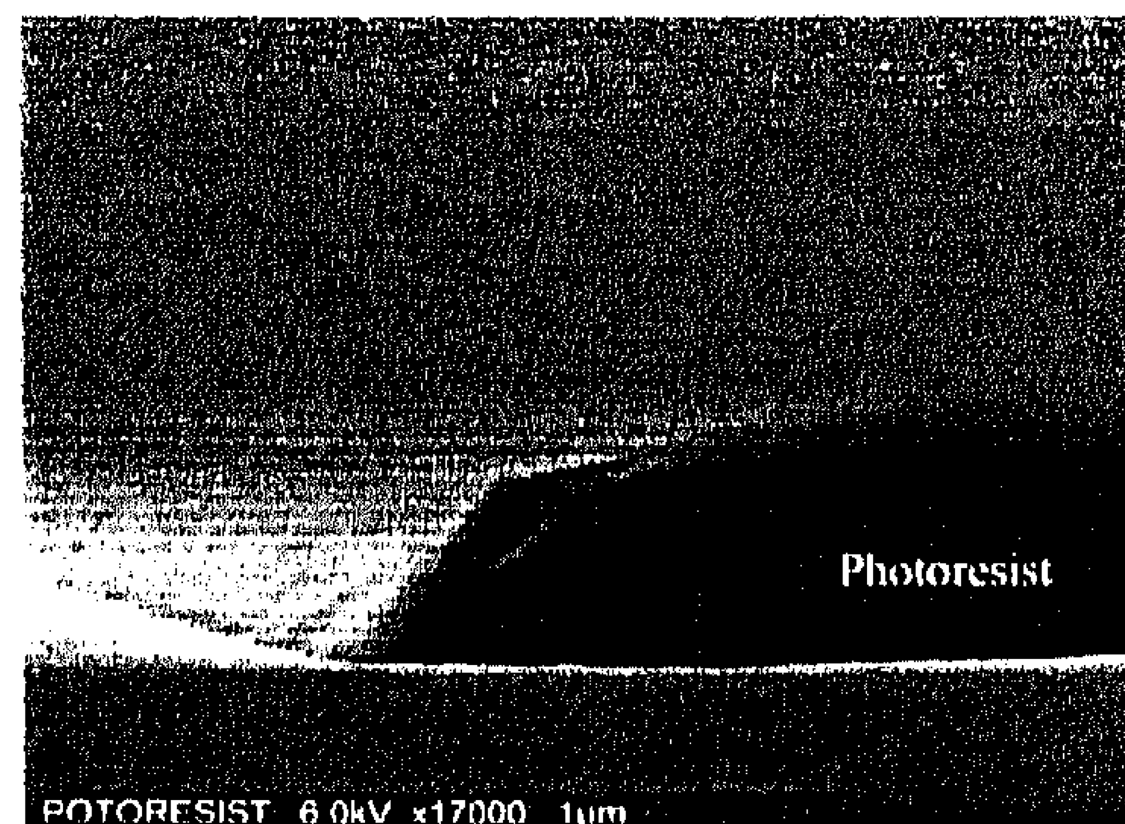


Fig. 3. SEM image of an Olin 907/17 positive photoresist, which was exposed by an Electronic Vision AL-6 mask aligner, developed and then annealed at 120°C for 45 min. The photoresist slope at the edge is estimated to be 60°.

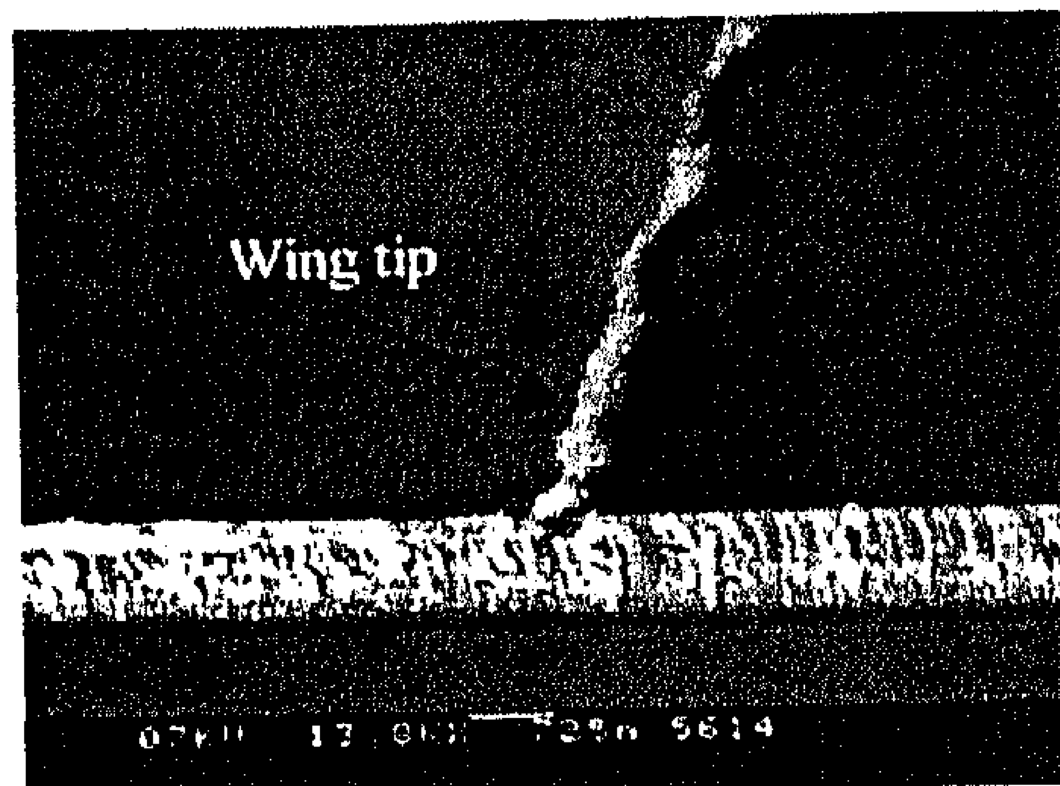


Fig. 4. SEM image of a Pt wing tip. The height of the Pt wing tip is about 500 nm.

It is evident that these wing tips can cause electrical short circuits with an opposite electrode placed within 1 μm of them. To prevent wing tip formation, a modified lift-off technique was developed, the process for which is shown in Fig. 5.[20,21] The basic idea is that the cavity etched in SiO_2 facilitates the separation of the metal deposited on the resist and the metal in the cavity. However, no elaborate study is reported in the literature on the modified lift-off technique. In this paper, the influences of the Ti/Pt thickness and the cavity depth are discussed.

2. Modified Lift-Off: Experiments

Figure 5 shows a schematic overview of the modified lift-off process. First, a 1 μm layer of wet thermal SiO_2 was grown on a 3-inch silicon wafer. Evaporated hexamethyldisilazane (HMDS) served as an adhesion promoter for the subsequent resist layer. A Positive Olin 907/17 resist was coated by spinning, resulting in a thickness of 1.7 μm. Then, a conventional photolithography process was carried out to define the windows. After development, the wafers were given a post-bake at 120°C for 45 min to strengthen the photoresist and to increase the adhesion between the photoresist and the SiO_2. Then the cavities in the SiO_2 were etched isotropically in a buffered HF-solution (1:7) at an etching rate of 70 nm/min. Due to isotropic etching of SiO_2, underetching of the photoresist occurred (see Fig. 6). After this, the wafers were rinsed in deionized water and spun dry. This step was directly followed by DC magneton sputtering of the metal(s). Layers of Pt with different thicknesses were deposited on a 40-nm-thick Ti adhesion layer. The bilayer was sputtered in one run without breaking the vacuum. The lift-off process was carried out in an ultrasonic acetone batch for 30 min at room temperature.

To investigate the possibility of applying the modified lift-off method to other metals, 300-nm-thick tantalum (Ta) layers were also deposited.

In Fig. 5, M is defined as the total thickness of the deposited metal layers and S is defined as the depth of the SiO_2 cavity. The influence of different K = M/S ratios on wing tip

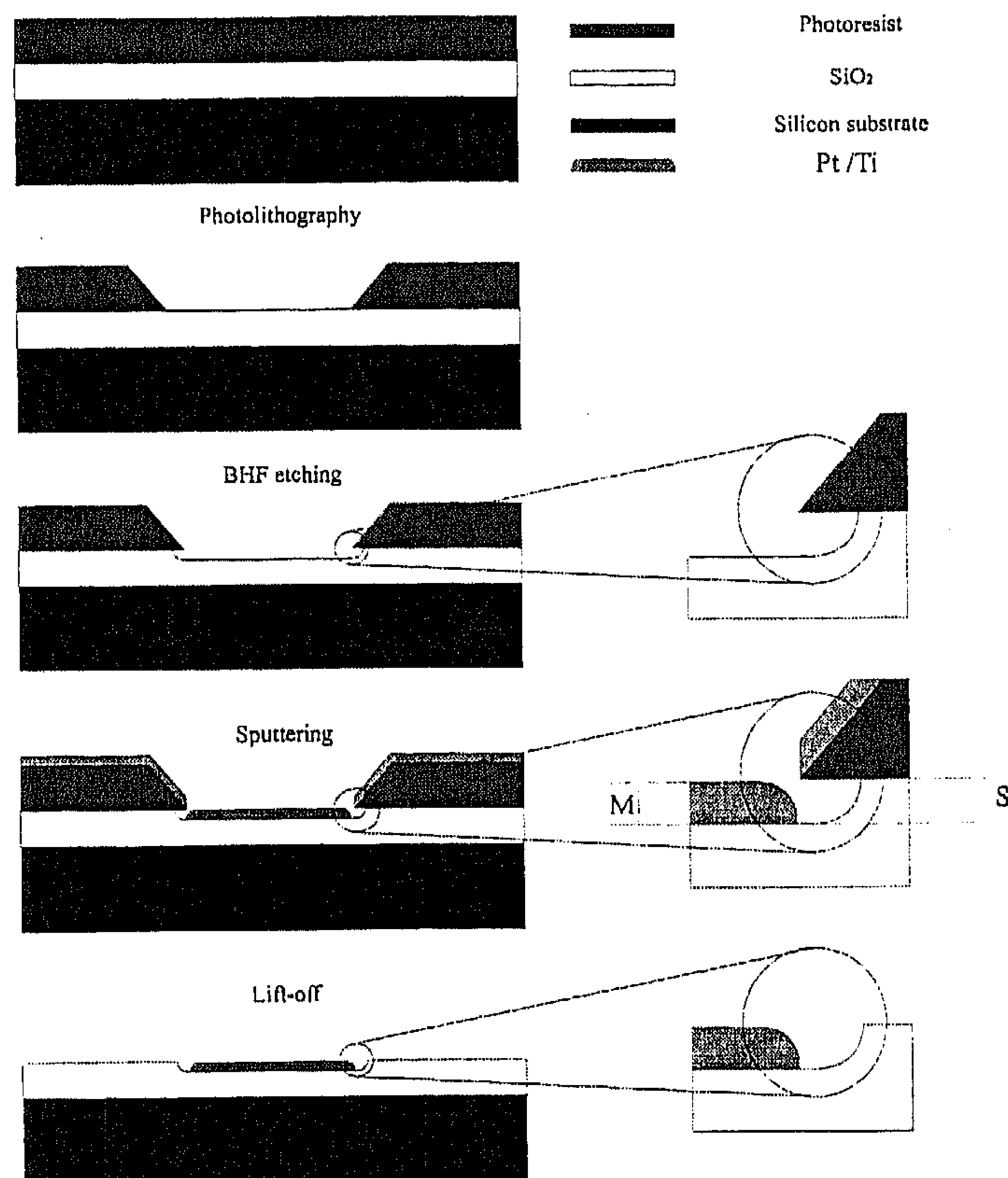


Fig. 5. Schematic overview of the modified lift-off process.

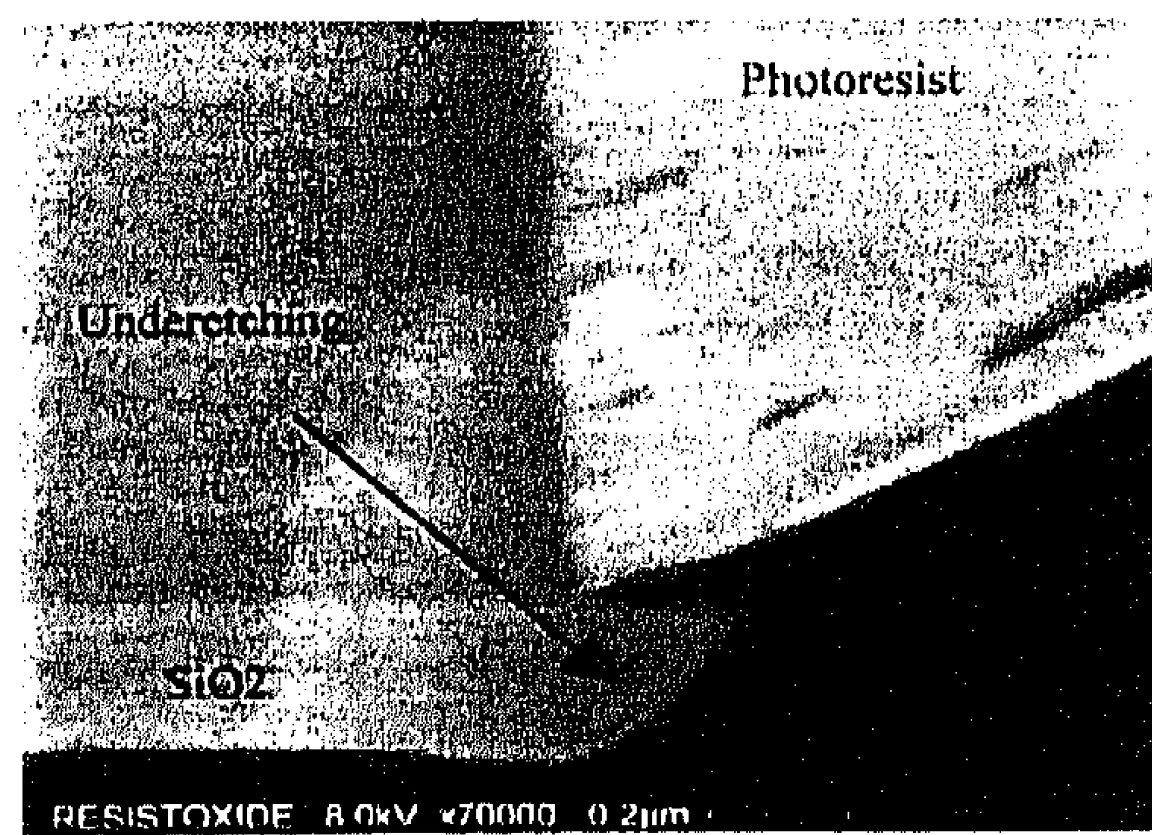


Fig. 6. SEM image of the underetching of the photoresist created by etching in BHF (1:7) for 3 min. The underetching is estimated to be 210 nm.

formation was investigated by SEM (scanning electron microscopy). In Table 1, the parameters of the different experiments are shown. The following considerations should be taken into account in looking at the table:

• The average roughness of samples 2 and 3 is expected to be the same because they have the same thickness (400 nm)

• *R*a is the average roughness of a Ti/Pt layer that was patterned by the modified lift-off method.

• *R*a* is the average roughness of a Ti/Pt layer that was directly sputtered onto a clean SiO_2/Si substrate without a resist layer.

• *R* is the square resistance of a deposited metal layer that was patterned by the modified lift-off method.

• *R* * is the square resistance of a Ti/Pt layer that was directly sputtered onto a clean SiO_2/Si substrate.

• Resistivity and average roughness of sample 5 were not considered due to wing tip formation.

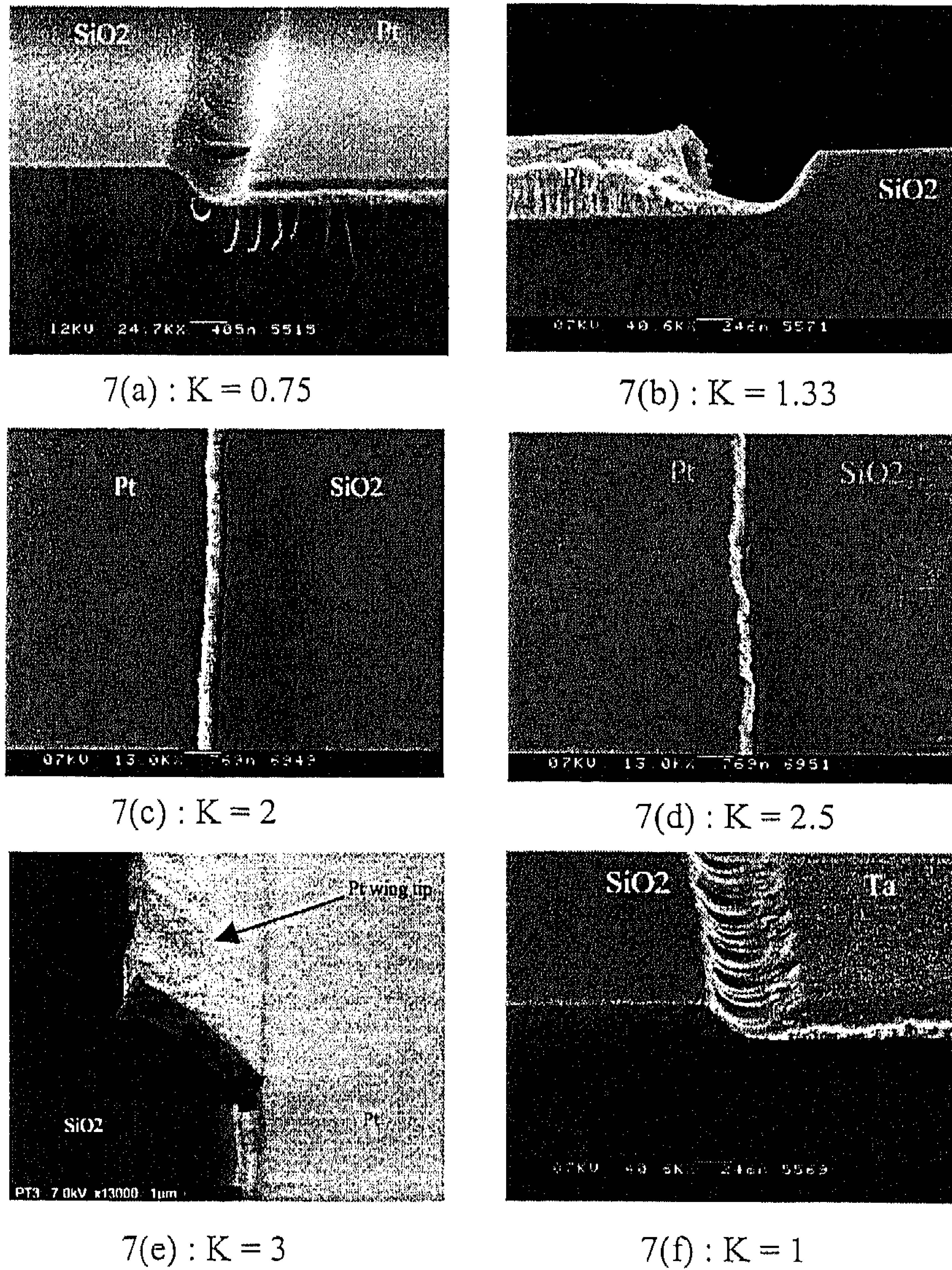
3. Results and Discussion

3.1 *Metals deposited at different K ratios*

Various layers of Ti/Pt at different K ratios were deposited and patterned. After removing the photoresist in ultrasonic acetone, samples were divided into small pieces and investigated by SEM. The SEM pictures of samples 1 to 6 are shown in Figs.7(a) to 7(f). From these pictures it appears that no wing tips or islands of Pt remain at the edges for K ratios up to 1, because no "metal bridge formation" occured. For $1<K\leq2.5$, it seems that a "metal bridge" between the deposited metal and undesirable metal was formed after

Table 1
Parameters for the different samples.

Sample number	1	2	3	4	5	6
Metal	Pt/Ti	Pt/Ti	Pt/Ti	Pt/Ti	Pt/Ti	Ta
S (nm)	400	300	200	200	200	300
M (nm)	300	400	400	500	600	300
K	0.75	1.33	2	2.5	3	1
SEM figure	7(a)	7(b)	7(c)	7(d)	7(e)	7(f)
Remark	No wing tip	No wing tip	No wing tip	No wing tip	Wing tip	No wing tip
AFM figure	8(a)	8(b)	*	8(d)		
Ra (nm)	3.2	2.7	*	2.9		
Maximum peak (nm)	5	4	*	4		
*R*a* (nm)	3.1	2.5	*	2.9		
R (Ω)	0.61	0.43	0.43	0.31		
R * (Ω)	0.57	0.41	0.40	0.29		



7(a) : K = 0.75 7(b) : K = 1.33

7(c) : K = 2 7(d) : K = 2.5

7(e) : K = 3 7(f) : K = 1

Fig. 7. SEM images of the deposited layers.

deposition, but it was subsequently broken in the ultrasonic acetone bath. Appareently, the underetching of the photoresist seems to be the reason for the success of the modified lift-off method, since it helps to separate or break the deposited metal from the undesirable metal.

However, wing tip formation is clearly visible after modified lift-off with a deposited Ti/Pt layer for which K = 3 (see Fig.7(e)). In this case the underetching of the photoresist is not sufficient to break the "metal bridge."

3.2 *Application of the modified lift-off method for other materials*

As shown for Ta (see Fig.7(f)), the modified lift-off technique can also be used for other metals. Of course, these metals can be etched by wet or dry etching, but redeposition and damage of the insulator layer (SiO_2) may be undesirable effects.[22]

3.3 *Roughness and resistance of as-deposited metals*

In the lift-off technique, a photoresist layer is patterned and used as a shadow mask. However, due to the removal of resist, organic residues may remain which influence the as-deposited thin film.[23] In addition, organic residues may be present due to redeposition of photoresist during sputtering. These residues influence the roughness and resistance of the film. The roughness and resistivity of as-deposited Pt/Ti thin films were compared to those in which Pt/Ti was sputtered directly onto clean SiO_2/Si substrates under the same conditions. The roughness and resistance were measured by a dimension 3100 AFM (atomic force microscope) and a Matheson resistivity prober, respectively. The differences between both measurements are shown in Table 1. The AFM images of the surfaces of as-deposited Ti/Pt films are shown in Figs. 8(a), 8(b) and 8(d).

From this data we observe that the resistance and roughness of the lift-off deposited Ti/Pt films are always higher than those of normal sputtered Pt/Ti films. However, the differences are quite small and the maximum peak height is always less than 10 nm.

4. Conclusions

A low-cost modified lift-off technique for preventing wing tip formation was investigated in detail. In this technique, SiO_2 is partly removed to create underetching, which is necessary to prevent the formation of Pt wing tips at the edges of the window. The results show that this technique can be applied to deposit and pattern Pt successfully. Moreover, the results for other materials seem promising. A wide range of K ratios was investigated and the results demonstrate that the modified lift-off method can be utilized for K ratios up to 2.5. However, deposition and patterning of layers with $K \geq 3$ results in wing tip formation.

In this study, the influence of organic residues on roughness and resistivity was also investigated. The differences between Ti/Pt deposited on wafers with and without photoresist are very small.

The modified lift-off technique has been successfully applied to pattern Pt electrodes for use in a silicon load cell. The load cell chip and an array of Ti/Pt electrodes are shown in Figs. 9(a) and 9(b), respectively.[11]

All of these results lead to the conclusion that the modified lift-off method can be a powerful tool for depositing and patterning Pt as well as other metals.

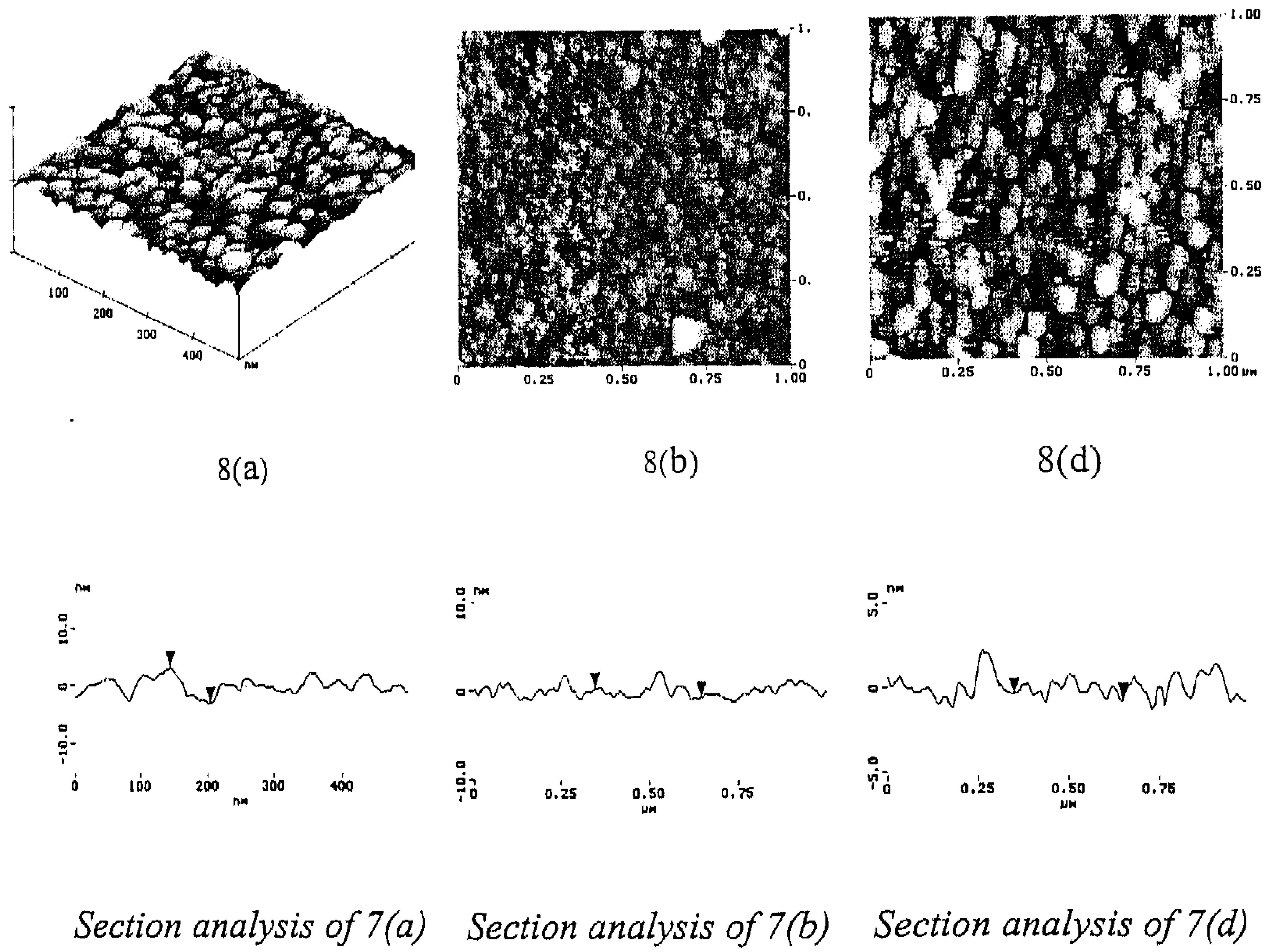


Fig. 8. AFM surface measurements.

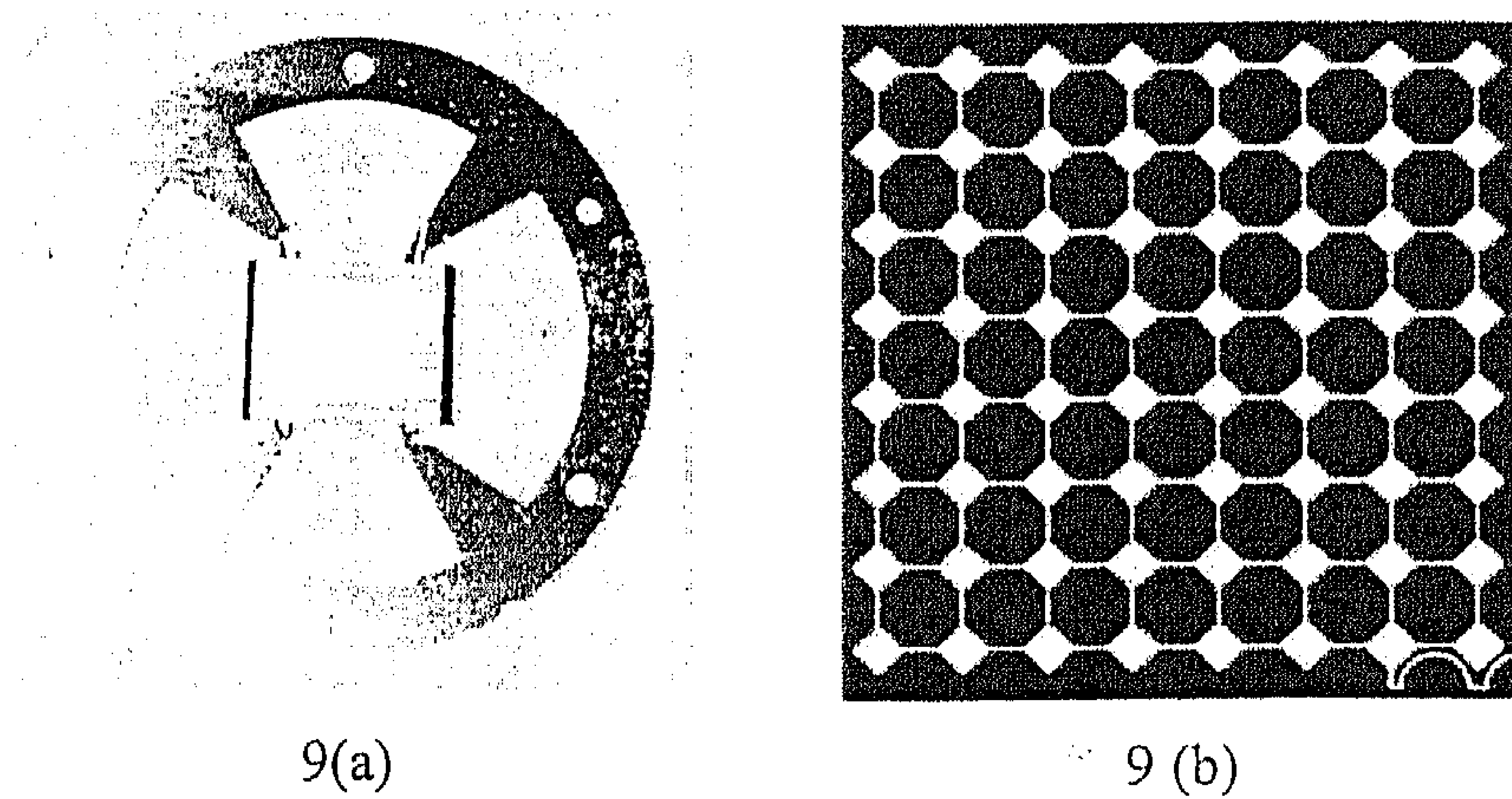


Fig. 9. (a) Silicon load cell chip and (b) array of the as-deposited Pt electrodes.

Acknowledgements

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References

1 S. L. Firebaugh, K. F. Jensen and M. A. Smidt: Journal Microelectromechanical Systems **7** (1998) p.128.
2 Q. Y. Tong, U. Goesele: Semiconductor wafer bonding: science and technology (Wiley-Interscience, 1999).
3 R. C. Weast: CRC handbook of chemistry and physics, 67th edition (CRC press, 1986–1987).
4 M. Dibattista, S. V. Patel, K. D. Wise, J. L. Gland and J. W. Schwank: Characterization of multilayer thin film structures for gas sensor applications, Symposium. Mater. Res. Soc (Pittsburgh, PA, USA; 1995) xii+496.
5 A. Verholen: Characterization of Lead zirconate titanate (PZT) thin film for applications in micromachining, thesis, University of Twente, May, 1997.
6 S. J. Kang, Y. S. Yoon: J. of Korean Inst. of Tel. and Elec. **32A** (1995) 78.
7 Y. Furumura, T. Yamazaki, M. Nakamura, S. Nakajima, M. Imai and T. Takesima: Proc. SPIE. **3506** (1998) p. 56.
8 A. Appelbaum: Proc. SPIE. **1219** (1990) p. 294.
9 R. J. Wiegerink, R. A. F. Zwijze, G. J. M. Krijnen, T. S. J. Lammerink and M. C. Elwenspoek: Proc. MEMS'99 (Orlando, U.S.A., 1999) p. 558.
10 R. J. Wiegerink, R. A. F. Zwijze, G. J. M. Krijnen, T. S. J. Lammerink and M. C. Elwenspoek: Proc. of Eurosensors XIII (The Hague, September, 1999) p. 545.
11 R. A. F. Zwijze, R. J. Wiegerink, G. J. M. Krijnen, H. D. Tong and M. C. Elwenspoek: Proc. of ASME conference (Florida, USA, 2000).
12 Al. Shareef, D. Dimos, B. A. Tuttle and M. V. Raymond: J. Materials Research **12** (1997) 347.
13 I. Kondo, T. Yoneyama, O. Takenaka: J. Vac. Sci. Technol. A **10** (1992) 3456.
14 Eichorst, D. J., and Baron, C. J.: Ferroelectrics **166** (1995) 73.
15 P. D. Hren, S. Rou, Al. Shareef and M. Ameen: Advanced metallization and processing for semiconductor devices and circuits, ii. symposium. mater. res. soc (Pittsburgh, USA, 1992) p. 575.
16 S & A lab manual, MESA book, University of Twente, 1995.
17 A. Cofer, P. Rajora, S. DeOrnellas and D. Keil: Int. Ferroelectrics. **16** (1997) 53.
18 A. Lecours, M. Meunier and M. Bisson: J. Vac. Sci. Technol. B. **8** (1990) 109.
19 W. M. Moreau: Semiconductor lithography: Principles, Practices and Materials (Plenum Publishing, New York, 1991) Ch. 12.
20 D. Wijngaards, M. Bartek and R. Woffenbuttel: Sensors and Actuators A **68** (1998) 419.
21 K. Reimer, C. Kohler, T. Lisec, G. Fuhr and B. Wagner: Sensors and Actuators A **46–47** (1995) 66.
22 M. Chuang, K. Hsieh and A. Chu: J. Electrochem. Soc. **145** (1998) 1020.
23 S. Thakoor: J. Appl. Phys. **75** (1994) 5409.