ELSEVIER

Microelectronics Journal **27** (1996) 623–632

0026-2692/96/$15.00

0026-2692(95)00105-0

Invited paper

Dielectric breakdown II: Related projects at the University of Twente

J.H. Klootwijk[1], J.F. Verweij, J.B. Rem[2] and S. Bijlsma[3]

MESA Research Institute, University of Twente, PO Box 217, 7500 AE Enschede, The Netherlands. Tel: (+31)53-892648. Secr. (+31)53-892644. Fax: (+31)53-341903. [1]E-mail: J.H.Klootwijk@el.utwente.nl. [2]E-mail: J.B.Rem@el.utwente.nl. [3]E-mail: S.Bijlsma@el.utwente.nl

In this paper an overview is given of the related activities in our group of the University of Twente. These are on thin film transistors with the inherent difficulty of making a gate dielectric at low temperature, on thin dielectrics for EEPROM devices with well-known requirements with respect to charge retention and endurance and, finally, on thin film diodes in displays with unexpected breakdown properties. Copyright © 1996 Elsevier Science Ltd.

1. Introduction

In this paper recent results are given obtained in three projects with investigations related to dielectric breakdown. In the first project thin film transistors (TFTs) made in polycrystalline GeSi layers are investigated. They have a gate oxide made at low temperatures. In the second project thin dielectrics for EEPROM devices are being investigated. This is concentrating now on the inter-poly dielectric. In the third project we are addressing the breakdown properties of thin film diodes in flat panel displays.

2. Thin film electronics for integrated sensors

For a wide application of sensors it is advisable to integrate some electronics, i.e. to construct a smart sensor. This results in two main advantages: first, cheaper substrate materials can be used. Secondly, because of the integration, the delicate process of bonding the sensor to the driver electronics is done by lithography instead of using bonding wires. This should result in fewer defects and cheaper production. For some sensors it is possible to integrate the sensor and electronics on one silicon chip, for others this is not possible because of incompatibility in processing or materials (usually, sensors are produced on glass substrates, which cannot withstand temperatures above about 600C). A way out is to make the electronic part in a thin film process using low temperatures [1] and to combine this with the sensor by deposition on any substrate.

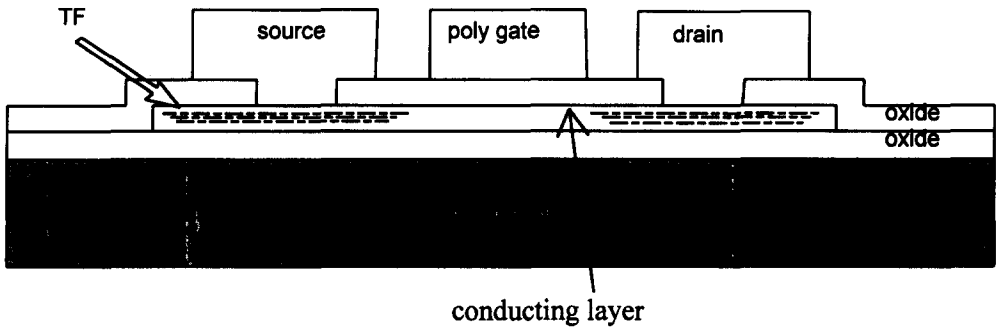

Fig. 1. A schematic view of an implanted thin film transistor. The source and drain regions are implanted into the Ge_xSi_{1-x} thin film using the gate material as an implantation stop.

A consequence of this approach could be to realize the electronic part in polycrystalline-silicon thin film transistors. A disadvantage of poly-Si is the relatively high process temperature, usually 625°C, necessary for deposition. An alternative is amorphous Si, which can be deposited at temperatures as low as 500°C. However, the drive current capability of amorphous Si is too low compared with the requirements for driver electronics. Therefore, we have selected a modification of this technique, namely, to use a silicon-germanium alloy of which we know that the crystallization takes place at a much lower temperature compared with amorphous Si [2]. Another consequence is the use of a low temperature gate oxide. The main goal is to reduce the thermal budget, so production costs can be decreased.

The structure we have selected for our first study is indicated in Fig. 1. We start with a silicon wafer with a thermally grown silicon oxide as a substrate. On top of this the so-called self-aligned TFT is formed. The active thin film of polycrystalline Ge_xSi_{1-x} is deposited and covered by a low pressure chemical vapour deposited (LPCVD) oxide. The gate material, *in situ* phosphorous doped poly-Si, is deposited and patterned, after which the source and drain regions are formed by implantation using the poly-Si gate as an implantation stop. The top gate oxide is an LPCVD oxide deposited at low temperatures (400-500°C), while the bottom gate oxide consists of a thermally grown oxide. This configuration gives the opportunity to evaluate the different oxide qualities using either the top gate or bottom gate.

A first difficulty encountered in this study is the selectivity of Ge [3] and poly-GeSi [4] alloys towards silicon dioxide materials. During the deposition the selectivity reveals itself as an inhibition time during which no apparent deposition occurs. This is unwanted because it would make the growth characteristics dependent on the substrate condition. The first results show that the inhibition time can be reduced by increasing the pressure or by giving a short pressure pulse at the start of the deposition [5].

A next step to be investigated is the (re)crystallization process of the GeSi films and their relation with the final transistor characteristics. It is expected that a large grain size in the thin film is preferable for good device characteristics, because less grain boundary trapping can occur. Two paths can be followed: the first one is the deposition of amorphous Ge_xSi_{1-x} films, which are subsequently crystallized. The second path is the deposition of polycrystalline Ge_xSi_{1-x} films, which can be recrystallized. The deposition of amorphous-GeSi is expected to result in the largest grain sizes while the deposition tempera-

ture is the lowest. A controlled crystallization step will be at a temperature slightly higher than the deposition temperature, thereby fulfilling the demand for lower thermal budget as described above.

A third part of the investigation of poly-GeSi thin film transistors is the development of the low temperature gate oxide. This includes LPCVD [6] and rapid thermal processing chemical vapour deposition (RTCVD) [7] methods. Preliminary results show that the LPCVD oxide can be obtained at a low deposition rate, necessary for reproducible growth of thin layers, with a reasonable thickness uniformity across the wafers. Initial electrical measurements, of which Fig. 2 shows a typical result, reveal that promising resistance to hot electron stress and Fowler-Nordheim tunnelling can be obtained. Still more chemical and electrical characterization of both the poly-GeSi and low temperature gate oxide layers is necessary.

An important part of this research is a study of the TFT stability as an important aspect of its reliability. At the moment the first batches of TFT devices have been processed in our laboratory. A first result of our transistors is given in Fig. 3 which shows a current-voltage characteristic of a TFT with 30 at.% Ge and an oxide

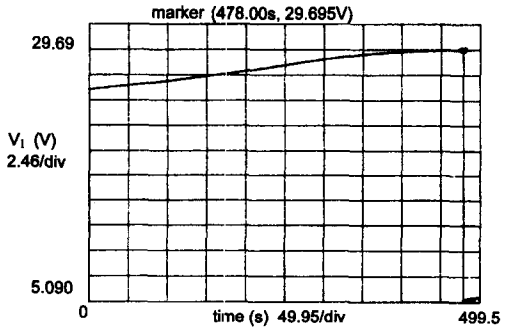

Fig. 2. A typical Q_{BD} result of an LPCVD oxide layer which has been densified at 950°C in N_2 for 10 min. The Q_{BD} value is approximately 0.5 C/cm^2.

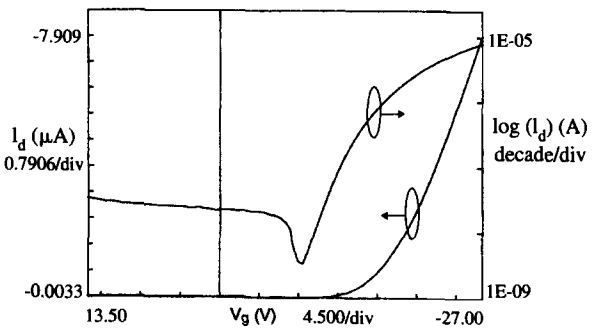

Fig. 3. A typical I_d-V_g characteristic of a 30% Ge TFT, using the bottom gate (thermal oxide) configuration and a V_{sd} of 1 V.

layer grown at 1100C. The LPCVD top gate oxide has been shown not to be sufficient. Of course, further optimization of the process is necessary, and is being investigated.

3. Breakdown in VIPMOS EEPROM devices

In EEPROM development [8] dielectric breakdown has become important. Recent progress in computers requires further efforts in developing higher density and higher reliability non-volatile semiconductor memories. Since the dimensions of devices and the supply voltage are decreasing and the operating speed has to be increased, the reliability of the gate and inter-poly dielectrics/oxides becomes very important. At the University of Twente a new way of programming an EEPROM, by means of hot electron injection, has been developed. This type of non-volatile memory is known as the VIPMOS EEPROM [9, 10]. The acronym VIPMOS stands for vertical injection punch-through based metal oxide semiconductor. The VIPMOS EEPROM has a buried injector, which creates a very efficient source of electrons that are injected into the floating gate. It is possible to have good control over the amount of stored charge. Even analogue values can be stored. A major advantage of this cell is the *in situ* programming, i.e. during programming the cell can be read. This option can be

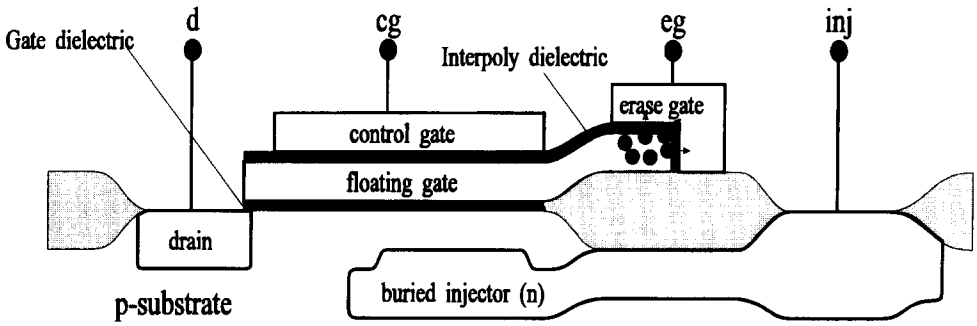

Fig. 4. A cross-section of the VIPMOS EEPROM cell. While applying a high voltage to the erase gate electrons are tunnelling (Fowler-Nordheim) from the floating gate through the inter-poly dielectric to the erase gate. The reliability of the VIPMOS EEPROM depends greatly on this dielectric.

very well used for analogue applications [11, 12] or analogue neural networks [13]. This section concerns the research that is currently performed for optimizing this EEPROM cell.

A typical cross-section of a VIPMOS EEPROM cell is shown in Fig. 4, in which the two important oxides/dielectrics are shown:

1 the gate oxide/dielectric; and

2 the inter-poly dielectric.

An important parameter for EEPROMs is the number of program/erase (P/E) cycles that can be realized before the cell breaks down/is not usable anymore (an endurance plot). An example is shown in Fig. 5. When we analyse this plot, the following aspects are important:

(1) The lifetime of the EEPROM is directly related to the number of P/E cycles. This number of P/E cycles can be extracted from this plot.

(2) Due to charge trapping the threshold voltage window narrows. For digital applications it is only necessary if the two states (i.e. programmed or erased) can be detected. As long as this is the case, the cell can be used. When several bits or even analogue values are stored this threshold voltage window must remain constant as long as possible, since a shift in the threshold voltage can result in a decreasing number of values that can be detected and thus a decreasing bit resolution.

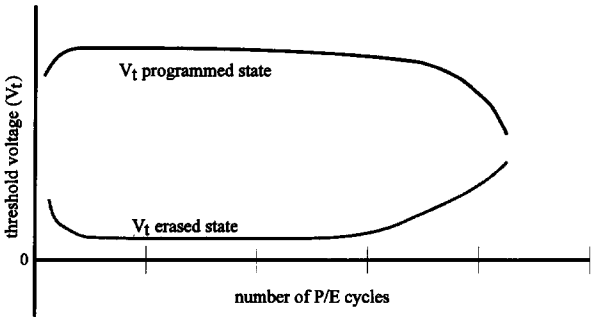

Fig. 5. A typical endurance plot of an EEPROM device. The threshold voltage is measured as a function of the number of program/erase cycles.

During programming the gate dielectric is stressed. By means of applying the necessary voltages a punchthrough condition is created in which electrons become hot and are accelerated towards the floating gate [8, 9]. A part of these electrons gain enough energy to surmount the potential barrier of the gate dielectric. However, a small part of these electrons is trapped in the dielectric which causes undesirable parameter shifts.

During erasure a high voltage is applied to the erase gate. Electrons on the floating gate are then tunnelling through the inter-poly dielectric (Fowler-Nordheim) to the erase gate (Fig. 4), again leaving some electrons behind (due to charge trapping).

The narrowing of the threshold window is mainly caused by two phenomena:

— charge trapping in the gate oxide/dielectric; and
— charge trapping in the inter-poly oxide/dielectric.

Currently research is concented on the inter-poly dielectric, because the quality of this dielectric dominates the behaviour of the VIPMOS EEPROM. It is very complex to realize due to the following conflicting properties:

— good tunnelling capabilities for high applied voltages;
— good insulating properties for low and moderate voltages.

Because it is very expensive and time consuming to realize complete EEPROM devices for dielectric research, other solutions have to be found. Fortunately the inter-poly dielectric can be very well simulated by means of simple capacitor structures, which are used to perform Q_{BD} and *I-V* measurements. An example of a measurement set-up is shown in Fig. 6.

The electrical properties of inter-poly dielectrics are highly influenced by the underlying silicon layer. Dielectrics on mono-Si hardly suffer from surface roughness in contrast to inter-poly dielectrics, which suffer a lot from the surface roughness. Therefore the influence of different deposition parameters on the poly-silicon structure has been investigated [14]. A recipe has been developed to obtain a surface as flat as possible to overcome locally enhanced electron injection and thus local breakdown.

Another way to decrease the influence of the poly-silicon surface is using deposited (LPCVD) dielectrics instead of thermal oxides. When LPCVD dielectrics are deposited on poly-silicon layers with a flat surface, this surface remains flat [13]. During thermal oxidation part of the poly-silicon layer is consumed, resulting in an increasing surface roughness. Although the influence of the surface roughness can be decreased, the electrical properties of deposited dielectrics are not yet as good as thermal oxides.

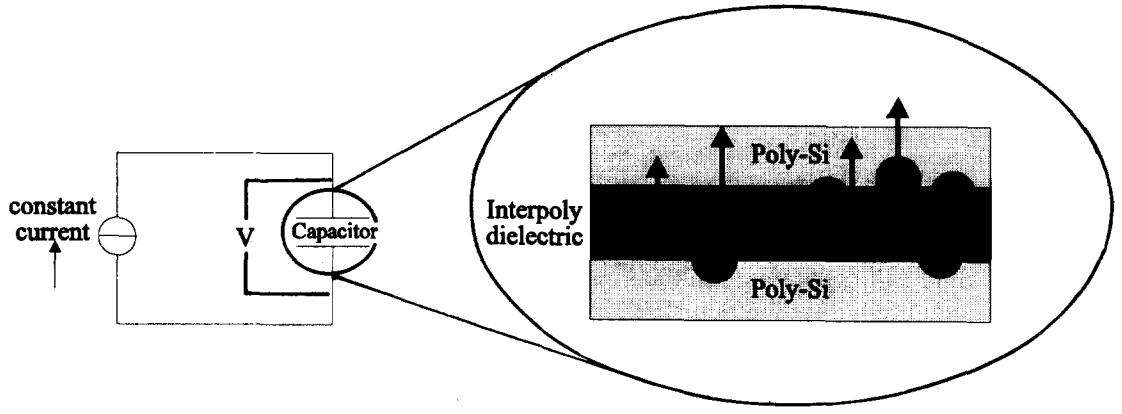

Fig. 6. Typical set-up for Q_{BD} and *I-V* measurements on simple capacitor structures.

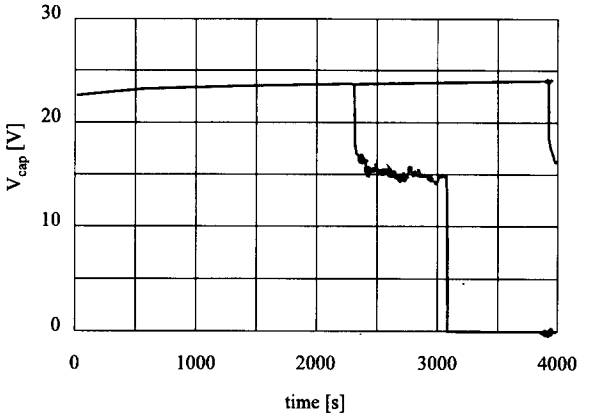

Fig. 7. Typical breakdown behaviour of the inter-poly dielectric at a current stress of 1 mA/cm^2. Two capacitors are stressed at the same time. One capacitor shows breakdown after 2350 s (Q_{BD} = 2.35 C/cm^2) and a complete breakdown after 3050 s. Soft breakdown of the other capacitor occurs after 3950 s (Q_{BD} = 3.95 C/cm^2). The dielectric layer consists of 15 nm LPCVD SiO_2 and 15 nm LPCVD Si_3N_4, both deposited at 800°C.

In the latest VIPMOS EEPROM batches that have been processed in our laboratory this inter-poly dielectric consisted of 15 nm LPCVD SiO_2 and 15 nm LPCVD Si_3N_4, both deposited at 800°C. A result of a Q_{BD} measurement is shown in Fig. 7. The Q_{BD} value (approximately 3 C/cm^2) satisfies the requirements and the voltage increase during the measurement is low (low charge trapping). However, due to the lower barrier height of Si_3N_4 to Si in comparison with the barrier height of SiO_2 to Si the retention (i.e. undesirable loss of electrons) seems to be in doubt. Therefore further research is required.

A special application of this EEPROM cell is the analogue neural network. For analogue data storage the V_T has to be extremely constant (both in programmed and erased state). This means that the charge trapping in the dielectrics has to be as low as possible. For analogue applications not only the lifetime of the dielectrics is important, but also the shift in parameters (V_T) and therefore dielectric breakdown.

4. Breakdown in thin film diodes (TFDs)

Thin film devices are being used in active matrix liquid crystal displays (AMLCD). The devices act as switches for the pixels, which consist of two indium tin oxide (ITO) transparent electrodes. A layer of liquid crystals (LC) is present between the electrodes. The ITO electrodes are present in an array of electrodes in series with switches to form the different pixels. The switches can be implemented using thin film transistors (TFT) or thin film diodes (TFD), resulting in a TFD-R display [15]. Diodes have only two terminals, which means that only two connections for one pixel are needed (TFTs have three terminals). A second advantage of TFDs is the simplicity, they are simple cross-over devices.

TFDs are deposited on one of the glass plates of the display, the active glass plate. The diode consists of amorphous hydrogenated SiN_x sandwiched between a chromium (Cr) and a molybdenum (Mo) electrode. The layout of such a TFD is shown in Fig. 8. The Cr electrode is connected to one of the ITO electrodes of the pixel capacitor. The SiN_x is actually an amorphous silicon layer with nitrogen added in the low temperature PECVD deposition process which increases the bandgap of the semiconductor. This improves the blocking properties of the TFD at low voltages. Hydrogen is added to reduce the number of states in the SiN_x, thus reducing the leakage current. An example of the current-voltage characteristic of a TFD is given in Fig. 9. The device physics and the electronic properties of the TFDs have been described before [16, 17].

In our co-operative project with the Flat Panel Display Co. (FPD) in Eindhoven, we are studying the intrinsic and extrinsic breakdown properties of the TFDs. The bandgap of the SiN_x is about 2 eV, which is somewhere between a semiconductor and a dielectric. One of the first important questions to be answered is: are the

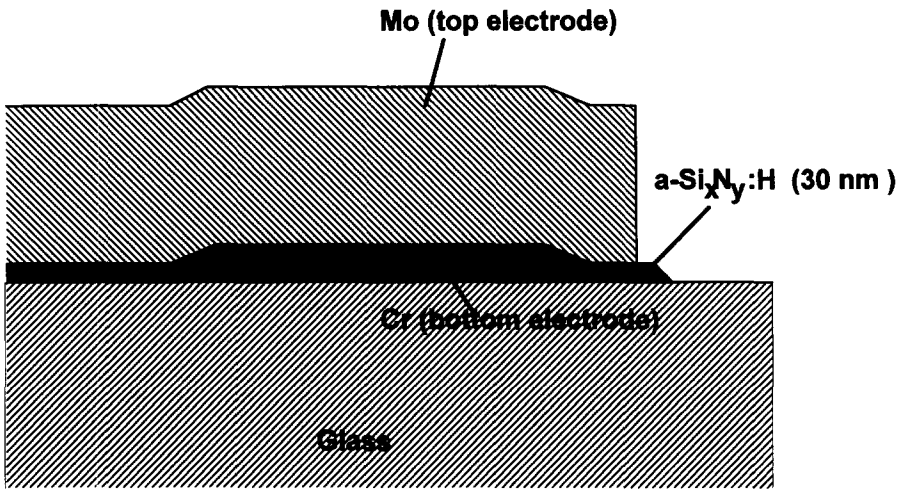

Fig. 8. Layout of a thin film diode.

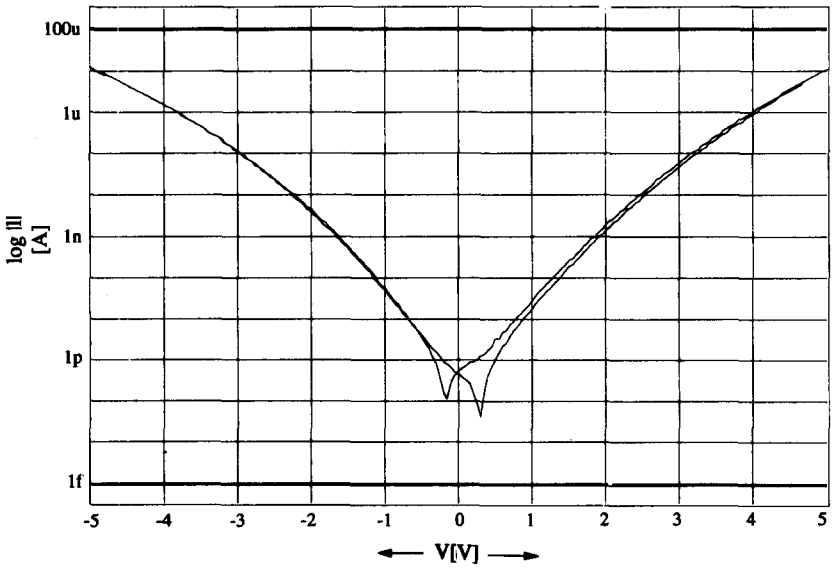

Fig. 9. *IV* characteristics of 100*100 μm^2 TFDs, double sweep.

breakdown characteristics of the TFD similar to that of a dielectric or to that of a semiconductor? The conduction mechanism is controlled by quantum mechanical tunnelling through a reverse biased Schottky barrier [18], which is very similar to that of a dielectric. From that point of view, one would expect a breakdown mechanism that can be related to charge injection, charge-to-breakdown (Q_{BD}) or charge trapping.

The intrinsic breakdown properties under dc conditions were analysed using electrical measurements, three-dimensional thermal

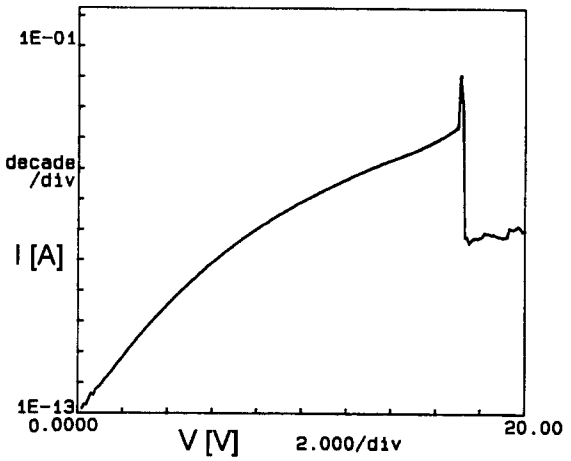

Fig. 10. Breakdown caused by ramp E measurement.

simulations and infrared microscopy to measure the temperature. The electrical measurements that have been carried out were IV, CV, ramp E, ramp I and constant I (Q_{BD}), measurements. Figure 10 shows breakdown due to a ramp E measurement. It was found that the dc breakdown voltage was strongly related to the area of the diode: the smaller area had the higher breakdown voltage. This result and the outcome of failure analysis and the related temperature simulations lead to the conclusion that the dc breakdown is determined by power dissipation, i.e. dc breakdown is a thermal process. Smaller diodes are colder compared with larger diodes, if the same current density is applied. This explains the relation between area and breakdown. Moreover, it should be noted that the concept of charge-to-breakdown is not valid. If a current below the dissipation limit is applied it seems to be able to flow infinitely while a current just above the dissipation limit will blow the diode immediately. Based on the results obtained so far we conclude that breakdown in the TFD is much more related to that in a semiconductor than to that in a dielectric. It was also found that the temperature at which breakdown occurs can be related to the diffusion of the hydrogen in the SiN_x. Infrared video recordings showed clearly gaseous emission of material coming from the SiN_x. Because the breakdown temperature was found to be a few hundred degrees, only the hydrogen in the SiN_x can be held responsible for the gaseous emission.

The intrinsic breakdown properties due to very fast signals (pulses of 50 ns to 500 ns) were analysed using a transmission line measurement (TLM), which is normally used for the characterization of electrostatic discharge (ESD) behaviour of integrated circuits. A strong asymmetry in breakdown behaviour was found, although the IV characteristics are almost symmetric. This can probably be related to the difference of the interfaces Cr-SiN_x and Mo-SiN_x. The intrinsic breakdown properties due to signals on an intermediate time scale (pulses 1 ms to 1 ms) were analysed using a dedicated measurement set-up. A smooth transition from dc breakdown properties to very fast breakdown was found.

The extrinsic breakdown characteristics of the TFDs were measured on specific test structures with different active areas and width/length ratios of the TFDs. The test structures and a statistical measurement should enable us to obtain statistical reliability monitoring of the active plate process. It is obvious that this is very important, because the large area of the AMLCDs enhances failure risk significantly. In Fig. 11, a plot from the statistical measurement is shown, which shows the breakdown voltage measured on 3360 samples (area 4100 μm^2) with the aid of the ramp voltage/field (ramp E) technique described before. In Fig. 4 we see two regions in the statistical breakdown plot: one narrow distribution at about 9.2 V indicative of intrinsic breakdown and a wide distribution of breakdowns below 9.2 V indicative of defect-related breakdown. Measurement results on test structures made in the standard process are presented in Fig. 12, from which we see that defects are virtually absent. We thus conclude that the above described breakdown measurement presents a useful technique for studying

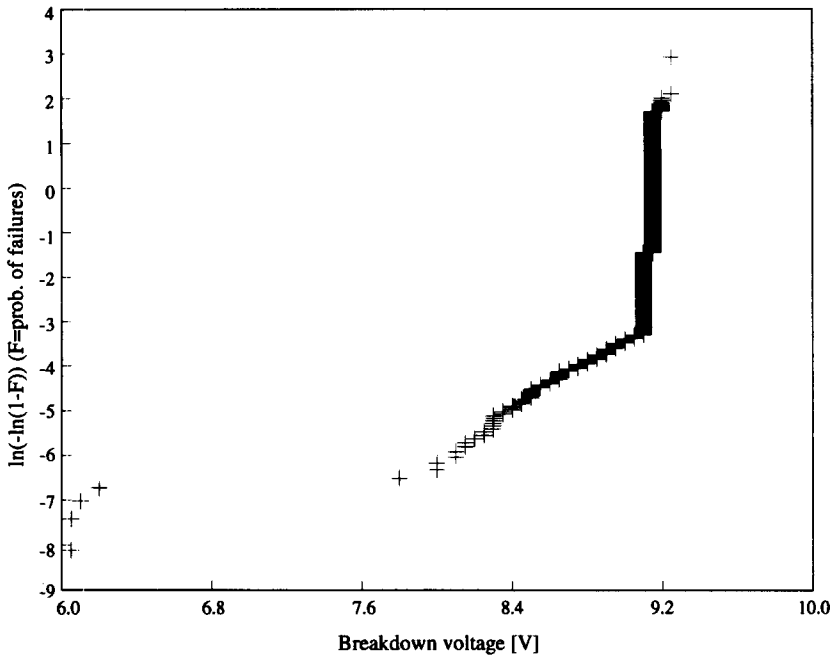

Fig. 11. Cumulative failures, 4*100 μm^2 TFDs, defect sensitive process.

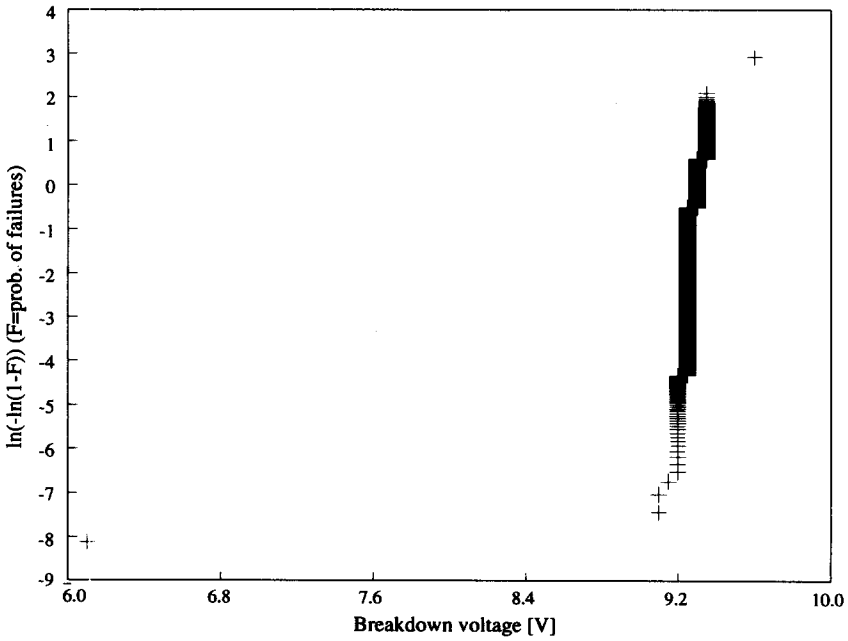

Fig. 12. Cumulative failures, 4*100 μm^2 TFDs, standard process.

and minimizing the defect-related failure probability in the manufacturing of a-SiN TFDs.

Acknowledgements

The second author (J.F. Verweij) thanks the organizers of the 6th ESPRIT Workshop on Growth and Characterization of Thin Dielectrics for Microelectronics for the invitation to present an invited talk at this conference. The contents of this presentation form the basis of this paper. Moreover, the authors thank the eight referees of this paper for valuable comments which greatly contribute to the final contents of the paper. The support of the Foundation for Fundamental Research on Matter and the Netherlands Technology Foundation is gratefully acknowledged. Finally, the careful typing of the manuscript was carried out by Mrs. Margie Rhemrev.

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