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Multi-silicon ridge nanofabrication by repeated edge lithography

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Abstract

We present a multi-Si nanoridge fabrication scheme and its application in nanoimprint lithography (NIL). Triple Si nanoridges approximately 120 nm high and 40 nm wide separated by 40 nm spacing are fabricated and successfully applied as a stamp in nanoimprint lithography. The fabrication scheme, using a full-wet etching procedure in combination with repeated edge lithography, consists of hot H₃PO₄ acid SiNx retraction etching, 20% KOH Si etching, 50% HF SiNx retraction etching and LOCAl Oxidation of Silicon (LOCOS). Si nanoridges with smooth vertical sidewalls are fabricated by using Si ⟨110⟩ substrates and KOH etching. The presented technology utilizes a conventional photolithography technique, and the fabrication of multi-Si nanoridges on a full wafer scale has been demonstrated.

1. Introduction

Beam writing techniques, such as electron beam lithography (EBL) and focused ion beam lithography (FIB), have become the conventional and standard means of nanofabrication. To reduce the high cost and low throughput of nanofabrication using beam writing techniques, the fabrication of nano-structures employing unconventional methods has been an attractive research topic in nanotechnology [1]. Researchers have explored the possibilities of integration of micro-machining technologies, for example conventional photolithography, chemical vapor deposition of materials and micro-machining etching methods, into nanofabrication. Amongst all the unconventional methods, edge lithography is widely used and has proven to be a competent means of nanofabrication in combination with micro-machining technologies [2]. In edge lithography, the edges of the original pattern become the features of the final pattern.

Developed in a similar way to edge lithography, the spacer patterning technique (SPT) generally comprises: (1) sacrificial structures with vertical sidewalls patterned by photolithography and directional etching; (2) conformal deposition of another layer; (3) maskless directional etching of this layer; and (4) final selective etching of the sacrificial layer [3]. Several publications have demonstrated the fabrication of spacer-like structures employing similar working principles to SPT. Choi et al demonstrated the fabrication of nanoscale phosphosilicate glass (PSG) complementary metal oxide semiconductor (CMOS) by conformal deposition of PSG over an SiGe block pattern defined by photolithography, reactive ion etching of this PSG and removal of the SiGe sacrificial pattern [4]. Degroote used a SPT in combination with resist based patterning to define a Si-fin with a critical dimension below 20 nm [5]. Based on SPT, multi-SPT was developed by repeating a series of conformal deposition and anisotropic etching steps; it was shown to have potential in nanoelectronics applications [6, 7].

The multi-spacer patterns can also be created by a so-called planar edge defined alternate layer (PEDAL) process [8, 9]. The PEDAL process consists of: (1) fabrication of trench-like structures with vertical sidewalls; (2) alternating deposition of materials upon the trench-like structure, e.g. silicon nitride and polysilicon; (3) substrate planarization by a spin-coated polymer; (4) etch-back of the polymer, silicon nitride and polysilicon by RIE etching; and finally (5) selective polysilicon etching to obtain spacers made of silicon nitride. Hussain et al employed a similar process flow to fabricate a template with Si nanowires for nanoimprint applications [10].
Generally, the critical dimensions of the spacers fabricated by either SPT or PEDAL are defined by the conformal layer deposition. The initial pattern with vertical sidewalls determines the verticality of the spacers. Both smoothness of the initial pattern sidewalls and selective dry etching influence the smoothness and the shape of the spacer sidewalls. In a previous publication, we introduced a related but different technique—the fabrication of monocrystalline Si nanoridges by using a full-wet etch procedure including local oxidation of silicon (LOCOS) and an adapted edge lithography technique on top of conventional photolithography [2]. Here, we present the fabrication of multi-monocrystalline Si nanoridges using repeated edge lithography, which consists of sequentially performed SiNₓ retraction etching in hot H₃PO₄ acid, Si etching in KOH, SiNₓ retraction etching in 50% HF and LOCOS.

2. Fabrication

The fabrication scheme for multi-Si nanoridges is shown in figure 1: (A) 100 mm, double side polished, p-type Si (110) substrates are used. The substrate is prepared with 200 nm low pressure vapor deposition (LPCVD) silicon-rich nitride (SiNₓ) and 50 nm LPCVD tetraethyloxydisilicate (TEOS) annealed in a furnace with a N₂ atmosphere at 1050 °C for 1 h. (B) The substrate is patterned by conventional photolithography using a resist mask (Olin 907-12) containing 4 µm gratings covering the whole wafer surface. The substrate is treated in UV/ozone for 300 s to increase the hydrophilicity of the photoresist to improve TEOS wet etching. Then the TEOS is patterned by buffered HF (NH₄F:HF = 1:7) for 45 s. Since the SiNₓ surface shows hydrophilic behavior, like TEOS, about 10% over-etch is performed here to ensure complete pattern transfer. A dummy wafer with only a TEOS layer is used to test the etch rate. The completion of etching can be observed when the wafer surface turns from hydrophilic to hydrophobic. The etch rate of TEOS annealed at 1050 °C in buffered HF is approximately 80 nm min⁻¹. (C) After stripping the photoresist in 100% HNO₃ for 20 min, the SiNₓ is patterned in 85% H₃PO₄ heated up to 180 °C (referred to as hot H₃PO₄ acid in the remainder of the paper) using a resist mask (Olin 907-12) containing 4 µm gratings covering the whole wafer surface. The substrate is treated in UV/ozone for 300 s to increase the hydrophilicity of the photoresist to improve TEOS wet etching. Then the TEOS is patterned by buffered HF (NH₄F:HF = 1:7) for 45 s. Since the SiNₓ surface shows hydrophilic behavior, like TEOS, about 10% over-etch is performed here to ensure complete pattern transfer. A dummy wafer with only a TEOS layer is used to test the etch rate. The completion of etching can be observed when the wafer surface turns from hydrophilic to hydrophobic. The etch rate of TEOS annealed at 1050 °C in buffered HF is approximately 80 nm min⁻¹. (C) After stripping the photoresist in 100% HNO₃ for 20 min, the SiNₓ is patterned in 85% H₃PO₄ heated up to 180 °C (referred to as hot H₃PO₄ acid in the remainder of the paper) using TEOS as the mask for 55 min. The completion of etching can be observed when water runs along the patterned surface, since
the Si surface shows hydrophobic characteristics. The etch rate of 1050 °C annealed SiNₓ and TEOS in hot H₃PO₄ acid is 3.9 nm min⁻¹ and 0.29 nm min⁻¹, respectively [11]. The SiNₓ etching is carried out with about 10% over-etch to ensure complete pattern transfer. (D) Before Si etching, TEOS is stripped in 1% HF for 20 min. Anisotropic Si etching is performed in 20% KOH used at room temperature (referred to as 20% KOH in the remainder of the paper) for 5 min and followed by RCA-2 cleaning (a mixture of HCl:H₂O₂:H₂O of 5:1:1 at 80 °C) for 10–15 min to remove contaminants harmful to the oxidation furnace in step F. The etch rate of Si (110) in 20% KOH solution is 25 nm min⁻¹. (E) Then SiNₓ retraction etching is carried out in 50% HF for 25 min to obtain an opening on the Si surface. The etch rate of SiNₓ in 50% HF dropped from 2.7 nm min⁻¹ before annealing to 1.7 nm min⁻¹ after annealing at 1050 °C. (F) Subsequently the exposed Si part is dry oxidized at 950 °C for 15 min using SiNₓ as the mask (the so-called LOCOS process). (G) SiNₓ retraction etching is performed in hot H₃PO₄ acid for 8 min to make an opening in the Si surface. (H) Si etching in 20% KOH for 10 min. Figures 2–6 show the fabrication results in accordance with steps (D)–(H).

This edge lithography scheme, which consists of hot H₃PO₄ acid SiNₓ retraction etching (G, K), 20% KOH Si etching (D, H, L), 50% HF SiNₓ retraction etching (E, I, M) and LOCOS (F, J, N), is repeated to fabricate multi-Si nanoridges. By iterating the repeated edge lithography steps results in the second fabricated Si nanoridge illustrated in figures 7 and 8. By terminating the fabrication scheme, for example after step (F), (J) or (N), single, double or triple Si nanoridges can be obtained by complete removal of SiNₓ in hot H₃PO₄ acid, Si etching in 20% KOH and then complete removal of SiO₂ in 50% HF. Stopped at step (N), figures 9 and 10 show examples of triple Si nanoridges by complete removal of SiNₓ in hot H₃PO₄ acid, Si etching in 20% KOH for 5 min and complete SiO₂ removal in 50% HF.
Figure 6. SEM image showing the result after step (H) of figure 1: the first Si ridge is finished by anisotropic etching of Si in 20% KOH for 10 min.

Figure 7. Continuation of Si nanoridge fabrication after figure 6 by repeating 50% HF SiN retraction etching for 25 min, LOCOS at 950°C for 15 min, hot H3PO4 acid SiN retraction etching for 8 min and 20% KOH Si etching for 10 min.

Figure 8. Magnification of figure 7 showing the non-uniform LOCOS inside the narrow trench.

Figure 9. SEM image of triple Si nanoridges after complete removal of SiN, 20% KOH etching and final removal of SiO2 in 50% HF.

3. Discussion

3.1. Substrate preparation and layer patterning

To illustrate the feasibility of the multi-Si nanoridge fabrication scheme, we chose to deposit 200 nm SiN, and then 50 nm TEOS. The 1050°C annealing step is introduced to increase the etch selectivity of SiN to TEOS in hot H3PO4 acid from 1.4 (4.2 to 2.9 nm min⁻¹) to 15 (3.9 to 0.29 nm min⁻¹) [11]. Therefore, 50 nm TEOS is sufficient for pattern transfer into 200 nm SiN in 52 min. Normally 10% over-etch is performed to ensure complete etching. As shown in figure 2, SiN displays an isotropically etched profile after etching in hot H3PO4 acid using TEOS as the mask.

3.2. Si etching in 20% KOH at room temperature (step D, H, L)

In figure 2, the vertical smooth Si sidewalls are achieved by 20% KOH etching of Si ⟨110⟩ substrate, which automatically stops etching at Si ⟨111⟩ planes. For the purpose of this fabrication scheme, 20% KOH is used instead of other standard wet chemicals for Si etching, which include OPD 4262, 5% tetramethylammonium hydroxide (TMAH) used at 70°C and 25% KOH used at 75°C. Table 1 lists the etch rates of ⟨110⟩ Si and selectivities between Si ⟨111⟩ and Si ⟨110⟩ planes in these wet chemicals. The etch rates of Si ⟨110⟩ in 5% TMAH used at 70°C and 25% KOH used at 75°C are too fast to be useful. Although the slow etch rate of OPD 4262 is favorable, the etch selectivity between the Si ⟨111⟩ and ⟨110⟩ planes makes the etching of Si ⟨111⟩ planes non-negligible while making Si nanoridges 100–200 nm deep and a few tens of nanometers wide. Therefore the use of OPD 4262 in this scheme can lead to reduced control of the lateral dimensions of multi-Si
Table 1. Etch rates of Si (110) planes and selectivity between Si (110) and (111) planes in different etch solutions.

<table>
<thead>
<tr>
<th>Etch Solution</th>
<th>Etch Rate (nm min$^{-1}$)</th>
<th>Selectivity (111):(110)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPD 4262 @ 20°C</td>
<td>3.5</td>
<td>1:5</td>
</tr>
<tr>
<td>5% TMAH @ 70°C</td>
<td>750</td>
<td>1:100</td>
</tr>
<tr>
<td>20% KOH @ 20°C</td>
<td>25</td>
<td>1:400 [12]</td>
</tr>
<tr>
<td>25% KOH @ 75°C</td>
<td>1800</td>
<td>1:400</td>
</tr>
</tbody>
</table>

Figure 10. SEM image of an overview of groups of triple Si nanoridges. nanoridges, and consequently making the control of spacing dimension more difficult. Therefore, 20% KOH is selected, considering the relatively low etch rate on Si (110) planes and high selectivity between Si (111) and (110) planes [12]. Moreover, the effect of line edge roughness brought by the use of conventional photolithography is avoided by self-alignment to Si (111) planes in KOH etching [13].

To obtain a relatively even level of the Si surface surrounding the Si nanoridges, the first KOH etching shown in figure 2 is executed for 5 min while the following 20% KOH Si etching shown in figures 6 and 7 is performed for 10 min. It is estimated that the large difference in the trench aspect ratio is the reason for the difference in etching time. In figures 6 and 7, the trench aspect ratio (depth to width) is approximately 3:1 (120 nm:40 nm), while the trench aspect ratio is about 0.03:1 (120 nm:4000 nm) in figure 2. In this specific case, to obtain an even trench depth, etching the nano-sized opening takes roughly twice as long as the time needed for the 4 μm opening. This effect can be called KOH lag and closely resembles RIE lag [14]. At present, we assume the reason behind the KOH lag is the depletion of active species into deep and narrow trenches.

3.3. SiNx retraction etching using a 50% HF (step E, I, M)

After Si patterning in 20% KOH and RCA-2 cleaning, SiNx is etched in both lateral and vertical directions using 50% HF for 25 min to receive an approximately 40 nm opening on the Si surface, as shown in figure 3. As the Si edge is exposed to the etchant, 50% HF is used instead of hot H$_3$PO$_4$ to avoid Si surface attack [2].

3.4. LOCOS (step F, J, N)

The LOCOS step is executed to form a thermal SiO$_2$ layer on the fabricated Si edges to protect them from being deteriorated in the following hot H$_3$PO$_4$ acid SiN$_x$ retraction etching and 20% KOH Si etching steps. Except for the purpose of serving as the protective layer, this SiO$_2$ layer influences the dimensions of the fabricated Si ridges and spacing between them. Since Si is consumed during oxidation, the LOCOS step leads to shrinkage in Si nanoridge height and width and widening of the spacing. Therefore we tried decreasing the oxidation time to minimize the influence of LOCOS. A thickness of 2 nm SiO$_2$ proved to be sufficient to withstand 20% KOH etching Si (110) for 400 nm at room temperature [12]. Figure 11 shows a Si ridge with a cleavage at the side. In this case, the protective SiO$_2$ was obtained by 5 min LOCOS (about 10 nm SiO$_2$ obtained), which proved to be insufficient due to the non-uniform SiO$_2$ thickness at shaped Si surfaces as discussed by Marcus et al [15]. The drawings shown in figure 12 illustrate the shaped Si surface after LOCOS for 5 min followed by etching in hot H$_3$PO$_4$ acid for 15 min [16]. Since the SiO$_2$ at the top corner is thinner, it can first be etched away during SiN$_x$ retraction etching in hot H$_3$PO$_4$ acid. The cleavage is then made during the next 20% KOH Si etching step as a result of opening at the protective SiO$_2$ layer. It is reported that the non-uniform SiO$_2$ thickness can be suppressed by: (1) increasing the oxidation temperature, (2) adding NH$_3$ gas during dry oxidation; or (3) decreasing the oxidation rate by inert gas addition [15, 17, 18]. All of these solutions are based on the fact that the oxide stress is reduced by viscous relaxation. Concerning this multi-Si nanoridge fabrication scheme, the LOCOS temperature cannot
go beyond 1100 °C so as to keep the intrinsic characteristics of SiNₓ [19]. Besides improving the uniformity of oxide growth, the selectivity between the SiNₓ and SiO₂ layers might be increased as found by Vos [20]. The improvement of the SiO₂ growth or SiNₓ selectivity needs further investigation but this is beyond the scope of this paper.

The result of LOCOS inside a narrow trench after dry oxidation can be observed in figure 8 with the help of the illustration in figure 12. Clearly, the thickness of the grown oxide layer depends on the position along the wall. At the convex and concave corners it is less than on the other positions as observed by Marcus [15]. Moreover, the thickness depends on the orientation of the underlying silicon surface [21]. Depletion of the oxidizing agent seems to be unlikely because both the narrow (40 nm) as well as the wide open trenches (4 μm) have an almost identical oxide layer at their surface. Further research is needed to fully understand the oxidation behavior in narrow high aspect ratio trenches.

3.5. SiNₓ retraction etching using hot H₃PO₄ acid (steps G, K)

After LOCOS, hot H₃PO₄ acid is used for SiNₓ retraction etching taking advantage of the selectivity between SiNₓ and SiO₂ (3.9 to 0.25 nm min⁻¹). An opening of 20 nm on the Si surface is obtained by etching SiNₓ in hot H₃PO₄ acid for 8 min, as shown in figure 5. Because the SiNₓ etch rate is 3.9 nm min⁻¹, we should have observed 31 nm of retraction. However, SiNₓ is partly oxidized during the LOCOS [22]. Due to this oxide, we have a delay of approximately 2 min before SiNₓ starts etching. Finally, we find that the etching of SiNₓ in hot H₃PO₄ acid plays an important role in influencing the uniformity of etching over the whole wafer. Therefore, a stirrer is used to maintain a uniform temperature within the heated acid.

3.6. The determination of multi-Si nanoridge dimensions

As can be concluded from the previous discussions, the height of the Si nanoridges is predominantly determined by 20% KOH Si etching while the width of each Si nanoridge and the opening between the Si nanoridges are largely determined by 50% HF SiNₓ retraction etching and hot H₃PO₄ acid SiNₓ retraction etching, respectively. Moreover, the LOCOS step influences the dimensions of the multi-Si nanoridges by reducing the width and height of the Si nanoridges and consequently widening the spacing between them. In other words, the width and height of the fabricated Si nanoridges are decreased in the subsequent fabrication steps due to the consumption of Si in LOCOS. Also the proposed multi-Si ridge nanofabrication scheme is performed with uniform results on a full 100 mm wafer scale. By knowing these factors, each Si nanoridge and spacing can be tuned according to specific requirements after calculation and careful experimental handling. Furthermore, the Si substrate is prepared with 200 nm SiNₓ and 50 nm TEOS to show the feasibility of our fabrication scheme. The substrate can be prepared with different SiNₓ layer thicknesses considering the dimensions and number of Si nanoridges required. Accordingly, the TEOS layer thickness can also be tuned as needed. Since the multi-Si nanoridge process steps can be well controlled, we assume that the fabrication of Si nanoridges down to 10 nm is attainable, as we have already demonstrated the successful wafer-scale fabrication of single Si nanoridges down to 10 nm by edge lithography in our previous publication [2].

4. Application in nanoimprint lithography

The fabricated triple Si nanoridge sample, as shown in figures 9 and 10, is used in thermal nanoimprinting [23]. Before imprinting, the wafer template is cleaned in Piranha (H₂SO₄; H₂O₂ = 3:1, around 100 °C) for 30 min, rinsed with deionized (DI) water and blown dry with N₂. Then, a monolayer of 1H,1H,2H,2H-perfluorodecyltrichlorosilane is deposited from the gas phase under vacuum condition in a desiccator. This layer acts as the anti-adhesion layer on the mold to facilitate demolding. The imprint process is performed on a wafer coated with PMMA (MW 38 kDa, 4 wt% as to receive 200 nm layer thickness at 3000 rpm spin rate) using an Obducat thermal nanoimprint machine. The imprint is carried out at 180 °C and 40 bar for 10 min and the demold temperature is 90 °C. The imprint result is shown in figure 13. We observed polymer filling problems inside Si narrow trenches of the imprint sample, as can be seen in the image. We did not try to solve the problem since polymer filling is a typical issue in thermal nanoimprinting and goes beyond the focus of this paper.

5. Conclusions

A multi-Si ridge nanofabrication scheme has been successfully used in producing multi-Si nanoridges. The use of 20% KOH and a Si (110) substrate promises to obtain smooth and vertical
Si sidewalls, which automatically stops at the Si (111) planes. Different from spacer patterning technology, the incorporation of LOCOS improves the dimension and shape of the silicon ridges. Without relying on the resolution on beam writing technologies, the width of an individual Si nanoridge and spacing can be well controlled by SiN$_x$ retraction etching in 50% HF and hot H$_2$PO$_4$ acid, respectively. We have demonstrated ridges 120 nm high, 40 nm wide and 40 nm apart but are confident of reaching sub-10 nm resolution without complicating the process scheme. We can fabricate these multi-Si nanoridges with uniform dimensions within the 100 nm wafer scale by using photolithography and the full-wet etching scheme. Multi-Si nanoridges with specific dimensions can be produced by modifying the fabrication parameters as required, such as the layer thickness of SiN$_x$ and TEOS, etching time of SiN$_x$ and Si and oxidation time.

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References