Analysis of the Subthreshold Current of Pocket or Halo-Implanted nMOSFETs

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***Abstract*—In this work, we analyzed the subthreshold current (I_D) of pocket implanted MOSFETs using extensive device simulations and experimental data. We present an analytical model for the subthreshold current applicable for any type of FET and show that the subthreshold current of nMOSFETs, which is mainly due to diffusion, is determined by the internal two-dimensional hole distribution across the device. This hole distribution is affected by the electric potential of the gate and the doping concentration in the channel. The results obtained allow accurate modelling of the subthreshold current of future generation MOS devices.**

***Index Terms*—Complementary MOSFETs (CMOSFETs), current, MOS devices, semiconductor device modeling, simulation.**

I. Introduction

POCKET or halo implants in CMOS technology were originally used to reduce short-channel effects in downscaled bulk devices [1], [2]. Huge research effort is presently undertaken to improve pocket-implanted MOSFETs with respect to source–drain resistances, junction capacitances, threshold voltage rolloff, and off-current [3]–[5]. In particular, the off-current is largely affected by the subthreshold current (I_D).

In the subthreshold regime, the nMOSFET is in weak inversion or diffusion mode, in which the electrons have to cross a potential barrier in the silicon channel region. For a pocket-implanted MOSFET, there can, in fact, be two barriers especially in a long channel, as shown in Fig. 1. Hence, conventional formulas for I_D in uniformly doped MOSFETs [6]–[8] are not applicable here.

In [9], it was stated that the surface-potential variation in the channel of pocket-implanted devices is important, which partly explains the physics behind the subthreshold current.

In [10], an analytical model for I_D of pocket-implanted devices was proposed based on the surface-potential variation. In this model, the subthreshold current depends on the doping concentration of the pocket implants only, but it includes the integral of the exponent of the surface potential along the channel region. However, it does not give the correct picture for long-channel pocket-implanted devices ($> 2\ \mu$m) and for the situation when the pocket implants from the source-side and drain side overlap each other in the middle of the channel region (short-channel devices).

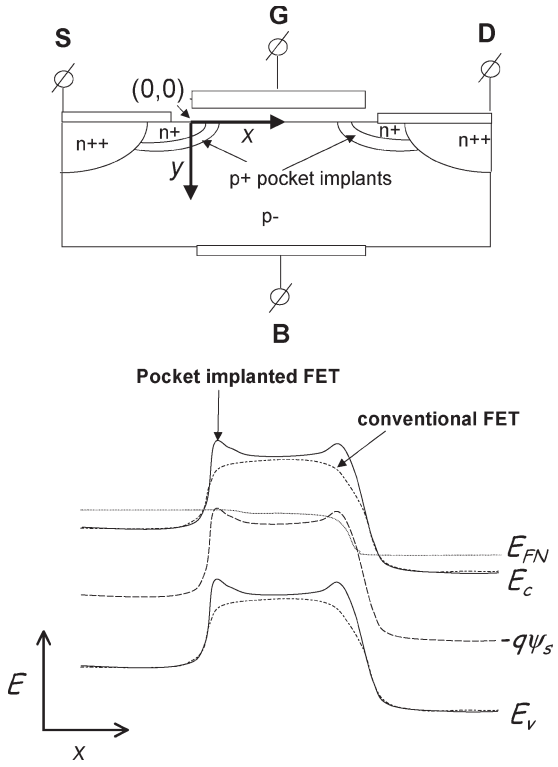

Fig. 1. Schematic cross section of an nMOSFET with a p+ pocket-implanted channel region (top) and schematic diagram in the channel region (bottom). Note the potential barriers caused by the pocket implants that also affect the surface potential ψ_s.

A more physically based analytical surface-potential model for pocket-implanted devices, which is applicable for the whole range of channel lengths, was proposed in [11]. However, in [12], Pang and Brews proposed an approximated subthreshold current model determined by an "effective" channel length that was used as a fit parameter and the minimal surface potential in the channel region. This subthreshold current model, for which the derivation was not clarified in the text, was claimed to be applicable for the situation when the pocket implants do not overlap.

In summary, it seems that the physics describing I_D in pocket-implanted MOSFETs is not well understood. Therefore, in this paper, we analyzed the I_D of these devices. In Section II, we describe the theory of I_D and present a new analytical model that forms the basis of a new compact model. We show that the subthreshold current of nMOSFETs is determined by the internal two-dimensional (2-D) hole distribution across the device, which is affected by the gate bias. In Section III,

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we use device simulation and experimental data for showing the validity of the theory described in Section II. Finally, in Section IV, we come up with conclusions.

II. Basic Theory

For the derivation of the subthreshold current model, we have the following assumptions.

1) Boltzmann's approximation is applicable.
2) There is no current flow through the gate dielectric and no recombination in the channel region, which yields a constant channel current.
3) The hole Fermi potential $\varphi_{\rm FP}$ is constant in the channel region.
4) There is no interface charge.
5) There is no quantum confinement.

For convenience, we assume no vertical current flow [assumption 2)], and therefore, we can define the electron current density as

$$J_n(x,y) = -q \cdot n(x,y)\mu_n(x,y)\frac{d\varphi_{\rm FN}(x)}{dx} \tag{1}$$

where q, n, μ_n, and $\varphi_{\rm FN}$ are the elementary charge, the electron concentration, the mobility, and the electron Fermi potential, respectively. The lateral and perpendicular distances with respect to the gate dielectric are denoted by x and y, respectively. The coordinate $(x,y) = (0,0)$ corresponds with the position below the gate edge at the source-side inside the silicon (Fig. 1).

Integrating all current density paths described by (1) inside the silicon perpendicular to the gate dielectric (y-direction), it can be stated that

$$\begin{aligned} I(x) &= \int_0^{t_{\rm Si}} J_n(x,y)dy \\ &= -q\frac{d\varphi_{\rm FN}(x)}{dx}\int_0^{t_{\rm Si}} n(x,y)\mu_n(x,y)dy \end{aligned} \tag{2}$$

where I is the electron current per-unit width and $t_{\rm Si}$ is the (p-type) silicon layer thickness underneath the gate.

Next, applying assumption 1) for the electron concentration, n can be expressed as

$$n(x,y) = \frac{n_{\rm ie}^2(x,y)}{p(x,y)} \cdot \exp\left(\frac{\varphi_{\rm FP} - \varphi_{\rm FN}(x)}{u_T}\right) \tag{3}$$

where $n_{\rm ie}$ is the actual intrinsic carrier concentration, which may include bandgap narrowing effects due to heavy doping or material (composition) variation, $u_T = kT/q$ (thermal voltage), and $\varphi_{\rm FP}$ is the hole Fermi potential, which is assumed to be constant [assumption 3)]. Because of the use of pocket implantations, the hole concentration and consequently the electron concentration depends on the x-coordinate.

Then, substituting (3) in (2) yields

$$\begin{aligned} I(x) &= \int_0^{t_{\rm Si}} J_n(x,y)dy \\ &= -q\frac{d\varphi_{\rm FN}(x)}{dx}\int_0^{t_{\rm Si}} \mu_n(x,y)\frac{n_{\rm ie}^2(x,y)}{p(x,y)} \\ &\quad \cdot \exp\left(\frac{\varphi_{\rm FP} - \varphi_{\rm FN}(x)}{u_T}\right)dy \end{aligned}$$

and hence

$$\begin{aligned} I(x) \cdot \left(\int_0^{t_{\rm Si}} \mu_n(x,y)\frac{n_{\rm ie}^2(x,y)}{p(x,y)}dy\right)^{-1} \\ = -q \cdot \exp\left(\frac{\varphi_{\rm FP} - \varphi_{\rm FN}(x)}{u_T}\right)\frac{d\varphi_{\rm FN}(x)}{dx}. \end{aligned} \tag{4}$$

Using assumption 2), i.e., $I(x) = I$, and integrating (4) as a function of x yields

$$\begin{aligned} I \cdot \int_0^L \left(\int_0^{t_{\rm Si}} \mu_n(x,y)\frac{n_{\rm ie}^2(x,y)}{p(x,y)}dy\right)^{-1} dx \\ = -q \cdot \int_{\varphi_{\rm FN,S}}^{\varphi_{\rm FN,D}} \exp\left(\frac{\varphi_{\rm FP} - \varphi_{\rm FN}(x)}{u_T}\right)d\varphi_{\rm FN} \end{aligned} \tag{5}$$

where L is the total device length and $\varphi_{{\rm FN},S}$ and $\varphi_{{\rm FN},D}$ are the electron quasi-Fermi potential at the source and drain, respectively. For L, the device length can be taken starting in the source diffusion and running into the drain diffusion. The reason for this is that the contribution to the integral of the values within the source and drain regions is negligible. This is induced by the direct link of the hole concentration with the subthreshold current (5).

Furthermore, the Einstein relation holds for minority transport [assumption 1)], and is expressed as

$$\frac{D_n}{\mu_n} = \frac{kT}{q} \tag{6}$$

where D_n is the diffusion coefficient.

By performing the integration at the right-hand side of (5) and using (6), the diffusion current per-unit width can be expressed as

$$I_D = -\frac{q \cdot n_{\rm io}^2}{G_{\rm CH}} \cdot \left(1 - \exp\left(-\frac{V_{\rm DS}}{u_T}\right)\right) \tag{7a}$$

where $n_{\rm io}$ is the intrinsic carrier concentration of pure silicon and

$$G_{\rm CH} = \int_0^L \left(\int_0^{t_{\rm Si}} \left(\frac{n_{\rm ie}(x,y)}{n_{\rm io}}\right)^2 \left(\frac{D_n(x,y)}{p(x,y)}\right)dy\right)^{-1} dx. \tag{7b}$$

Hence, the 2-D hole distribution $p(x, y)$ determines the subthreshold current. Equations (7a) and (7b) apply for any type of FET, including double-gate devices. However, the equations for $p(x, y)$ and the potential $\psi(x, y)$ depend on the type of FET.

The hole concentration for our devices can be expressed as

$$p(x,y) = N_A(x,y) \cdot \exp\left(-\frac{\psi(x,y)}{u_T}\right) \tag{8}$$

implying that the hole concentration depends on the electrostatic potential and the doping concentration.

For very short channel devices, the subthreshold current is limited by the electron saturation velocity in the drain depletion layer. This implies that there is a limit in the drain–current despite of a continuous reduction of the hole concentration in parameter $G_{\rm CH}$ in (7b). For this situation, D_n depends on the lateral electric field. In the devices presented here, this velocity saturation effect in the subthreshold current is not important, as discussed further in Section III. When the channel length is comparable to the mean free path of the electrons, the electron transport may become quasi-ballistic, and as a result, the electron velocity may locally reach a value larger than the saturation velocity.

Assuming a constant doping concentration in y-direction, no material (composition) variation, and no heavy doping effects, (7b) can be simplified to

$$\begin{aligned} G_{\rm CH} &= \frac{1}{D_n}\left(\frac{n_{\rm io}}{n_{\rm ie}}\right)^2 \int_0^L N_A(x)\left(\int_0^{t_{\rm Si}} \exp\left(\frac{\psi(x,y)}{u_T}\right)dy\right)^{-1} dx \\ &= \frac{1}{D_n}\left(\frac{n_{\rm io}}{n_{\rm ie}}\right)^2 \cdot P_{\rm CH}. \end{aligned} \tag{9}$$

As shown in (9), the doping concentration and the potential distribution are inside the integral; hence, not only the doping concentration of the pocket implantation is important, as reported earlier [10].

Furthermore, because the mobile charge can be neglected with respect to the depletion charge in diffusion mode, we may assume that the total surface charge Q_s is equal to the depletion charge.

Hence,

$$Q_s(x) \approx -\sqrt{2q\varepsilon_{\rm Si}N_A(x)\psi_s(x)} \tag{10}$$

where $\varepsilon_{\rm Si}$ is the silicon dielectric constant and ψ_s is the surface potential.

The total gate voltage can be divided by the voltage drop over the silicon layer ($V_{\rm Si}$) and the one over the oxide layer ($V_{\rm ox}$) and can be expressed as

$$\begin{aligned} V_{\rm GB} &= V_{\rm Si}(x) + V_{\rm ox}(x) \\ &= \phi_m - \phi_s(x) + \psi_s(x) - \frac{Q_s(x)}{C_{\rm ox}} \end{aligned} \tag{11}$$

where ϕ_m and $\phi_s(x)$ are the workfunction of the gate electrode and the silicon, respectively. $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$, where $t_{\rm ox}$ and $\varepsilon_{\rm ox}$ are the oxide thickness and dielectric constant, respectively.

After substituting (10) in (11), we can derive the surface potential as

$$\begin{aligned} \psi_s(x) = \frac{qN_A(x)\varepsilon_{\rm Si}}{C_{\rm ox}^2} + (V_{\rm GB} - V_{\rm FB}(x)) - \frac{\sqrt{qN_A(x)\varepsilon_{\rm Si}}}{C_{\rm ox}^2} \\ \cdot \sqrt{(qN_A(x)\varepsilon_{\rm Si} + 2\,(V_{\rm GB} - V_{\rm FB}(x)) \cdot C_{\rm ox}^2)}. \end{aligned} \tag{12}$$

The vertical potential distribution can be derived using the one-dimensional (1-D) Poisson's equation. Neglecting the mobile charge again, we can express the vertical electric field $E(y)$ as

$$\frac{\partial E(y)}{\partial y} = -\frac{qN_A(x)}{\varepsilon_{\rm Si}}. \tag{13}$$

We also know that, at the depletion layer edge ($y = W$), the vertical electric field is zero. Hence, applying (13) yields

$$E(y) = \frac{qN_A(x)}{\varepsilon_{\rm Si}} \cdot (W(x) - y)\,. \tag{14}$$

As a result, because $-\partial\psi(x,y)/\partial y = E(y)$ and $\psi(x,0) = \psi_s(x)$, we can express the potential as

$$\psi(x,y) = \frac{qN_A(x)}{\varepsilon_{\rm Si}}\left(\frac{y^2}{2} - W(x)\cdot y\right) + \psi_s(x). \tag{15}$$

ψ_s is, in fact, the maximum potential in the channel in y-direction and hence gives the minimum (surface) hole concentration (8) that affects $G_{\rm CH}$ drastically (9).

However, as shown in Fig. 1, the surface potential depends on the horizontal (x) direction due to the lateral redistribution of charge carriers (i.e., holes) in the nonuniformly doped channel region and the source and drain depletion regions. Equation (12) gives qualitatively only the correct trend for $\psi_s(x)$ because we basically assumed it to be dependent only on the doping concentration and applied gate bias.

We can use (7a), (9), and (12) for qualitatively understanding the experimental and simulation data discussed in Section III.

III. Results

The motivation for this paper was to analyze I_D in pocket-implanted MOSFETs. In order to do so, we first fitted our device simulations to the measurements using MEDICI [13] with block-shaped doping profiles in the channel, which are uniformly perpendicular to the gate. We used the substrate doping concentration ($5 \cdot 10^{16}$ cm^{-3}), the width (75 nm), and the doping concentration ($7.3 \cdot 10^{17}$ cm^{-3}) of the pocket implants as fit parameters. The oxide thickness was 2 nm. In the simulation work, the field- and doping-dependent Lombardi mobility model [14] was used.

Some results for a device with a gate length L_G of 90 nm are shown in Fig. 2. The data show a subthreshold slope of about 75 mV/dec and a threshold voltage of about 0.4 V. We see an increase of the subthreshold current due to the drain-induced barrier lowering, which is directly related to the reduction of the parameter $P_{\rm CH}$ in our model (9), as discussed further in this section. As shown, the simulation data are in good agreement

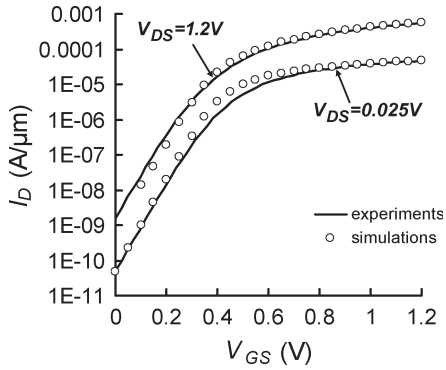

Fig. 2. Experimental (lines) and simulation data (open symbols) of the drain–current I_D versus the gate–source voltage $V_{\rm GS}$ for the saturation mode ($V_{\rm DS} = 1.2$ V, top) and the linear mode ($V_{\rm DS} = 25$ mV, bottom) of the 90-nm-gate-length device (T = 300 K).

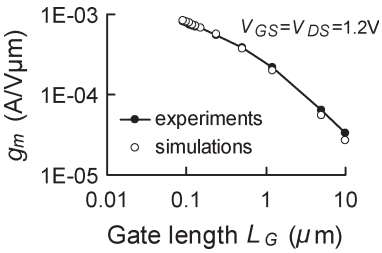

Fig. 3. Experimental (closed symbols) and simulation data (open symbols) of the transconductance g_m per-unit gate width versus the gate length L_G for $V_{\rm GS} = V_{\rm DS} = 1.2$ V(T = 300 K).

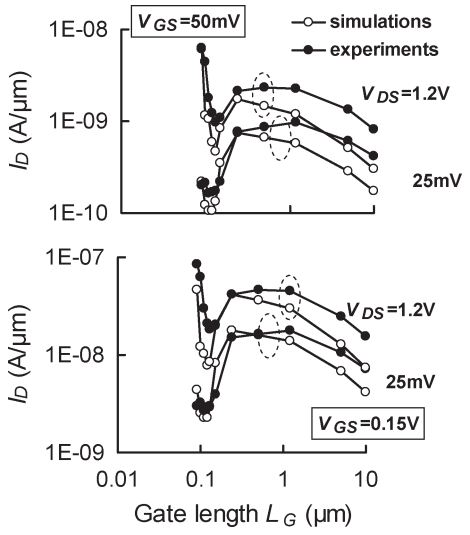

Fig. 4. Experimental (closed symbols) and simulation data (open symbols) of the subthreshold current I_D versus the gate length L_G for $V_{\rm GS} = 50$ mV (top) and $V_{\rm GS} = 0.15$ V (bottom) for both linear region ($V_{\rm DS} = 25$ mV) and saturation region modes ($V_{\rm DS} = 1.2$ V, T = 300 K).

with the experiments. We also checked the simulation data of the (maximum) transconductance (Fig. 3), and we also obtained good agreement with the experimental data. Therefore, we think that it is legitimate to use simulation data for further investigation.

Fig. 4 shows the experimental data of I_D in linear and saturation region modes against the gate length (L_G). For practically

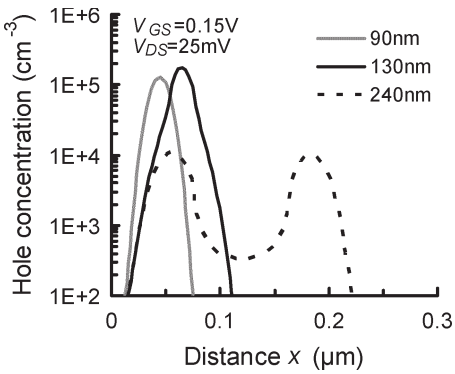

Fig. 5. Simulated hole distributions in the channel region for three gate lengths: $L_G = 90$, 130, and 240 nm ($V_{\rm GS} = 0.15$ V, $V_{\rm DS} = 25$ mV, $T = 300$ K).

all applied voltages, the simulation data are in good agreement. The trend that the I_D of the 5-μm device is higher than that of the 90-nm device in the linear region mode, whereas it is the opposite in the saturation mode is also correct. The systematic difference between simulations and measurements for large L_G is possibly due to a somewhat overestimated substrate doping concentration.

Because we used block-shaped profiles in the simulations, from which the results are in agreement with the measurements, we may say that the exact shape of the doping profile is not important rather the integral $P_{\rm CH}$, as described in (9). This could drastically simplify the (analytical) calculations with (7a) and (9). Given the integral $P_{\rm CH}$ at low bias, the shape of the doping profile is becoming more important for calculating the drain-induced barrier-lowering effect in short-channel devices, as discussed further in this section.

For $V_{\rm GS} = 0.15$ V and $V_{\rm DS} = 25$ mV, the simulated hole distribution in x-direction just underneath the channel is depicted in Fig. 5 for three L_Gs: 90, 130, and 240 nm. For the 240-nm device, the hole distribution has two peak values caused by the pocket implants at the source- and drain side. In the 130-nm device, the pocket implants from the source side and drain side overlap in the middle of the channel. This increases the peak channel doping concentration, which reduces the surface potential according to (12), and hence drastically increases the peak hole concentration according to (8). By reducing L_G from 130 to 90 nm, the peak doping concentration does not change, but due to the source- and drain-induced depletion layers, the hole concentration reduces. For L_G greater than 240 nm, the integral of the hole concentration continuously increases because nothing changes in the pocket implants; only the contribution of the substrate doping increases, integrating it over a longer (channel) length. Hence, the opposite trend aforementioned for the hole distribution is observed for I_D (Fig. 4).

In order to show the validity of the theory described in (9) in combination with (7a), we calculated in our device simulator the integrals for obtaining $P_{\rm CH}$, assuming a constant mobility and intrinsic carrier concentration. Fig. 6 shows the I_D versus the parameter $P_{\rm CH}$ for different L_Gs and three different gate biases. As expected, for the same L_G, the increase in gate bias results in an increase of $P_{\rm CH}$ because of the reduction of the

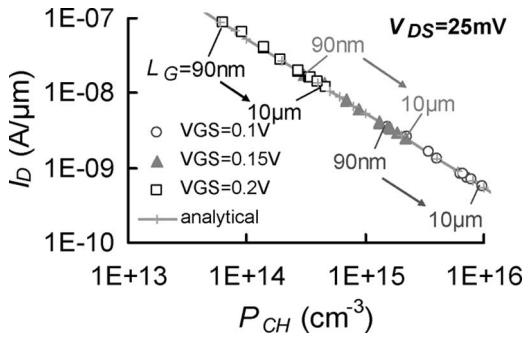

Fig. 6. Simulated subthreshold currents I_D for all available gate lengths L_G versus the parameter $P_{\rm CH}$ for three different applied $V_{\rm GS}$s of 0.1, 0.15, and 0.2 V (T = 300 K). The drawn line represents analytical data obtained from (7a) and (9).

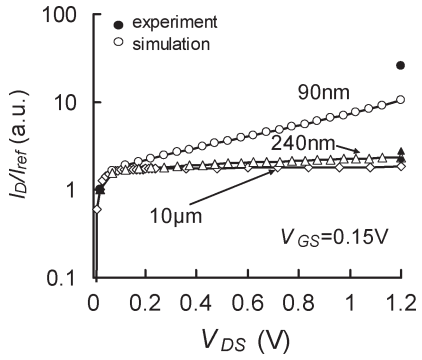

Fig. 7. Drain–source characteristics for $V_{\rm GS} = 0.15$ V for three devices: 90, 240, and 10 μm. Closed and open symbols represent experimental and simulation data, respectively. For reference, the experimental value of the drain–current at $V_{\rm DS} = 25$ mV was taken.

minimum hole concentration. For all gate biases, the $I_D(P_{\rm CH})$ graph shows straight lines with a slope of -1.017, indicating that, indeed, (9) in combination with (7a) can be used. For reference, analytical data obtained from (7a) and (9) are shown in the same figure. We used the product of the diffusion coefficient and intrinsic carrier concentration as a fitting parameter ($D_n \cdot n_i^2 = 5.6 \cdot 10^{21}$ cm$^{-1} \cdot$ s^{-1}). In the saturation mode, the same behavior was observed for the $I_D(P_{\rm CH})$ graph. For this case, the graph is shifted somewhat more upward.

The fact that the hole concentration can directly be linked with the subthreshold currents also implies that, in short-channel pocket-implanted devices, the hole distribution should be (and is) affected by the drain-induced barrier-lowering effect. This effect can be described as follows: At high $V_{\rm DS}$, the potential at the drain side of the channel is increased, thereby reducing the hole concentration locally (8). This reduces $P_{\rm CH}$ drastically in short-channel devices because, for these devices, the peak hole concentrations in the pocket implants are forming the dominant factor in the integral in (9); hence, this affects the current via (7a).

In Fig. 7, simulated drain–source curves for the three different devices (90-, 240-, and 10-μm) are shown at $V_{\rm GS} = 0.15$ V, in which some experimental data points are indicated.

For instance, in the simulations of the 10-μm devices, we see an increase of about a factor of 2 in the current when $V_{\rm DS}$ is increased from 25 mV to 1.2 V, as done in the experiments.

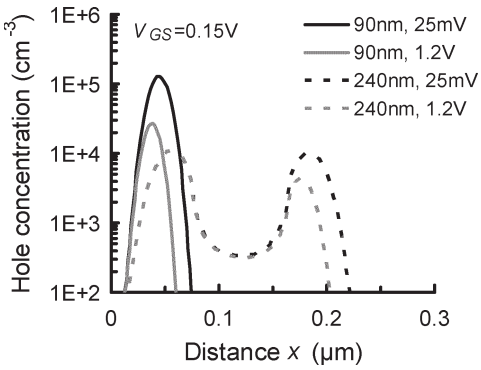

Fig. 8. Simulated hole distributions of the 90- and 240-nm devices in the horizontal direction of the channel region just underneath the gate for different applied drain–source biases 25 mV and 1.2 V (T = 300 K, $V_{\rm GS} = 0.15$ V).

When changing from a gate length of 240 to 90 nm, this factor rises from about 2.5 to 10. In the experiments, however, we see a stronger increase for the 90-nm device, which is 25. This difference could be caused by the shape of the doping profiles that becomes relatively more important for short-channel devices. In our simulation work, we used uniformly shaped doping profiles in the channel region, which is, of course, not realistic. For a less uniform channel doping profile, however, the drain depletion layer extends more in the channel region. This yields a lower $P_{\rm CH}$ and consequently a larger change in current.

Fig. 8 shows the hole distributions for the 90- and 240-nm devices at $V_{\rm DS} = 25$ mV and 1.2 V. As shown, there is a strong reduction of the hole concentration in the 90-nm device compared with that of the 240-nm device when the drain–source voltage is increased. For the former, the integral of the hole distributions reduces by about a factor of 5 when $V_{\rm DS}$ is increased from 25 mV to 1.2 V. When we take into account the change in the electron quasi-Fermi level [the term $(1 - \exp(-V_{\rm DS}/u_T))$ in (7a)], we calculate a total change in current of about a factor of 9, which is close to the factor observed earlier for the simulated drain–current. This indicates that the velocity saturation effect in the drain depletion layer is not important for the subthreshold current in our devices, and hence, (7a) and (7b) are applicable.

IV. Conclusion

We analyzed the subthreshold current of pocket-implanted nMOSFETs, and we have shown that it is directly linked with the 2-D hole distribution in the transistor. The results obtained so far improve the understanding of the subthreshold currents in FETs, which is important for future device modeling. The next step would be to come up with a compact model that is suited for modeling these transistors based on this paper and compare this with models reported earlier. This could imply simplifying (9) and (12) drastically.

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