

Sigma-Delta A/D Converter in HTS Ramp Edge Technology

A. H. Sonnenberg, I. Oomen, H. Hilgenkamp, G. J. Gerritsma, and H. Rogalla

Abstract.— We have successfully fabricated and tested a high temperature superconducting sigma-delta A/D converter. The quantizer is a balanced comparator that has been characterized separately in two temperature regimes. The circuits have been fabricated with ramp edge junctions with a PrBaCuGaO-barrier on a buried ground plane. For the current to voltage conversion in the sigma-delta converter we fabricated a 50 mOhm resistor with an in-situ gold layer. The sigma-delta converter has been tested at an internal clock of up to 174 GHz. The signal-to-noise ratio has been measured at a relatively low frequency of 3.4 kHz and was at least 63 dB but most likely higher since the measurement was limited by the noise in the amplifiers. As a first attempt towards the development of a decimation filter we have fabricated and tested a toggle flip-flop. The toggle flip-flop has been tested successfully at 40 K up to a frequency of 33 GHz, which corresponds to 70 % of the $I_c R_n$ -product of a reference junction.

Index Terms.—Balanced comparator, oversampling, AD converter, toggle flip-flop.

I. INTRODUCTION

APPLICATION of superconducting electronics is generally sought in its possibility to allow high frequency operation, short sampling pulses and/or high precision due to the existence of a fundamental unit of quantization, i.e. the flux quantum. In recent years a strong development has been shown in the niobium trilayer junction technology allowing RSFQ circuits consisting of many Josephson junctions. A further gain in operation speed and sampling pulse width can be obtained by turning to the high temperature superconductors. For example, SFQ-pulses as narrow as 100 fs may be obtained at 4 K by using HTS junctions. Recently, strong improvements in the fabrication technology of high- T_c ramp edge junctions have been demonstrated by the NEC-group showing a ramp edge junction process with a small critical current spread [1]. In this study we present three high- T_c circuits: the balanced comparator, a sigma-delta A/D converter and the toggle flip-flop. The last device is vital for transferring the high data rate to a lower one allowing further processing by another technology.

II. FABRICATION AND CHARACTERIZATION

The quantizer and toggle flip-flop have been fabricated using a three superconducting layer ramp edge junction technology. First, a ground plane of 100 nm DyBa₂Cu₃O_{7-x} (DBCO) is deposited. The ground plane is patterned in order to minimize the probability of shorts, to provide for so-called moats in order to avoid flux trapping, and to minimize the overlap of the wiring layers with the ground plane. The latter is important in order to avoid hysteresis in the junction characteristics due to additional capacitance that is introduced by the ground plane. Next, the dielectric layer is deposited which is a trilayer of SrTiO₃/PrBa₂Cu₃O_{7-x}/SrTiO₃. In this trilayer the STO provides the electrical insulation between ground plane and wiring layers whereas the PBCO provides the dielectric separation since it is more suitable for high frequency applications than STO [2]. The total layer thickness is of the order of 400 nm. After etching the vias in the dielectric layer, the base electrode and a separation layer are deposited. Following, the ramp is etched by unidirectional Ar⁺-ion milling under 40 degrees. After cleaning the ramp by ion milling, the barrier, 18 nm of PrBa₂Cu_{2.9}Ga_{0.1}O_{7-x} and the counter electrode are deposited. In the last two lithography steps the gold contact pads for electrical contacts are deposited and the junctions and inductances are defined by Ar⁺-ion milling.

In the case of the sigma-delta converter the process is slightly more complex due to the addition of the low ohmic resistor. After the deposition of the counter electrode the sample is warmed up again to the deposition temperature of YBCO in a different deposition chamber. Following, 50 nm of YBCO is deposited and when the sample has cooled down to about 100° C, a 50 nm gold layer is deposited in-situ. In this way a low contact resistance is achieved between the YBCO and the gold. After defining the resistor contact pads by ion milling, an ex-situ gold layer is deposited by lift-off in order to define the resistor. Although we have deposited the gold on the contact pads in-situ the contact resistance of the YBCO/Au interface will still dominate the resistor. The contact resistivity is around $6 \cdot 10^{-7} \Omega \text{cm}^2$. Further improvement in the contact resistance might be achieved by depositing the gold at elevated temperatures.

The junctions are 10 μm wide, which allows a maximum critical current density, J_c , of around 10^4 A/cm^2 . The junctions have been characterized by measuring the current voltage characteristics and the magnetic field dependence of the critical current. Before reducing the overlap between the wiring layers and the ground plane the junctions showed hysteresis in their IVC's. The hysteresis has been removed

Manuscript received September 18, 2000. This work was supported by the EC ESPRIT program under contract No 23429.

All authors are with the University of Twente, Faculty of Applied Physics, Low Temperature Division, P.O. Box 217, 7500 AE Enschede, The Netherlands (e-mail: g.j.gerritsma@utwente.nl), tel. +31 53 4893122).

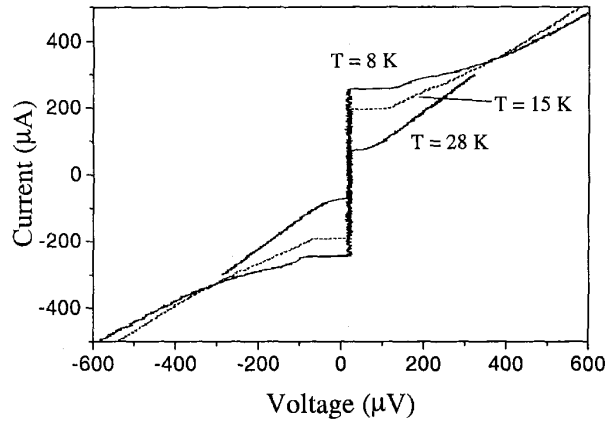


Fig. 1. Current voltage characteristics for different temperatures of a ramp edge junction on top of a ground plane.

successfully by the above mentioned reduction and using the thick insulation trilayer given above. Fig. 1 shows the IVC's at different temperatures. The bump in the IVC at low temperatures can be attributed to the junctions already being in the wide junction limit.

The best values of the spread in the critical current is around 10 % but is based on only four junctions. For further examination a larger data set should be built up. Further improvement in the spread could be sought for in achieving better control over the process parameters in the fabrication. Possible candidates for further improvement are decreasing the roughness of the individual layers, which is currently typically 5 nm rms. Another example is the detailed investigation of the ramp edge formation due to etching and thermal annealing due to heating to deposition temperatures.

Besides better control over the process parameters the spread may be improved as well by adaptation of the interfaces by appropriate doping. For bicrystal junctions, Ca-doping has been shown to increase the critical current density [3], [4]. If doping the superconducting electrodes, or its interfaces, in ramp edge junctions will lead to J_c enhancements as well, this would allow on the one hand thicker barrier layers in order to reduce the spread, and on the other hand possibly an improvement of the high frequency properties by increasing the $I_c R_n$ -product. In order to explore the opportunities of doping the superconducting electrodes in ramp type junctions, we are studying ramp edge junctions in which Ca replaces 20% of the Dy in the $\text{DyBa}_2\text{Cu}_3\text{O}_{7.8}$ electrodes. This substitution is expected to give rise to an effective overdoping. The fabrication process of the ramp edge junctions with doped electrodes is identical to that with the undoped electrodes as described above, except that the ground plane has been omitted and the junctions are 5 μm wide. The thickness of the superconducting base electrode is 100 nm and that of the counter electrode 120 nm, with a $\text{PrBa}_2\text{Cu}_{2.9}\text{Ga}_{0.1}\text{O}_{7.8}$ separation layer of 135 nm. Two barrier thicknesses were studied; 10 and 18 nm. The critical temperatures of the $\text{Dy}_{0.8}\text{Ca}_{0.2}\text{Ba}_2\text{Cu}_3\text{O}_{7.8}$ films were around 75 K, whereas for the undoped $\text{DyBa}_2\text{Cu}_3\text{O}_{7.8}$ films T_c 's in the range 89-92 K were obtained. Fig. 2 shows typical critical

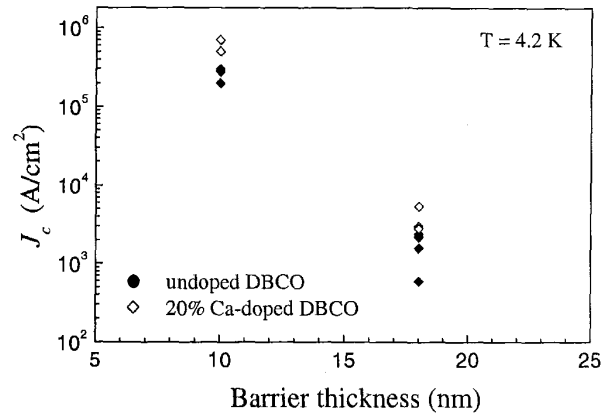


Fig. 2. Critical current density enhancement at 4.2 K due to the Ca doping of the DBCO electrodes.

current density data at $T = 4.2$ K for ramp edge junctions with doped and undoped superconducting electrodes. Despite the reduced critical temperatures of the doped electrodes, the absolute values of J_c were slightly higher than those of the junctions with undoped electrodes and with the same barrier thickness, suggesting a possible improvement of the interface properties. It was found that, while doping enhances J_c , it did not strongly influence the normal state resistivity of the junctions, $R_n A$, so that $I_c R_n$ has also increased slightly due to the doping. These first studies indicate that doping the superconducting electrodes provides an interesting additional degree of freedom for optimization of the junction properties. Further studies on doping the electrodes of the ramp edge junctions are in progress and will be presented elsewhere [5].

The inductance of the microstrips in the circuits has been measured using direct injection SQUIDS. Using these SQUIDS we have characterized the inductance per micrometer in our process and verified the functionality of the ground plane lying underneath the circuits. The inductance has been measured between 4 and 45 K. In this temperature range we have seen only a slight increase in inductance for the microstrips that have a ground plane underneath. We have

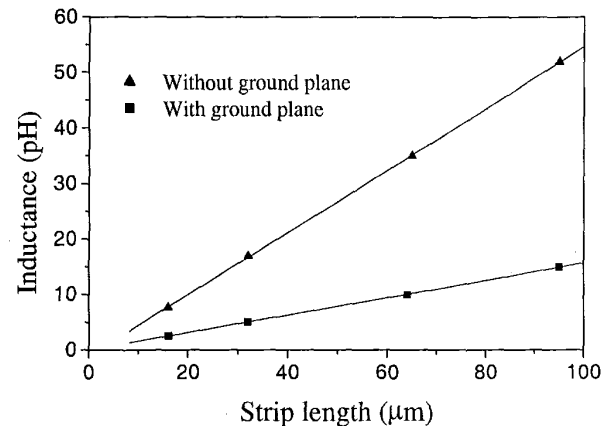


Fig. 3. Inductance as a function of microstrip length at 10 K for a direct injection SQUID both with and without a ground plane underneath the SQUID.

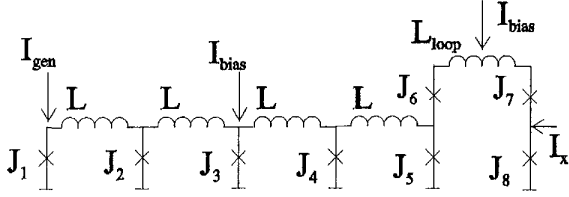


Fig. 4. Equivalent diagram of the balanced comparator.

attributed this increase to the increasing London penetration depth with temperature. We have fabricated SQUIDs with and without a ground plane in order to verify the functionality of the ground plane. The measurements are shown in Fig. 3 and present a reduction in inductance by a factor 3.5 due to the ground plane. This reduction is in agreement with the results found in [6]. For the microstrips with a ground plane we obtain an inductance of $0.16 \text{ pH}/\mu\text{m}$ or a square inductance of 0.80 pH .

III. BALANCED COMPARATOR

The first step in the development of the sigma-delta converter is the characterization of the quantizer. We have chosen for the balanced comparator pair [7], because it is less sensitive to fluctuations in the bias current and sampling pulses in the comparator. The equivalent diagram is shown in Fig. 4. The sampling pulses are generated by biasing junction J_1 with a current higher than its critical current. The pulses arrive at the balanced comparator pair J_7 and J_8 via the transmission line and leave the comparator loop via either one of the junction pair. For the current I_x above a threshold, junction J_7 has a higher switching probability while under the threshold J_8 has a higher switching probability. The uncertainty due to fluctuations in the switching characteristics of the balanced comparator depends on the impedance of the pulse driver that feeds the sampling pulses to the comparator junction pair [6]. For low impedance drivers the width of the gray zone is given by the following:

$$\Delta I_x = \sqrt{2\pi\mu I_{th} I_c}, \quad (1)$$

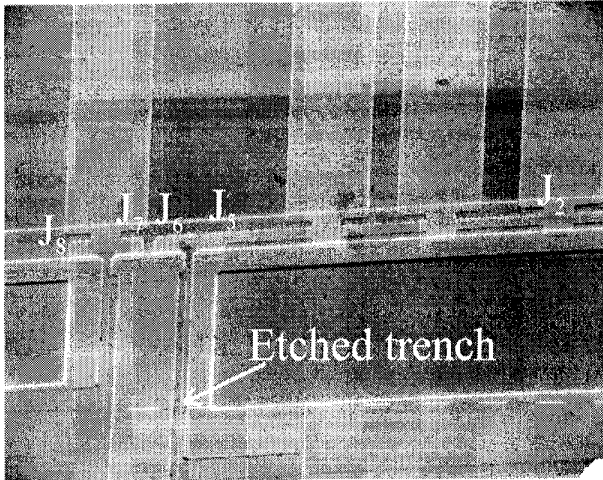


Fig. 5. Detailed picture of the balanced comparator junction pair, junctions J_7 and J_8 .

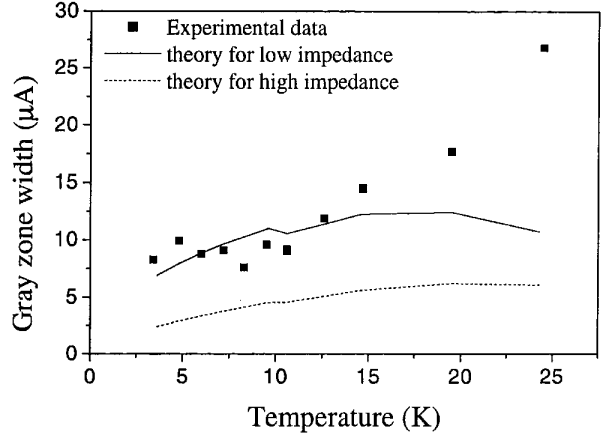


Fig. 6. The width of the gray zone of the balanced comparator in the low temperature regime measured for an generator voltage of $50 \mu\text{V}$.

where μ is a parameter close to one, I_{th} is the thermal noise current and I_c is the critical current of the junction. For the high impedance driver the gray zone width is given by:

$$\Delta I_x = 2.3 I_{th}^{2/3} I_c^{1/3} \quad (2)$$

The gray zone width is in general smaller for the high impedance driver than for the low impedance driver.

Our first layout resulted in a balanced comparator that suffered high capacitive shunts due to the buried ground plane. This shunt leads to hysteretic junctions and hysteresis in the switching characteristic of the balanced comparator. This has been reduced effectively by improving the layout of the balanced comparator by etching a trench in the ground plane as indicated in Fig. 5, and applying a thicker intermediate layer between the ground plane and the electrodes of the junctions and circuit.

The 'new' balanced comparator has been measured in two temperature regimes. For low temperatures the width of the gray zone as a function of temperature is depicted in Fig. 6 for generation voltage of $50 \mu\text{V}$. The measurements are in reasonable agreement with the model for a low impedance driver as expressed by (1). For temperatures higher than 15 K

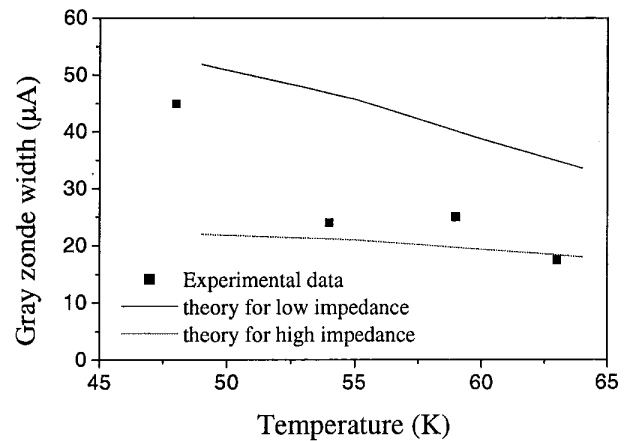


Fig. 7. Gray zone width of the balanced comparator in the high temperature regime.

both models fail to describe the width of the gray zone. However, for these temperatures the generation voltage is relatively high with respect to the $I_c R_n$ -product that drops with increasing temperature. This explains the drastic increase of the width of the gray zone with temperature[8], [9]. The order of magnitude of the gray zone width is in agreement with that found in [10].

In a higher temperature regime, the model that best describes the behavior of the balanced comparator is the one that assumes a high impedance driver (2). The experimental data and model lines are shown in Fig. 7. The measurement point at 48 K, however, seems to fit better to the model for the low impedance driver. This could be explained by the fact that the loop inductance decreases with decreasing temperature. However, care should be taken at this temperature since the junctions effectively were in the wide junction limit due to the increased critical current. Therefore, it could be possible that flux quanta can be stored in the comparator loop due to the increased normalized inductance.

IV. SIGMA-DELTA CONVERTER

By addition of an inductor at the signal input of the balanced comparator, the balanced comparator is used as the quantizer in a sigma delta analog to digital converter[11]. The voltage signal is integrated by the inductor and feedback is provided by the reset current of Φ_0/L . The inductor is designed to be around 150 pH. It is worth mentioning at this point that for proper operation of the modulator this feedback current should be larger than the gray zone of the comparator. Due to the low impedance of the junctions the source is effectively a current source. Therefore, a small conversion resistor is required to convert the current into a voltage. By adding a YBCO/Au layer to the normal fabrication procedure we realized a resistor with a resistance typically between 10 and 50 m Ω . Due to the conversion resistor a cut-off frequency is introduced below which the signal improvement is not the expected 9 dB per octave but only 3 dB per octave since below the cut-off frequency noise shaping is not taking place. The signal to noise ratio can be estimated by taking only the

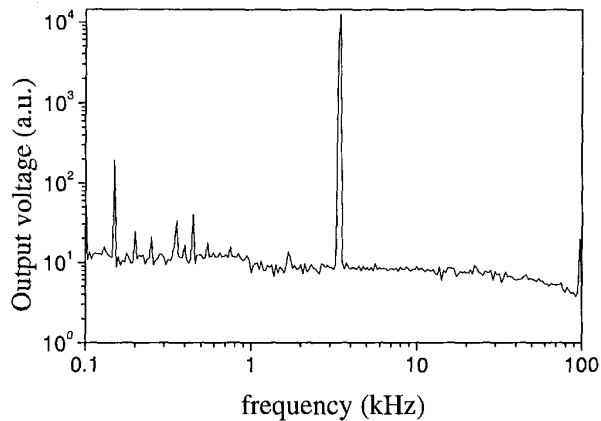


Fig. 8. Frequency spectrum of the sigma delta converter with a signal frequency of 3.4 kHz and a clock frequency of 174 GHz at 10 K. The peaks below 1 kHz and at 100 kHz are due to the instrumentation.

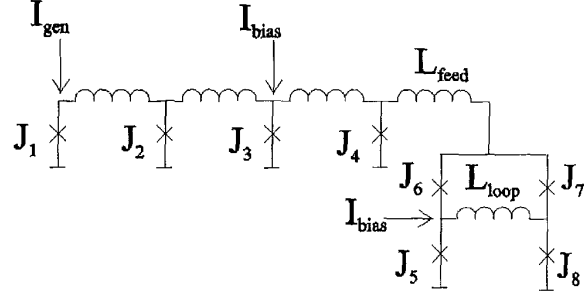


Fig.9. Equivalent diagram of the toggle flipflop.

oversampling ratio with respect to the cut-off frequency for the sigma delta modulation action according to [12]:

$$SNR = \frac{3}{2\pi} \sqrt{2} (OSR)^{\frac{3}{2}} \quad (3)$$

The sigma delta A/D converter has been tested by using a signal of 3.4 kHz that is sampled at different clock rates from 20 GHz up to 174 GHz. The frequency spectrum at the output of the modulator is shown in Fig. 8. For the highest clock rate we have measured a signal to noise ratio of 63 dB which is limited by the noise of the amplifiers of our measurement set-up. The measured noise floor is also present if the modulator is not running. From (3) we can expect a signal to noise ratio higher than 96 dB which is much higher than our measured result. Besides the amplifier noise part of the observed degradation may be due to an increased gray zone at very high frequencies. In that case the value of the integrating inductor should be reduced.

V. TOGGLE FLIPFLOP

A very important element in the reduction of the clock frequency is played by the toggle flipflop, Fig. 9. Again the pulses are generated at junction J_1 and reach the flipflop via a transmission line. The loop of J_5 - L_{loop} - J_8 is capable of storing one flux quantum, while the loop of J_6 - L_{loop} - J_7 is not. The incoming pulses are split by junctions J_6 and J_7 and leave the flipflop toggling between J_5 and J_8 . We have fabricated and tested a symmetric toggle flipflop where the junctions of the non-storing loop, have a critical current of 70 % of that of the storing loop, J_5 and J_8 . The layout of the toggle flipflop is such to minimize the distance between the junctions in the flipflop loop while. All the junctions are oriented in one direction in order to minimize parasitic inductances. This resulted in the switch of functionality of the base and counter electrode when going from the Josephson transmission line to the toggle flipflop. In the first the counter electrode functions as the ground while in the second the base electrode functions as the ground. A very wide junction connects both grounds. A SEM micrograph of the toggle flipflop is shown in Fig. 10.

The toggle flipflop has been tested at 37 K and shows correct divide by two operation up to 65 μ V, Fig. 11. This value corresponds to 70 % of the $I_c R_n$ -product of a reference junction. This is agreement with [13] where it has been shown that the maximum operation frequency up to which a relatively simple RSFQ-circuit can operate successfully is 70 % of the $I_c R_n$ -product.

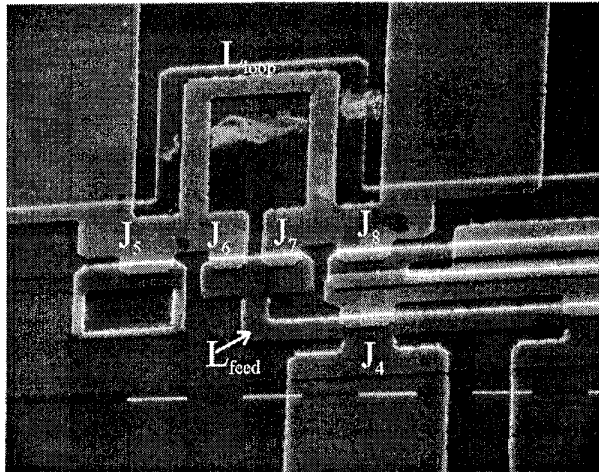


Fig.10. SEM photograph of the toggle flipflop. L_{loop} is the main arm of the flipflop that stores a flux quantum and L_{feed} connects the flipflop to the Josephson transmission line..

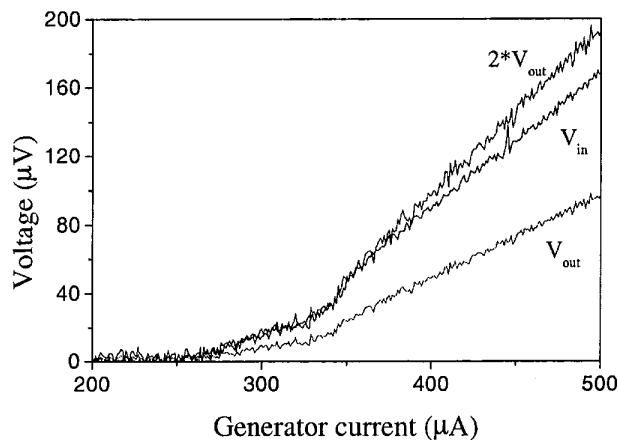


Fig. 11. Correct divide by two operation of the T-flipflop at 37 K over a range of generator voltages.

VI. CONCLUSIONS

Three key subcircuits to a HTS analog to digital converter have been designed fabricated and tested successfully. The first is a balanced comparator that we characterized at a moderate frequency where the fluctuations are mainly determined by the temperature and the corresponding driver impedance at that temperature. By adding an integrating inductor and low-ohmic resistor the balanced comparator has been extended to a sigma-delta converter. Although the resistance is complete determined by interface effects it turned

out to be quite linear. It has been successfully tested over a wide clock frequency range up to 174 GHz. As input signal we used a low frequency sine wave, the frequency of which was determined by the available amplifiers. A signal to noise ratio higher than 60 dB has been obtained, which is still limited by the equipment, although at very high clock rates the increased gray zone of the comparator also comes into play.

First studies have been presented that suggest that overdoping the superconducting electrodes improves the interfaces in ramp edge junctions, which may be of benefit to high frequency circuits.

ACKNOWLEDGMENT

The authors thank the help of H.J.H. Smilde in the growth of the in-situ YBCO/Au layer with pulsed laser deposition.

REFERENCES

- [1] T. Satoh, J.G. Wen, M. Hidaka, S. Tahara, N. Koshizuka, S. Tanaka, "High-temperature superconducting edge junctions with modified interface barriers", *Superc. Sci. Technol.*, Vol. 13, pp. 88-92, Jan. 2000.
- [2] J. Satchell, DERA, United Kingdom, private communication, 1999.
- [3] A. Schmehl, B. Goetz, R.R. Schulz, C.W. Schneider, H. Bielefeldt, H. Hilgenkamp, and J. Mannhart, "Doping-induced enhancement of the critical currents of grain boundaries in $YBa_2Cu_3O_{7.8}$ ", *Europhys. Lett.*, Vol. 47, pp. 110-115, Apr. 1999.
- [4] G. Hammerl, A. Schmehl, R.R. Schulz, B. Goetz, H. Bielefeldt, C.W. Schneider, H. Hilgenkamp, and J. Mannhart, "Enhanced supercurrent density in polycrystalline $YBa_2Cu_3O_{7.8}$ at 77 K from calcium doping of grain boundaries", *Nature*, Vol. 407, pp. 162-164, Sep. 2000.
- [5] I. Oomen, et al., "High-Tc ramp-type junctions with doped superconducting electrodes", to be published.
- [6] H. Terai, M. Hidaka, T. Satoh, S. Tahara, "Direct injection high-Tc de-SQUID with an upper YBCO ground plane", *Appl. Phys. Lett.*, Vol. 70(20), pp. 2690-2692, May 1997.
- [7] T.V. Filippov, Yu.A. Polyakov, V.K. Semenov, K.K. Likharev, "Signal resolution of RSFQ comparators," *IEEE Trans. Appl. Superc.*, Vol. 5(2), pp. 2240-2243, June 1995.
- [8] B. Oelze, B. Ruck, E. Sodtke, T. Filippov, A. Kidiyarova, M. Kupriyanov, W. Prusseit, "Investigation of the signal resolution of a high-Tc balanced comparator", *IEEE Trans. Appl. Superc.*, vol. 7(2), pp. 3450-3453, June 1997.
- [9] A.H. Sonnenberg, G.J. Gerritsma, H. Rogalla, "Balanced comparator fabricated in ramp edge technology", *Physica C*, 326-327, pp.12-15, Nov. 1999.
- [10] V.K. Semenov, T.V. Filippov, Y.A. Polyakov, K.K. Likharev, "SFQ balanced comparators at a finite sampling rate", *IEEE Trans. Appl. Superc.*, Vol. 7(2), pp. 3617-3621, June 1997.
- [11] J.X. Przybysz, D.L. Miller, E.H. Naviasky, J.H. Kang, "Josephson sigma-delta modulator for high dynamic range A/D conversion", *IEEE Trans. Appl. Superc.*, Vol. 3(1), pp. 2732-2735, Mar 1993.
- [12] J.C. Candy, G.C. Temes, "Oversampling methods for A/D and D/A conversion", *IEEE Press*, pp. 1-29, 1992.
- [13] V.K. Kaplunenko, "Fluxon interaction in an overdamped Josephson transmission line", *Appl. Phys. Lett.* Vol. 66(24), pp. 3365-3367, June 1995