Fabrication of metallic nanowires with a scanning tunneling microscope

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A procedure to pattern thin metal films on a nanometer scale with a scanning tunneling microscope (STM) operating in air is reported. A 30 nm film of hydrogenated amorphous silicon (*a*-Si:H) is deposited on a 10 nm film of TaIr. Applying a negative voltage between the STM tip and the *a*-Si:H film causes the local oxidation of *a*-Si:H. The oxide which is formed is used as a mask to wet etch the not-oxidized *a*-Si:H and subsequently, the remaining pattern is transferred into the metal film by Ar ion milling. Metal wires as narrow as 40 nm have been fabricated. Since *a*-Si:H can be deposited in very thin layers on almost any substrate, the presented procedure can be applied to structure all kind of thin films on a nanometer scale. © *1995 American Institute of Physics.*

During the previous 5 years, the scanning tunneling microscope (STM) has attracted interest as a tool for lithography on a nanometer scale.[1–7] In scanning tunneling microscopy tip-substrate interactions are very local, making it possible to modify the surface of a substrate to a very high lateral resolution (<20 nm). Several methods to fabricate metallic nanowires using this technique, have been demonstrated. Ehrichs *et al.*[2] and McCord *et al.*[3] have used an STM induced chemical vapor deposition (CVD) process in which a metalorganic gas is decomposed between the STM tip and the substrate, depositing metal on the substrate surface. A drawback of this technique is that there is only a limited choice of metals which can be deposited, due to the number of gas precursors which are available. Alternatively, the STM can be used to expose organic resist layers. For example, McCord *et al.*[3] have used poly(methylmethacrylate) PMMA, Marrian *et al.*[4] have used SAL 601 and recently Stockman *et al.*[5] have used a Langmuir–Blodgett film. Since these layers do not always conduct sufficiently, the STM tip can penetrate the resist during lithography which can limit the tip lifetime due to mechanical interactions between tip and layer.

In this letter, we present a method to pattern a thin film on a nanometer scale with an STM operating in air, using on a conducting resist layer. The method was inspired by the work of Dagata *et al.*[1] who demonstrated that a hydrogen terminated silicon (111) surface can be locally oxidized with the STM. The oxide layer which is formed can act as a mask for etching the silicon, as was demonstrated by Snow *et al.*[6] A thin film could be patterned with this method if a silicon layer which is both stable against oxidation in air and sufficiently conducting could be deposited on the metal film. Hydrogenated amorphous silicon (*a*-Si:H) is a material which can fulfill both requirements. It is stable against oxidation in air because of its high hydrogen content (≈10 at. %).[8] Thin films of *a*-Si:H can be highly doped, to make them electrically conducting for STM operation. In addition, with plasma enhanced chemical vapor deposition (PECVD) a layer of *a*-Si:H can be deposited on almost any surface at low temperature, because of the high reactivity of the silane radicals. In the following we describe how *a*-Si:H can be used as a STM resist layer to fabricate metallic (in our case TaIr) nanowires.

A 10–20 nm thin film of TaIr is sputtered on an undoped silicon (100) wafer, in a high vacuum ($<10^{-7}$ mbar) triode sputtering system. This metal film has a very low surface roughness (<2 nm measured over a 2×2 μm^2 area) and is, therefore, suitable for the fabrication of nanostructures. On top of the TaIr film, a 30 nm layer of *n*-type *a*-Si:H is deposited. The 30 nm *a*-Si:H is deposited in a PECVD system, using a gas mixture of silane (SiH_4 flow 20 sccm) with 1% phosphine (PH_5) and hydrogen (H_2 flow 100 sccm) and the substrate is kept at 190 °C. Before writing with the STM, the sample is dipped for 10 s in 10% diluted HF to remove any native oxide and passivate the surface with hydrogen.

For the STM lithography a homemade STM operating in air with hand cut PtRh tips is used. Oxide lines are written with a negative tip substrate voltage of 3.5 V, a tunneling current of 50 pA, and a writing speed of 1.0 μm/s. After writing the oxide lines, the sample is etched in tetramethyl ammonium hydroxide (TMAH) for 7 s at 70 °C.[9] This only etches away the not-oxidized regions of the *a*-Si:H film but leaves the oxidized regions intact. The control of this etch step is critical as *a*-Si:H is etched isotropically. Some undercutting is therefore inevitable, however, this can be minimized by etching just long enough to remove the *a*-Si:H layer and not any further. The TaIr film is not etched by TMAH. Figure 1 shows a scanning electron microscope

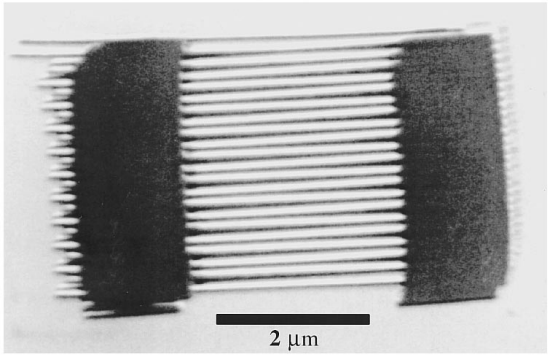

FIG. 1. SEM image of a pattern written with the STM after removing the not-oxidized *a*-Si:H with a wet etch. The resist pattern (*a*-Si:H+SiO_x) appears dark on the metal (TaIr) background.

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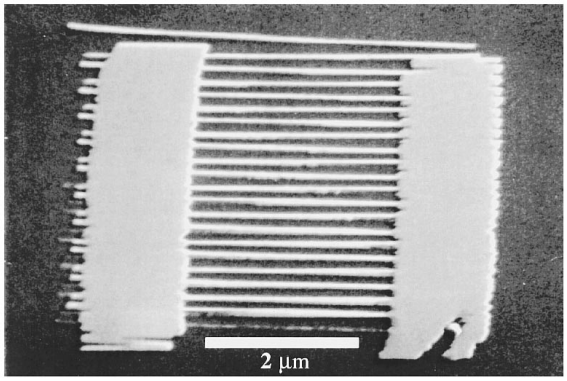

FIG. 2. SEM image of a pattern written with the STM after transferring the resist pattern into the metal (TaIr) film by Ar^+ sputtering, and subsequent removal of remaining *a*-Si:H. The dark background is the Si substrate and the light pattern is metal (TaIr) structure.

(SEM) image of a pattern written by STM after this etch step. The dark pattern is the *a*-Si:H with the oxide layer on top. The metal background appears brighter due to a higher secondary electron yield from the TaIr.

The next step is to transfer this pattern into the metal. To achieve this we use a simple Ar^+ sputter process, during which the *a*-Si:H/SiO_x pattern acts as mask. The sample is sputtered for 150 s in a plasma etching system (Alcatel GIR 300), using Ar (10 mbar) and an rf power of 100 W, giving a self-bias of ~500 V. The sputter time was found to be long enough to remove the TaIr, but not all of the *a*-Si:H resist pattern. After the sputtering a short HF dip was given followed by a 5 s etch in TMAH at 70 °C to remove the remaining silicon oxide and *a*-Si:H which is still left on the TaIr. The SEM image in Fig. 2 shows an STM written structure after this second process step. Compared to Fig. 1 the contrast is now inverted. The dark background is silicon and the brighter pattern is TaIr. The lines written in Figs. 1 and 2 are ~100 nm wide. The width of the lines is determined by the quality of the tip. With a better tip higher resolution can be obtained as can be seen in Fig. 3. This figure shows a SEM image of TaIr wires with a width of ~40 nm, demonstrating the potential of this fabrication technique. Higher resolution can be achieved if thinner *a*-Si:H layers are used and sharper tips are employed.[7]

In order to prove that our metallic wires are really conducting, large gold contact were defined on the structure,

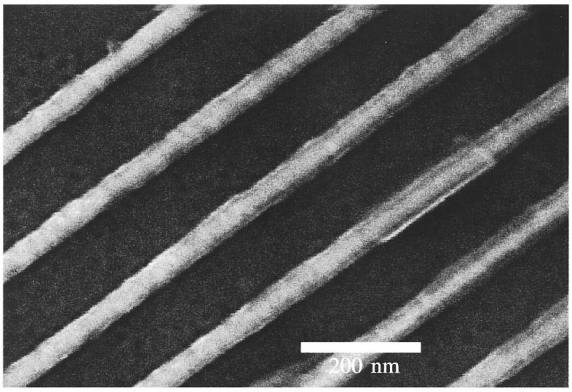

FIG. 3. SEM image of metal (TaIr) wires on Si. The dark background is Si.

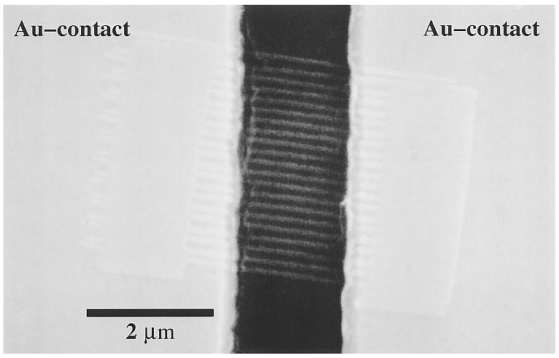

FIG. 4. SEM image of TaIr wires with gold contacts on the left and right. The pattern, similar as in Figs. 1 and 2, can also be seen in the gold contact area due to a height contrast.

using a conventional *e*-beam lithography and lift-off process. Figure 4 shows a SEM image of a contacted structure. Each of the 21 TaIr wires has a width of about 90 nm and a length of 2 μm, defined by the layout of the contacts. Preliminary measurements of the electrical conductivity of the wires are encouraging. The wires are conducting, however, the resistance of the wires, 3 KΩ at 5 K, is larger than would be expected from the sheet resistance of the TaIr film. Based on the sheet resistance of the TaIr film we would expect a resistance of 300 Ω at 5 K. This discrepancy is attributed to a contact resistance between the TaIr structure and the Au contacts. The contact resistance can be reduced if the sample is cleaned carefully before the Au contacts are deposited. Results on the electrical transport properties of these wires will be reported elsewhere. In magneto-transport measurements at low temperatures an increase in the resistance is observed when a magnetic field is applied perpendicular to the wires. Such a behavior can be expected for a strongly disordered metal in which quantum interference effects occur.[10]

In conclusion, a new procedure to pattern thin films with an STM was reported, using hydrogenated amorphous silicon (*a*-Si:H) as resist. The use of *a*-Si:H has several advantages; it is stable against oxidation in air, it is conducting, and it can be deposited in thin layers on almost any substrate. This procedure can, therefore, be applied to structure all kind of thin films and its potential was demonstrated by the fabrication of metallic wires as narrow as 40 nm.

During the writing of this letter we became aware of related work by Minne *et al.* In this work the fabrication of a 0.1 μm metal–oxide semiconductor field effect transistor is demonstrated using a scanning probe microscope as a lithographic tool.[11] Similar to our work, the breakthrough is based on the use of amorphous silicon as resist.

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