ELSEVIER

Journal of Electrostatics 33 (1994) 313–325

Journal of
ELECTROSTATICS

Suppression and origin of soft ESD failures in a submicron CMOS process*

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Received 12 October 1993; accepted after revision 1 April, 1994

Abstract

Soft failures occurring after low-level ESD stress of thick and thin oxide NMOSTs in a submicron CMOS process have been studied. Simple drain engineering appears to have a dramatic improving effect. Simulation is used to study the cause for the soft failures.

1. Introduction

ESD damage manifests itself basically in two ways: in soft failures and hard failures. A hard failure is a short like defect, causing a device to fail functional tests. Soft failures are increased leakage currents. These leakage currents usually lie below device specification limits, and do not keep devices from being functional. By now, the concepts of second breakdown should be familiar for process development and protection design. Soft failures, however, have received attention but are not fully understood yet [1–3]. Reduced input leakage specifications increase the need for a better understanding of the phenomenon even more. In a standard CMOS process with LDD *n*-channel transistors, both thick- and thin-oxide NMOSTs may be sensitive for soft failures. In this paper, leakage currents during stepped ESD stress are studied on thin- and thick-oxide ESD protection transistors in a submicron CMOS process. It is shown how leakage currents evolve during a stepped ESD stress. It is investigated whether design variations like transistor width W, gate length L and contact-to-gate spacing CO-PS influence the susceptibility for low-level ESD stresses and whether there is a correlation between leakage currents after low-level ESD stress and catastrophic failure threshold levels.

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SSDI 0304-3886(94)00011-K

Moreover, the effect of simple drain variations, like omitting the LDD implantation, or overdoping the LDD [4, 2, 3] is studied. Omitting the LDD has the advantage that the process remains the same. It is only required to introduce an LDD mask that differs from the mask with which the $n+$ drain/source areas are defined at the protection transistors. Device simulation is applied to explain the observed behaviour.

2. Experimental

The process under study is a 0.8 μm (drawn) CMOS LDD process, with 15 nm gate oxide thickness. For the ESD stresses (human body model and machine model) a TMT Verifier 2 was used. The machine model had a series inductance of 0.5 μH. Via an intermediate board between tester board and package, an effective series inductance of 2.5 μH could be simulated as well. Furthermore, a transmission line model tester (TLM) with a pulse duration of 100 ns was used, together with an HP547210A, 2Gsamp./s digital storage oscilloscope and an HP4140B pA meter in an automated test-environment.

Typical leakage currents lie in the picoAmp range, which is well below the TMT measurement range. The leakage currents that are typical for soft failures lie between the nanoAmp and the microAmp regime. To evaluate the leakage currents, a HP4142 source/monitor unit and an HP4145 analyser were used. The leakage currents were determined at $V_{ds} = 5.5$ V, with gate (only present in the thin-oxide transistors), source and substrate connected together. The test structures that were used for this study were grounded gate NMOSTs and lateral bipolar transistors (field oxide NMOSTs without a gate). The test structures consisted of various widths, lengths and contact to gate or thick oxide spacings. A subset is shown in the leakage evolution graphs.

In Figs. 1 and 4 the design variations are summarised for the thin- and thick-oxide structures, respectively. With these test structures, the main design parameters can be determined that are relevant for ESD protections.

3. Results and discussion

Typical leakage current evolutions during stepped ESD stress are depicted in Figs. 1–3 for thin-oxide transistors and in Figs. 4–6 for thick oxide transistors. One sees that the behaviour of the test structures is as follows: the entire group of test structures is prone to leakage current increase. In a second stage, the structure fail catastrophically. Interestingly, the leakage current increase is the most severe for the 2.5 μH machine model stresses. To investigate whether there is a relation between leakage currents after a low-level ESD stress and the fail voltage, the leakage current after the first stress (100 V MM or 1 kV HBM) is plotted versus the catastrophic fail voltage in Fig. 7 for thin-oxide NMOSTs. From Fig. 7 it can be concluded that there is no clear relationship. Apparently, leakage and catastrophic failure are two different phenomena. There seems also no relation with design variations. The low-level ESD

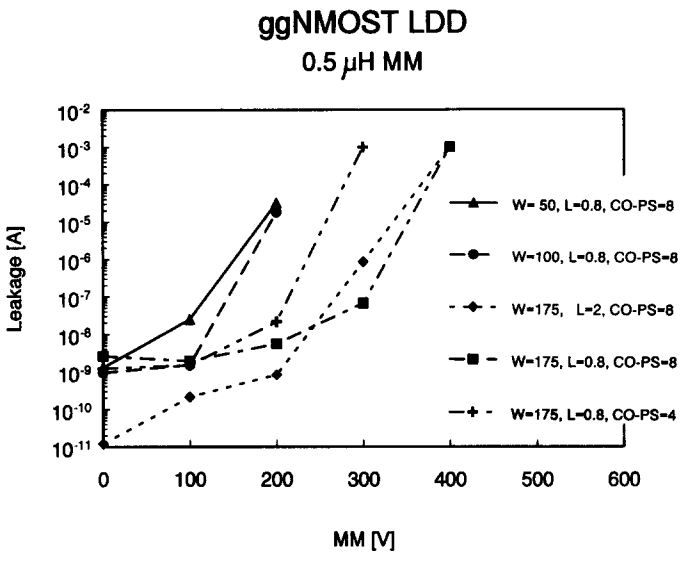

Fig. 1. Leakage evolution during a stepped 0.5 μH machine model ESD stress of various grounded gate NMOS transistors with standard LDD.

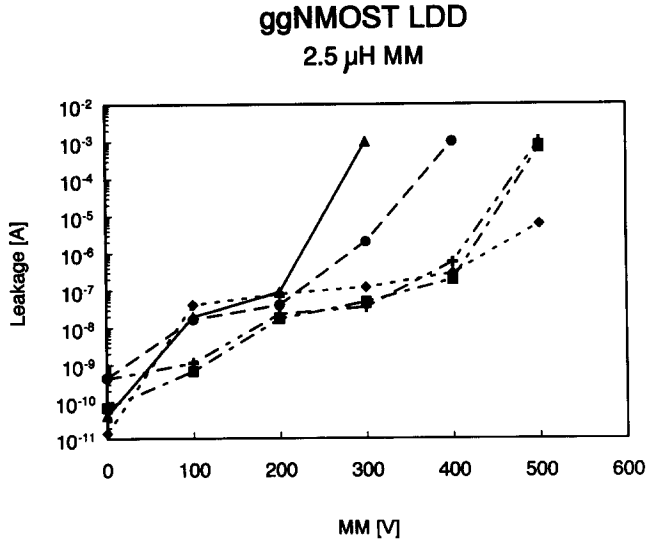

Fig. 2. Leakage evolution during a stepped 2.5 μH machine model ESD stress of various grounded gate NMOS transistors with standard LDD.

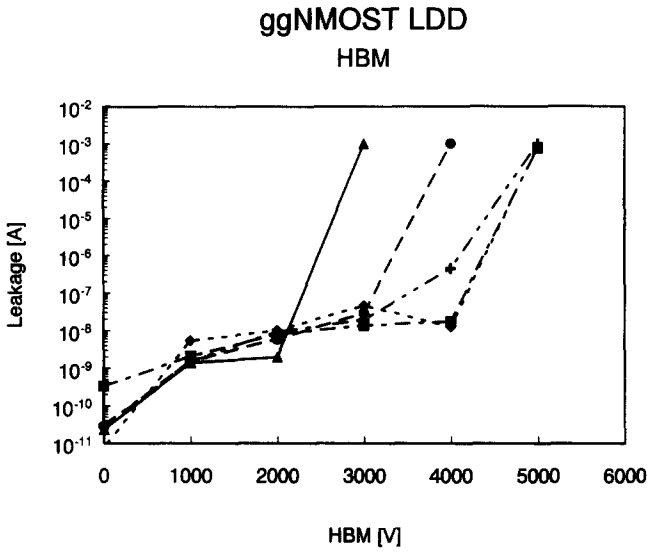

Fig. 3. Leakage evolution during a stepped human body model ESD stress of various grounded gate NMOS transistors with standard LDD.

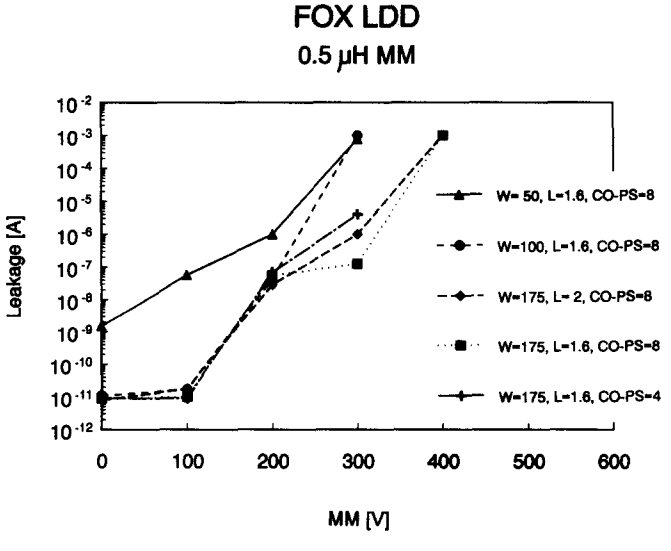

Fig. 4. Leakage evolution during a stepped 0.5 µH machine model ESD stress of various thick-oxide transistors with standard LDD.

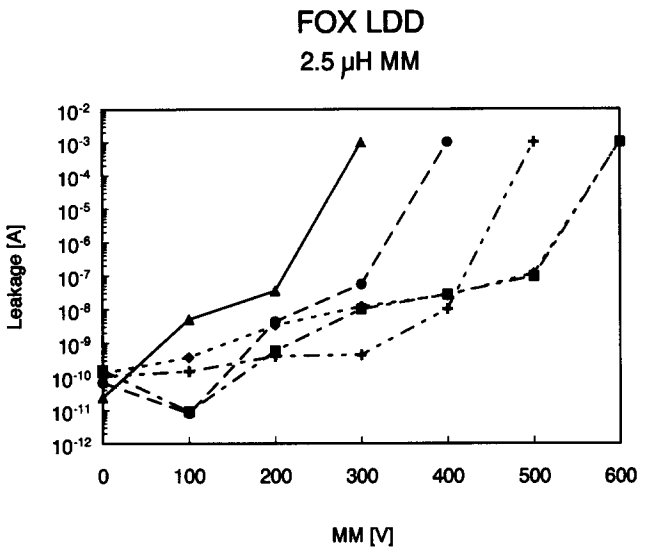

Fig. 5. Leakage evolution during a stepped 2.5 µH machine model ESD stress of various thick-oxide transistors with standard LDD.

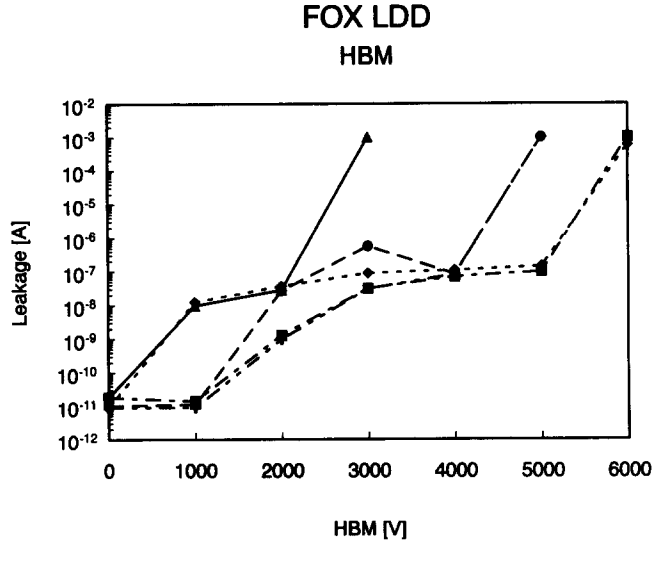

Fig. 6. Leakage evolution during a stepped human body model ESD stress of various thick oxide transistors with standard LDD.

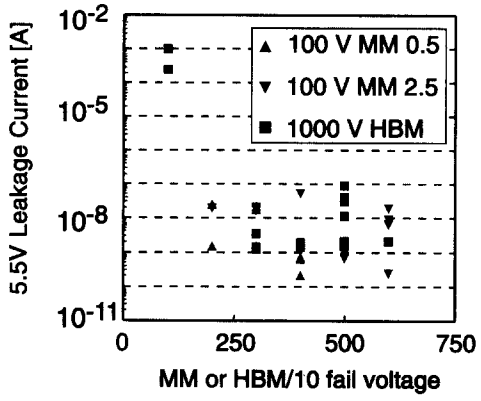

Fig. 7. Leakage current after a 100 V MM or a 1000 V HBM stress versus the catastrophic failure level of grounded gate NMOSTs with standard LDD.

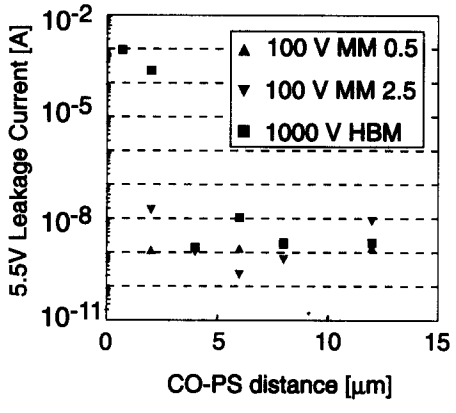

Fig. 8. Leakage current after a 100 V MM or a 1000 V HBM stress verses the contact to polysilicon spacing of grounded gate NMOSTs with standard LDD.

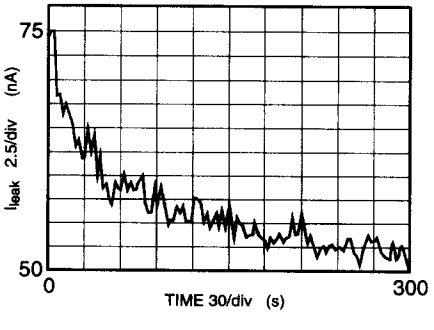

Fig. 9. Typical leakage versus time curve of a grounded gate NMOS transistor with standard LDD immediately after an ESD stress.

leakage level is plotted as a function of the contact to polyspacing in Fig. 8. In the classical concept (i.e. for catastrophic failures), this is a very relevant parameter. The leakage currents that are observed are prone to cold healing: the leakage current decreases in time.

The effect of this decrease is however limited: it is well within a decade, as is shown in Fig. 9 where the leakage current after an ESD stress is depicted as a function of time.

4. Drain engineering

Perhaps the most simple way (and the cheapest, because it does not require an extra process step) to change a drain profile is to leave the LDD implantation out. Other methods are to change the LDD dose or species and to implant an additional dopant at the $n+$ stage to overdope the LDD. We studied omitting the LDD as well as overdoping the LDD with an extra phosphorus implant at the $n+$ stage (see Figs. 10–12). To reduce the number of figures, only some 2.5 μH MM stepped stress results are depicted. It is seen that omitting the LDD as well as overdoping the LDD have similar effects. The soft failures are postponed, whereas the hard failures occur at a similar moment.

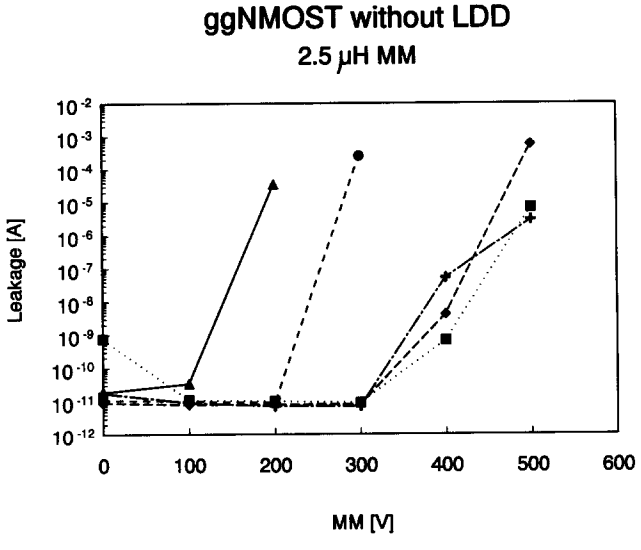

Fig. 10. Leakage evolution during a stepped 2.5 μH machine model ESD stress of various grounded gate NMOS transistors without an LDD.

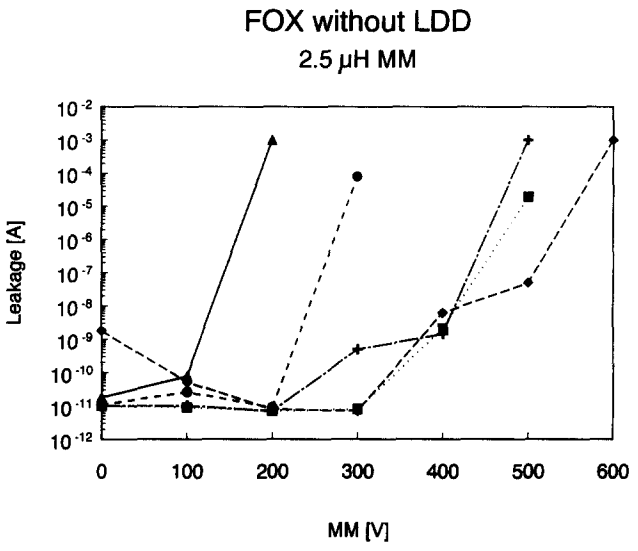

Fig. 11. Leakage evolution during a stepped 2.5 µH machine model ESD stress of various thick-oxide transistors without an LDD.

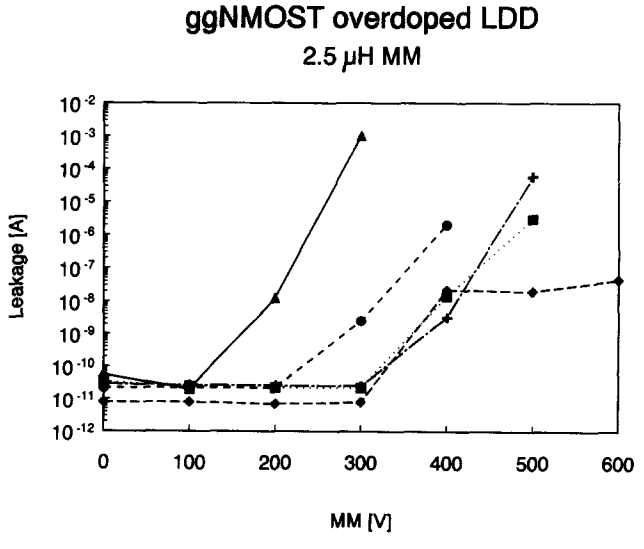

Fig. 12. Leakage evolution during a stepped 2.5 µH machine model ESD stress of various grounded gate NMOST transistors with a phosphorous overdoped LDD profile.

5. Discussion and analysis

For some reason, the LDD junctions are very vulnerable to low-level ESD stresses, and a relative simple change in the profile has already a strong effect. The cause for this effect was studied with a device simulation of a junction in a similar process. The simulator used was 'CURRY', a Philips device simulator. In Figs. 13 and 14 the power density ($J \cdot E$) in the drain of the transistor, which may be used as a measure for the heat dissipation [5], is depicted 2 ns after a typical HBM current pulse was started through a grounded gate NMOST for standard LDD profile and for a junction that was obtained by omitting the LDD implantation. Two nanosecond is well after snapback and gives a good impression of the location of the generation of the heat.

In the simulation of the standard transistor, it is seen that apart from the power density peak deep in the junction, there is an extra dissipative spot just below the surface. Leaving out the LDD reduces this subsurface effect considerably. The existence of such a narrow region was expected from the studies in [2]. Here we see where it is and that we are dealing with two separate mechanisms: one deep in the junction and one just below the surface. In [3] soft failures were attributed to points which had a lower breakdown voltage. From this simulation it is however concluded that the phenomenon is an intrinsic one, occurring parallel to the regular high current effects.

The power density concentration just below the surface is very dangerous. The cooling might not be as effective as deeper in the bulk, resulting in a high-temperature region just below the surface and an early subsurface second breakdown. The

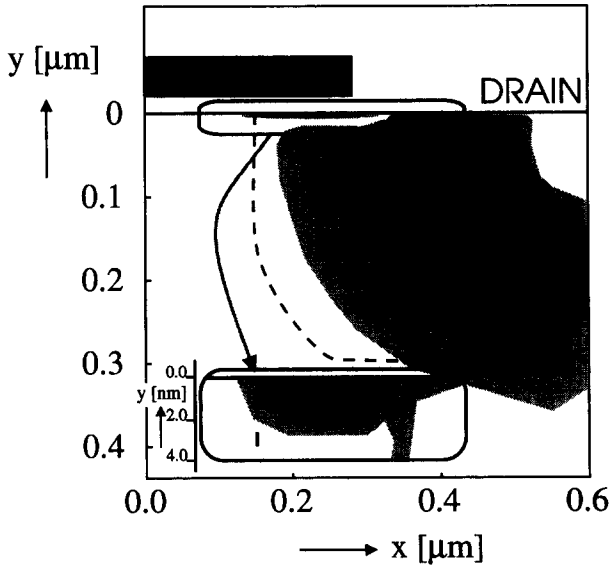

Fig. 13. Power density ($J \cdot E$) of a standard grounded gate NMOST 2 ns after a typical HBM pulse was started.

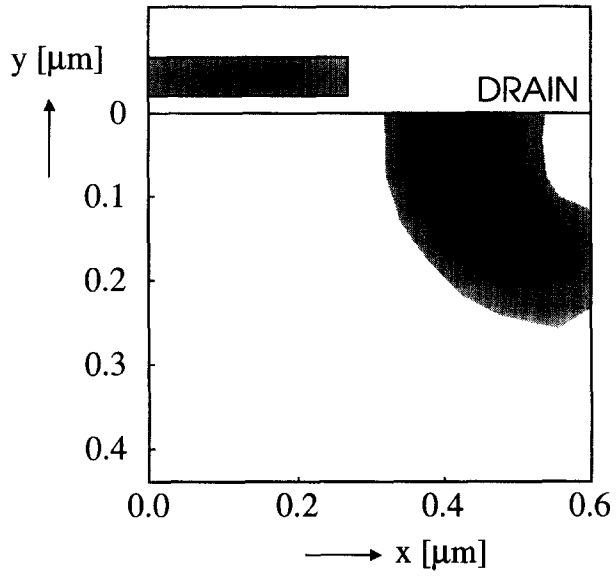

Fig. 14. Power density ($\boldsymbol{J} \cdot \boldsymbol{E}$) of a grounded gate NMOST without LDD 2 n after a typical HBM pulse was started.

experiments suggest that the effect of the subsurface second breakdown is only a damaged junction, recognisable by a leakage current above the nanoAmp range and no catastrophic failures. Failure analysis [1,6] revealed that the damage is not homogeneously distributed and several damaged sites can usually be distinguished. The leaking sites are in fact small filaments, and were made visible in an excellent TEM analysis in [7].

This apparent concentration of damage is typical in the case of a second breakdown with its inherent instability (thermal runaway). The 'subsurface second breakdown' does not cause catastrophic failure. The dissipated energy appears not to be high enough to cause short circuits. The real catastrophic failure occurs at second breakdown of the entire junction, i.e. the classical phenomenon. Due to thermal runaway, the catastrophic failure is localised as well. In Figs. 15 and 16 this process is illustrated by means of a Transmission Line Model analysis of thin oxide transistors, with and without LDD. In these figures, the high current V(I) curve as well as the leakage current after stress are depicted. It is seen that the main effect of omitting the LDD is an increase of the current level at which the soft failure occurs. Only after second breakdown of the entire junction, which is easily recognisable from the V(I) curve, the real catastrophic failure occurs.

The magnitude of leakage current after low level ESD stress does not give information on the ESD voltage level at which the structure will fail catastrophically during the extended step stress. It was also shown that the design variations under study have hardly any effect on the soft failures. The simulations suggest that the soft failure phenomenon is intrinsic and should therefore scale with transistor width. The ESD

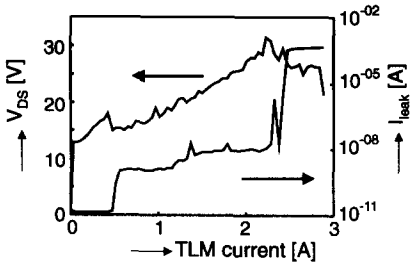

Fig. 15. A V(I) curve and the concurrent leakage evolution during stepped TLM stress of grounded gate NMOS transistors with standard LDD.

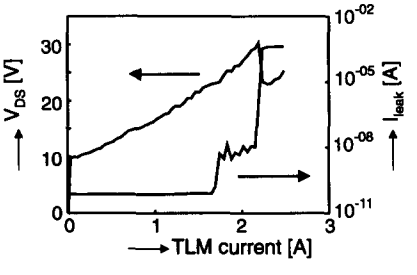

Fig. 16. A V(I) curve and the concurrent leakage evolution during stepped TLM stress of grounded gate NMOS transistors with no LDD.

stresses described here were performed with a large step. A detailed study of the intrinsic nature of soft failures was done with the aid of a Transmission Line Model tester. In Fig. 17 the current at which the catastrophic failure occurs I_{t2} is plotted versus transistor width. Also the current at which the leakage current starts to increase (here defined as I_{ssb}, the subsurface second breakdown current) is shown versus transistor width. It is clearly seen that both currents scale with the transistor width, which proves the prediction of the simulations that soft failures are an intrinsic phenomenon.

There are other effects playing a role as well: After snapback, there is a discharge of the ESD test system, with socket, etc., included. This discharge alone might already be enough to cause local subsurface second breakdown. The form of the discharge is very dependent on the tester characteristics, and would explain why different ESD testers exhibit a different behaviour with respect to soft failures [8]. The difference between 2.5 and 0.5 μH MM stresses is probably caused by this effect as well. Interestingly enough, in [3] it is also mentioned that with respect to soft failures, a machine model stress is more severe than a human body model stress.

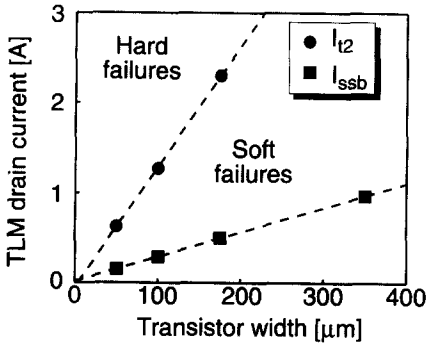

Fig. 17. The TLM current at which the leakage current starts to increase and the current at which catastrophic failure occurs versus transistor width.

6. Summary and Conclusions

ESD damage manifests itself basically in two ways: in soft failures and hard failures. A hard failure is a short like defect, causing a device to fail functional tests. Soft failures are increased leakage currents, that do not keep devices from being functional. In this paper soft failures occurring in thin- and thick-oxide protection transistors are studied. It appears that the magnitude of leakage current after low-level ESD stress does not give information on the ESD voltage level at which the structure will fail catastrophically during the extended step stress. It is also shown that the design variations under study have hardly any effect on the soft failures. On the other hand, simple drain engineering, even omitting the LDD implantation, is shown to lead to dramatic improvement with respect to the soft failure after ESD stresses.

Simulation suggests that soft failures are caused by a subsurface second breakdown. This implies that soft failures are an intrinsic phenomenon, and should scale with transistor width. Transmission line model experiments show that this is indeed the case. Now that the physics of soft failures is understood better, the soft failure behaviour can already be included in the design of a process.

Soft failures are caused by a second power density ($\boldsymbol{J}\cdot\boldsymbol{E}$) region just below the surface. Simple drain engineering, like omitting the LDD implantation, is shown to lead to strong improvement with respect to the onset of leakage, and likewise to the subsurface power density pit. The suppression of the subsurface power density causes the soft failure to occur at higher stress levels.

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