Micromachining of Buried Micro Channels in Silicon

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***Abstract*—A new method for the fabrication of micro structures for fluidic applications, such as channels, cavities, and connector holes in the bulk of silicon wafers, called buried channel technology (BCT), is presented in this paper. The micro structures are constructed by trench etching, coating of the sidewalls of the trench, removal of the coating at the bottom of the trench, and etching into the bulk of the silicon substrate. The structures can be sealed by deposition of a suitable layer that closes the trench. BCT is a process that can be used to fabricate complete micro channels in a single wafer with only one lithographic mask and processing on one side of the wafer, without the need for assembly and bonding. The process leaves a substrate surface with little topography, which easily allows further processing, such as the integration of electronic circuits or solid-state sensors. The essential features of the technology, as well as design rules and feasible process schemes, will be demonstrated on examples from the field of μ-fluidics. [482]**

***Index Terms*—Lab-on-a-chip, micro channels, μ-fluidics, silicon micromachining.**

I. Introduction

MICRO channels are essential components of micro-fluidic systems, in which they act as connections between, e.g., pumps, valves, and sensors [1], as separation columns for several different types of chromatography [2]–[4] or as heat exchangers, e.g., in microreactors [5] or for electronic chip cooling [6]. Initially, most of these structures were fabricated by conventional micromachining in single-crystalline silicon bulk material [7], but recently, with the advent of planar electrophoresis chips, micromachined channels in electrically insulating and optically transparent materials, like glass and quartz, have become of increasing importance [8]–[11].

To construct closed micro channels, wafer-to-wafer bonding techniques like anodic bonding or direct (fusion) bonding are usually required [12]. A disadvantage of such a process is that wafer-to-wafer misalignments [see Fig. 1(a)] and micro voids may be introduced during the bonding process, which may change or even destroy the functional performance of the device. Enclosed micro channels can also be fabricated by surface micromachining, which consists of the embedding of thin-film structural parts in layers of a suitable sacrificial material [13] on the surface of a substrate. The sacrificial material is dissolved, leaving a complete micro channel [see Fig. 1(b)], thus avoiding the need for aligned bonding. The dimensions of such channels are generally restricted by the maximum sacrificial layer thickness (ca. 5 μm) that can be deposited within an acceptable time period.

As an alternative to conventional bulk and surface micromachining, a new method of bulk micromachining, called buried channel technology (BCT), is proposed in this paper. The method is derived from the well-known SCREAM process [14]. Fig. 1(c) shows a typical example of the channels that can be constructed with the BCT method. Important features of the method are large freedom of design and the absence of assembly or wafer-to-wafer alignment steps because processing only occurs on one side of the silicon wafer. Since the structures are implemented underneath the surface of the wafer, the surface is, in principle, still available for integration of electronic circuits, fluidic devices, or sensor chips, which leads to a more efficient use of substrate surface and eventually to further miniaturization.

II. BCT

A. Principle of BCT

The technology consists of the ten basic steps, which are shown in Table I. A bare substrate is covered with a suitable mask material (step 1) and patterned by lithography and etching (step 2). To protect the trench coating, a special process is needed (step 3). This is explained in Section II-B.2. A trench is etched in the substrate (step 4) and conformally coated with a suitable coating material (step 5). The coating is removed only at the bottom of the trench (step 6) and the structure is etched in the bulk of the substrate (step 7). After stripping of the coating (step 8), the structure is sealed by filling the trench with a suitable material (step 9). If required, the structure may be (partly) released (step 10). The depth of the trench (step 4) defines the distance of the center of the channel from the surface of the substrate, while the shape and dimensions of the structures are defined by the type of etchant (step 7), the crystal orientation of the silicon wafer (for the case of anisotropic etching in KOH), and the etching time.

B. Process Schemes

In Table I, four process schemes are given, that differ in terms of the solutions used to etch the buried structure and the materials used to protect the silicon wafer. Methods like isotropic

Manuscript received August 10, 1999; manuscript revised November 16, 1999. This work was supported by the Dutch Technology Foundation Stichting Technische Wetenschappen, by the applied division of Nederlandse Organisatie voor Wetenschappelijk Onderzoek, and by the technology program of the Ministry of Economic Affairs. Subject Editor, R. T. Howe.

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Publisher Item Identifier S 1057-7157(00)02094-1.

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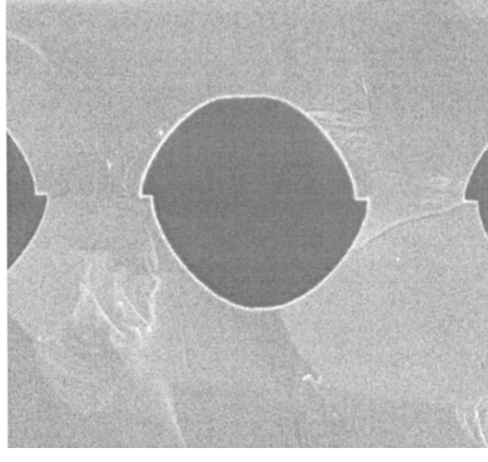
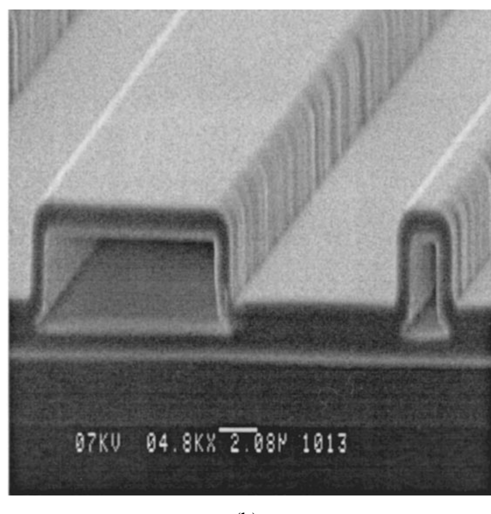


(a)



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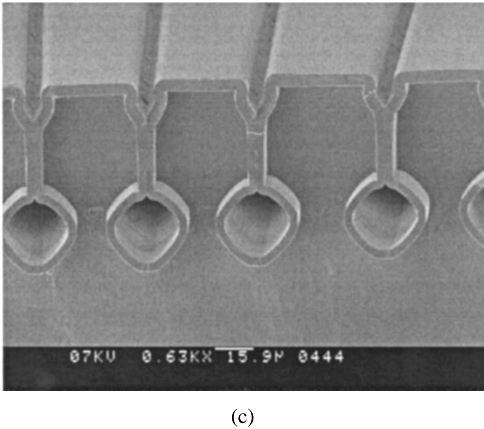


(c)

Fig. 1. SEM pictures of several types of micro channels, fabricated with: (a) bulk micromachining and wafer bonding, (b) surface micromachining, and (c) BCT.

reactive ion etching (RIE) in SF_6 gas, etching in HF–HNO_3 solutions or electrochemical etching in HF solutions are used in process schemes 1– 3, respectively [15]–[17]. In process scheme 4, an anisotropic etchant like KOH is used [18].

When a curved layout has to be fabricated, an isotropic etchant has to be chosen. For these etchants, the etch rate is equal in all directions, yielding a larger freedom in mask layout than when anisotropic etchants are used. Curved mask layouts cannot be fabricated using anisotropic etchants due to the differences in etch rate between the different crystal planes of silicon and underetching at convex mask corners. The shape of the etched structures in that case is determined by the relative etch rate of different crystallographic planes. In practice, the structures will be bound by slowly etching {111} planes.

Fig. 2 illustrates how four different shapes can be constructed in {100} silicon, using the process schemes described in Table I. The shapes are created by varying the depth of the trench and the type of etchants used in step 7.

Hemi-Circular Surface: Complex curved mask layouts can be realized using process schemes 1–3. The shape of the cross section is hemi-circular. Since step 4 is not implemented, steps 5, 6, and 8 can be skipped.

Circular-Bulk: Process schemes 1–3 can be used. All steps of the BCT have to be carried out to construct this type of channels.

V-Groove-Bulk: The process sequence of scheme 4 has to be applied, e.g., in silicon {100} substrates. The shape of the channel is determined by the slowly etching {111} planes in silicon. Simple V-groove (or rather, rhombus-shape) structures are obtained, when the structures are aligned parallel to one of the ⟨110⟩ directions of the silicon crystal. To adjust the size of the V-groove channel, after removal of the coating on the bottom of the trench, an extra deep reactive ion etching (DRIE) step should be carried out. Otherwise, the channel would end up in a small V-groove with the width of the trench. The depth of the extra trench, created by the additional DRIE step, determines the size of the V-groove. The etching time in this case is reduced by the high etching rate of the {110} planes, which make up the sidewalls of the extra trench (Fig. 2).

V-Groove-Surface: Only the process-steps 1–4, 7, and 9 of scheme 4 are used to construct the V-groove-surface channel in silicon {100}. The size of the V-groove shape is determined by the depth of the extra trench created during DRIE and the slow etching {111} planes in silicon. In the following sections, the essential features of the process steps of BCT will be discussed in detail.

1) Mask Material and Pattern Transfer: The mask material has to withstand all the process steps mentioned in Section II-A. Most importantly, the desired mask layout has to be transferred to the mask material with high precision. Furthermore, the material has to withstand the etching of the buried structure in step 7, while it should possess a low internal stress, to avoid bending of the wafer. It was observed that during pattern transfer to the silicon–nitride mask material, using a photoresist mask and RIE-CHF_3 etching, widening of the mask opening occurred. The reason for this is that, during the RIE process, the photoresist pattern erodes at the edges, leaving a tapered profile in the silicon–nitride mask material. This results in a widening of the trench and problems with closure of the trench in step 9. A thin chromium layer (50 nm) on the silicon nitride can be used to prevent this problem. The chromium mask is not eroded during RIE-CHF_3 etching.

2) Protection of the Coating: When no precautions are taken, in some cases very small undesired openings are etched into the protective coating layer. These openings were observed

TABLE I
DIFFERENT PROCESS SCHEMES FOR BCT

Step nr.	Scheme 1 (Isotropic-Dry) RIE	Scheme 2 (Isotropic-Wet) Electrochemical HF	Scheme 3 (Isotropic-Wet) $HF/HNO_3/H_2O$	Scheme 4 (Anisotropic-Wet) KOH
Substrate specifications	p or n-type silicon resisitivity not critical crystal orientation not critical	p-type silicon resisitivity 0.01-10 ohm.cm crystal orientation not critical	p or n-type silicon resisitivity not critical crystyal orientation not critical	p or n-type silicon resisitivity not critical anisotropic etching {100}, {110}
1: Mask material	Thermal SiO_2 + Cr	LPCVD of Si_xN_y + Cr	LPCVD Si_xN_y + Cr	LPCVD Si_xN_y + Cr
2: Pattern transfer	Lithography,RIE-CHF_3	Lithography,RIE-CHF_3	Lithography,RIE-CHF_3	Lithography,RIE-CHF_3
3: Protection of coating layer	1.Underetch DRIE 2. Isotropic pre-etch 3. SLE-etch	1. Isotropic pre-etch or 2. SLE-etch	1. Isotropic pre-etch 2. SLE-etch	1. Isotropic pre-etch 2. SLE-etch
4: DRIE of the trench	Cryogenic ICP-SF_6 plasma	Cryogenic ICP-SF_6 plasma	Cryogenic ICP-SF_6 plasma	Cryogenic ICP-SF_6 plasma
5: Coating of the trench	Thermal SiO_2	LPCVD Si_xN_y	LPCVD Si_xN_y	LPCVD Si_xN_y
6: Etching of the coating at the bottom of the trench	RIE-SF_6	RIE-SF_6	RIE-SF_6	RIE-SF_6
7: Etching of the buried structures	Isotropic SF_6 plasma	Electrochemical etching in HF	$HF/HNO_3/H_2O$	KOH
8: Stripping coating	SiO_2in HF, BHF	HF (50%)	HF(50%)	HF (50%)
9: Filling of the trench	LPCVD of poly Si, SiO_2 or Si_xN_y	LPCVD of poly Si, SiO_2 or Si_xN_y	LPCVD of poly Si, SiO_2 or Si_xN_y	LPCVD of poly Si, SiO_2 or Si_xN_y
10: Release of channels	SixNy: KOH	SixNy: KOH	SixNy: KOH	SixNy: KOH

to lead to the formation of holes in the silicon during step 7 [see Fig. 3(a)]. Since the size and position of the holes is unpredictable, these holes make sealing of the buried structures in step 9 more difficult and, therefore, they should be avoided. The effect is most pronounced when isotropic etching is used because in that case etching is not limited by slowly etching crystal planes.

Preliminary experiments showed that a small underetching of the mask during DRIE of the trench resulted in a good protection for buried structures, based on process scheme 1, with

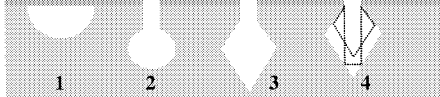
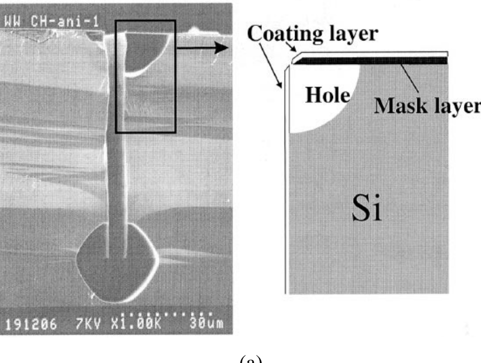
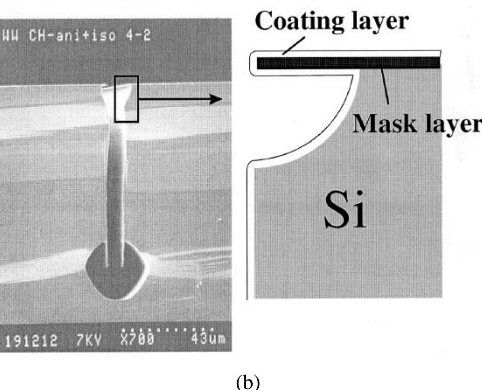


Fig. 2. Different shapes of micro channels made by thin-film techniques and BCT process schemes. (1) Hemi-circular at surface. (2) Circular in bulk. (3) V-groove in bulk. (4) V-groove at surface.



(a)



(b)

Fig. 3. (a) Buried channel etched without the isotropic per-etch step. When the silicon nitride at the bottom of the trench was removed, the nitride at the top corners also opened, resulting in the voids at the side of the trench. (b) Buried channel etched with an isotropic pre-etching step. In this case, no unwanted voids appear.

a diameter less than 5 μm. Since in this case the substrates are only subjected to the etching medium for a relatively short time, coating of the trench was done by thermal oxidation of the silicon [see Fig. 4(a)]. However, it was observed that the protection was not very reproducible, due to small variations of the underetching during the DRIE process. Furthermore, in case the trench was protected with a deposited layer, it was found that for trenches with small underetching, the coating at the edges of the trench was not sufficiently protected by the mask. To obtain a good protection, a special process step had to be implemented in the process schemes 2–4. Two methods were developed to obtain a good protection. The first method is based on an isotropic pre-etch, creating an underetched region in the substrate directly beneath the mask [see Figs. 3(b) and 4(b)]. After trench etching, the coating was also deposited on the underside of the mask layer, due to good step coverage of the low-pressure chemical vapor deposition (LPCVD) process used in step 5. In Fig. 3(b), a buried channel is shown after isotropic pre-etching, and it can be seen that no holes appear in unwanted positions along the trench.

The second method is based on sacrificial layer etching. A silicon–dioxide layer was applied before the deposition of the silicon–nitride mask layer in step 1. The silicon–dioxide layer was sandwiched between the silicon substrate and the silicon–nitride mask, as is shown in Fig. 4(c). After deep silicon trench etching, a small cavity was created by etching of the oxide layer in HF. The cavity was completely filled with the silicon–nitride coating and perfect protection was achieved. Advantages of the latter process are that the uniformity of underetching across a wafer and from wafer to wafer is generally better than in the case of the isotropic underetching of Fig. 4(b), and the fact that the upper part of the trench can be filled more easily by the closing process of step 9 so that the silicon substrate surface will be more planar than in the case of the isotropic pre-etching.

3) DRIE of the Trench: For DRIE trench etching, we used cryogenic SF_6-based plasma chemistry [19] and a state-of-the-art inductively coupled plasma (ICP)-RIE system by Oxford Instruments, Bristol, U.K. The maximum size (diameter) of circular bulk and V-groove-bulk structures is mainly determined by the depth of the trench in the substrate. The maximum depth is determined by the width of the trench and the maximum obtainable aspect ratio (depth/width) of the RIE processes [20], which, in our process, is ca. 25. The growth rate and intrinsic stress of the material to seal the buried structure determine the maximum allowable width of the trench. In practice, the trench should be smaller than 5 μm to avoid excessive deposition process times. Too high a stress in the sealing material may introduce bending of the wafer and render further processing almost impossible. The profile of the trench must have no taper [see Fig. 5(a)], which can be achieved by an optimization procedure that was described before [21], [22]. In case of a positively tapered trench [see Fig. 5(b)], the coating at the sidewalls will also be etched in step 6, increasing the probability of the appearance of pinholes in the coating. Sealing (step 9) will also be difficult in case of a tapered trench. In case of a positively tapered trench, the closing will take place only at the bottom, whereas in the case of a negatively tapered trench, the top of the trench will be closed [see Fig. 5(c)]. The roughness of the walls is also important. A conformal coating adopts the texture of the trench wall. In case of a rough wall, pinholes are easily etched in the coating during process step 6, and may give unwanted holes in the silicon during etching of the buried structures. For a smooth silicon trench wall, we observed no pinholes in the coating after step 6. To achieve this, a process with a relatively high oxygen flow was used [19]. A disadvantage of the described process is that smaller mask openings etch slower than wider mask openings. This is a well-know effect called "RIE-lag" [20]. To control the depth of the trenches, a multimask procedure may be used. To obtain trenches with the same depth, the layout has to be split up in several masks, each mask containing only openings or structures of one particular size. The larger openings are protected with photoresist and the smaller openings are preetched to a certain depth. After the photoresist is removed, all the openings can be etched in one run.

4) Coating of the Trench: The coating layer must be pinhole free and uniformly deposited or grown in the trench to protect the silicon wafer during etching in step 7. Processes like LPCVD

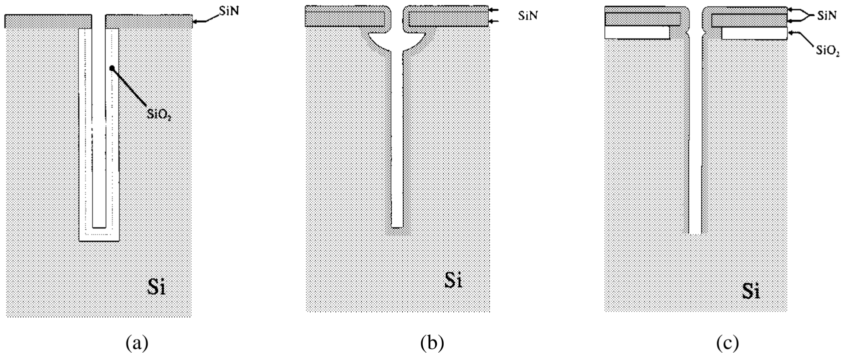


Fig. 4. Three methods to protect the coating in the trench. (a) Underetching (plus thermal oxidation). (b) Isotropic pre-etch. (c) Short sacrificial layer etch.

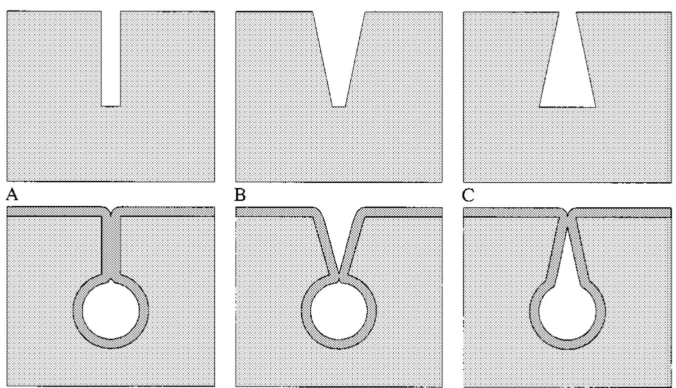


Fig. 5. Different trench shapes and their effect on the sealing procedure in step 9. (a) Without taper. (b) Positive taper. (c) Negative taper.

TABLE II

PROCESS PARAMETERS FOR ETCHING OF THE SILICON–NITRIDE LAYER AT THE BOTTOM OF A DEEP TRENCH USING AN ELECTROTECH PLASMAFAB 310/340 RIE MACHINE. TRENCH DEPTH AND WIDTH WERE 75 AND 5 μm, RESPECTIVELY

Power (*W/cm²*)	V_{dc} (*Volt*)	*Pressure* (*mTorr*)	*SF_6 flow* (*sccm*)	*SiN layer* (*μm*)	*Etching rate at surface* (*nm/min*)	*Etching rate in trench* (*nm/min*)
0.15	-240	1	25	0.3	85	35
0.15	-240	1	25	0.6	85	27
0.20	-350	1	25	0.6	110	50

of silicon nitride [23] or silicon dioxide [24], or thermal oxidation of silicon may be used. Another aspect to take into account is the mechanical stability of the coating. During etching of the buried structure, the coating of the trench walls will become partially freestanding. Due to bending of the coating material, the trench can be locally closed, which may slow down etching.

For a proper process, the etch rate in step 7 of the coating material should be significantly lower than the etch rate of silicon. For process schemes 2–4, we used LPCVD silicon nitride with a thickness of 300 nm for trenches with an aspect ratio (depth/width) of 0.1–15. For layers thinner than 200 nm, we observed holes in the silicon trench wall due to pinholes in the silicon nitride after etching of the buried channels. For trenches with a high aspect ratio (15) coated with a thick silicon–nitride (more than 600 nm) layer, we observed a low etch rate at the bottom of the trench (step 6). The low etch rate will be explained in Section V. For process scheme 1, we used thermal silicon dioxide with a thickness of 400 nm. The etch rate of silicon dioxide under the isotropic SF_6 plasma etch conditions described in Section VI is a factor of 100 lower than that of silicon nitride.

5) Etching of the Coating at the Bottom of the Trench: To remove the coating at the bottom of a deep trench without creation of pinholes in the coating at the sidewalls, a directional etching process like low pressure RIE SF_6 plasma has to be used. To be able to adjust the parameters of the RIE process correctly, first the plasma properties that determine directional etching have to be explained. Directional etching in plasma processes is a result of ion-enhanced reactions [25]. In a plasma, the sheath electric field (V_{dc}) accelerates ions along the macroscopic surface normal, creating a directed flux of energetic particles, which induce directional etching [26]. Ion scattering in the sheath produces a distribution of bombarding kinetic energies and angles at the surface, called the ion energy distribution (IED) and ion angular distribution (IAD), respectively [27]. The energy and angle of an ion incident on a surface are determined by the electric field in the sheath, the ratio of the sheath thickness to the mean-free-path, and the number of RF cycles required for an ion to cross the sheath. These parameters are determined by operating conditions such as power, frequency, electrode spacing, and pressure. Directional RIE SF_6 etching can be obtained at low pressures (below 10 mtorr), relatively high ion energies (200 eV), and high plasma frequencies (13.56 MHz and higher). At low pressures and high frequencies, ion scattering in the sheath is low and most of SF_5^+ ions of the SF_6 plasma will enter the trench traveling in a direction perpendicular to the bottom of the trench (small IAD). In that case, the IED is also small, which means that most of the ions will hit the bottom of the trench with the energy gained by the electric field (V_{dc}) in the sheath [28].

By applying this process, we removed the bottom of trenches with aspect ratios of up to 15 without etching pinholes in the coating on the sidewalls. In Table II, the process parameters are given, which are used to remove the silicon–nitride coating at the bottom of the trench, using an Electrotech Plasmafab 310/340 RIE. We observed that for trenches with a depth of 75 μm and a width of 5 μm, which were coated with 300-nm silicon nitride, the ion energy had to exceed 200 eV (V_{dc}) to remove the coating from the bottom of the trench. An explanation

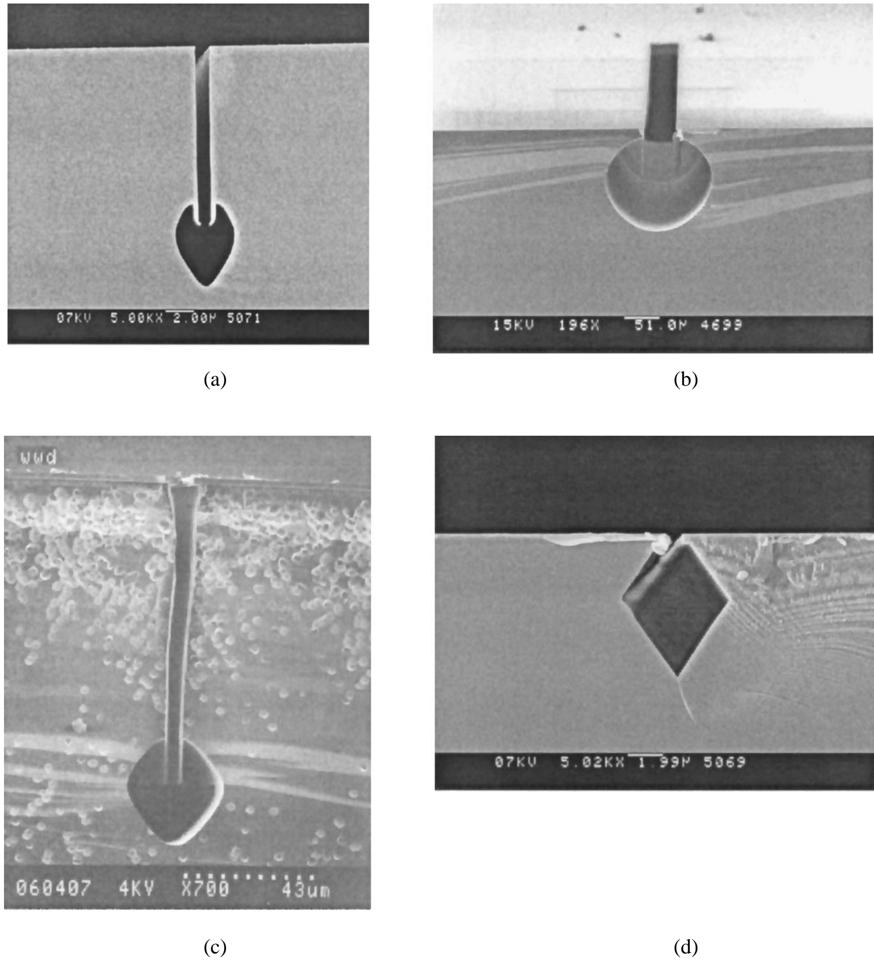


Fig. 6. Different channel shapes obtained after step 7. (a) Pear-shaped channel, obtained by isotropic RIE. (b) Circular channel etched electrochemically in an 5% aqueous HF solution. (c) Circular channel obtained after wet chemical etching in HF-HNO_3 solution. (d) V-groove channel obtained after KOH etching.

for this rather high required energy may be that, due to charging of the silicon nitride through electrons from the plasma, an electric field is induced in the trench [29]. The SF_5^+ ions are deflected by the electric field in the trench, move toward the walls of the trench, and will not reach the bottom of the trench. To verify this assumption, more research will be required. Due to the charging phenomenon, the etch rate at the bottom of the trench is lower than the etch rate at the surface of the wafer (see Table II). We observed that, when the aspect ratio of the trench was higher, the etch rate at the bottom was also reduced. The aspect ratio was increased by the layer thickness of the deposited coating in the trench, thereby reducing the width of the trench. For a trench coated with 300-nm silicon nitride the aspect ratio is 17, and for a trench coated with 600 nm, the aspect ratio is 20. The etch rate at the bottom is reduced by 23%.

The charging phenomena and influence of the aspect ratio on the etch rate at the bottom of the trench imply that the mask on the substrate (step 1) must be thicker than the coating. For silicon dioxide under similar process conditions, we observed the same phenomena as mentioned in Table II.

6) Etching the Buried Structure: Process scheme 1: Isotropic etching of silicon using RIE-SF_6 plasma can be achieved by reducing the self-bias of the RF plasma, thereby decreasing the kinetic energy of the ions. The isotropic etching rate of silicon can be increased by using pressures above 250 mtorr, high SF_6 flows, substrate temperatures above 25 °C, thereby enhancing the spontaneous chemical processes of the plasma [30]. The etch rate was in the order of 1.0 μm/min. The plasma etched structures where not perfectly circular, but pear-shaped [see Fig. 6(a)]. These experiments were done on an Electrotech Plasmafab 310/340 RIE apparatus. The anisotropic behavior of the plasma is probably due to ions that are continuously accelerated by the plasma potential to a kinetic energy of 10 eV.

In process scheme 2, we used a p-type silicon substrate in an electrochemical etching process in a 5% aqueous HF solution [see Fig. 6(b)]. The samples were etched at a potential of 3 V versus Ag/AgCl. The etching rate was 1 μm/min and the shape of the etched structures was circular. In process scheme 3, we used a 5:15:80 vol-% solution of HF (50%), HNO_3 (69%) and DI water to etch a circular shape in silicon. In order to achieve perfect wetting of the trench, the substrate was subsequently immersed in acetone, isopropanol, and water. The substrate was not allowed to dry during transfer from one liquid to the next, and was left in each liquid for at least 5 min. The shape of the cross section was not completely circular; but showed some minor anisotropy [see Fig. 6(c)]. An explanation of this phenomenon could be the depletion of active etching species or the

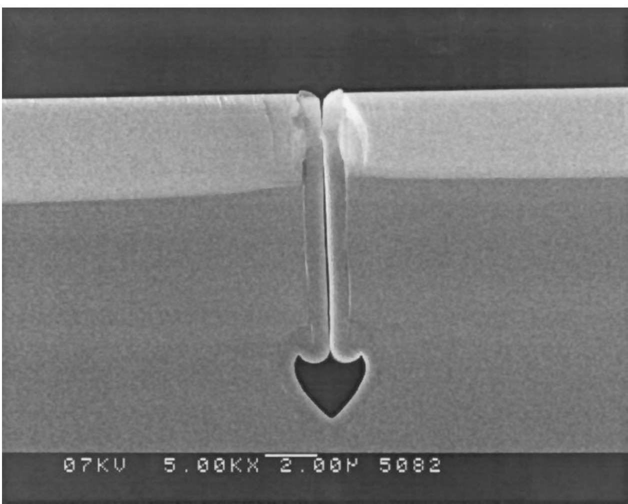


Fig. 7. Structure after sealing with silicon nitride.

accumulation of etching products in the trench, which gives rise to a lower driving force for etching, which is known to give rise to increased anisotropy [31]. As can be derived from measurements of the etching rate, which was 1 μm/min at the surface of the wafer and 0.3 μm/min at the bottom of a trench with an aspect ratio of 85/5, the etching rate in the trench is indeed hampered by limited mass transport. Finally, Fig. 6(d) shows the result of anisotropic etching in a 25 wt-% KOH solution at 78 °C.

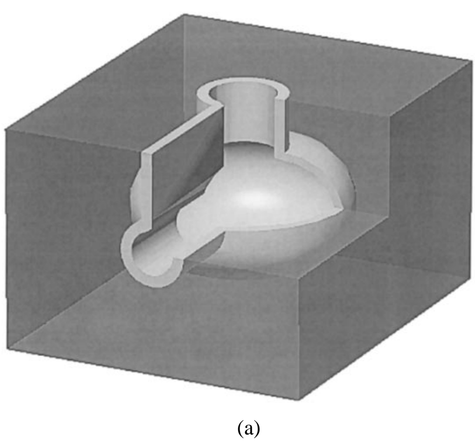
7) Filling of the Trench: Before filling of the trench, the coating layer has to be stripped. For materials like silicon nitride and silicon dioxide, this can be done by wet chemical etching in an HF solution, although it has to be mentioned that the stripping rate of silicon nitride is generally very low in such a solution.

For a perfect seal, a deposition process with an excellent step coverage is required. The deposition rate determines the maximum layer thickness that can be deposited in a reasonable time. The material should also have a low residual stress to avoid bending of the wafer. The choice of the filling material also depends on whether or not a second buried structure should be integrated (see Section III). To achieve a perfect closure, the trench should have no taper (see Section III and Fig. 7). Processes like LPCVD of low-stress silicon nitride [23] and LPCVD poly-silicon [32] have these characteristics and were investigated (see Table III). For low-stress silicon–nitride layers with a thickness larger than 2.5 μm and a layout with a high structure density, we observed a permanent deformation of the wafer, which made further lithographic processing very difficult. The internal stress of the silicon–nitride layer can be controlled by the ratio of the precursors for LPCVD, viz. SiH_2Cl_2 and NH_3. According to [23], a precursor ratio $SiH_2Cl_2 : NH_3$ of seven will have a residual stress close to zero and should, therefore, be ideal for filling trenches. However, it is our experience that for such a process, the LPCVD equipment requires more frequent maintenance, due to heavy deposition of reaction products on reactor walls. LPCVD poly silicon is, therefore, a better choice since it also can be deposited with low residual stress, which may be reduced even further by annealing processes [32]. Another advantage of poly silicon over silicon nitride is the fact that it allows integration of a second buried structure (see Section III) because

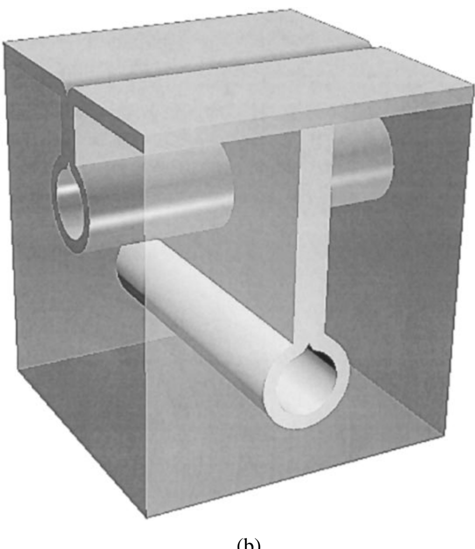
TABLE III
PROCESS PARAMETERS AND MATERIAL PROPERTIES OF LPCVD SILICON NITRIDE AND POLY-Si USING A TEMPRESS LPCVD REACTOR

Parameter	*'low-stress' Si_xN_y*	*Poly-silicon*
Gases (100 %)	$SiH_2Cl_2 : NH_3$	SiH_4
Gas flow ratio (sccm)	70 : 18	50
Deposition temperature (°C)	850	590
Pressure (mTorr)	200	250
Deposition rate (nm/min.)	8.3	4.48
Maximum layer thickness# (µm)	2.5	5
Stress (MPa)	300	very low
Etching rate (in step 6) (µm/min)	0.01-0.05	1-5

the maximum thickness is the layer thickness that can be deposited in an acceptable time, e.g. one day.

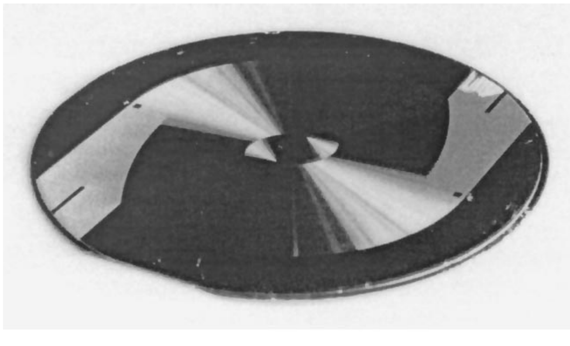


(a)

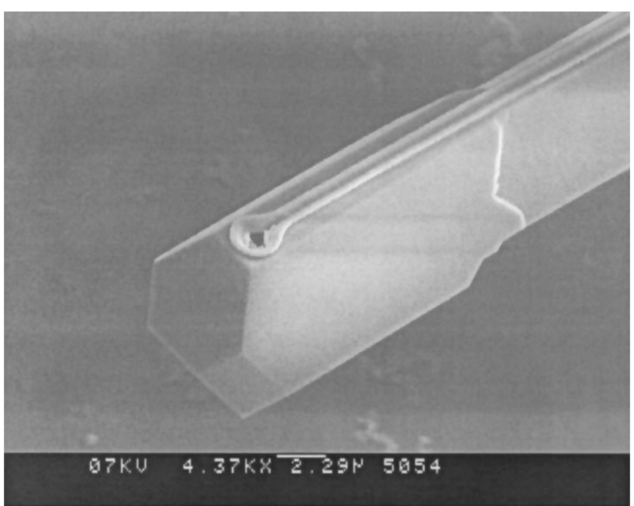


(b)

Fig. 8. (a) Impression of a cavity connected to a buried fluidic channel. The vertical channel might also serve as an opening for capillary connection. (b) Crossing buried channels.



(a)



(b)

Fig. 9. (a) 10-m long spiral-shaped channel with a diameter of 30 μm. (b) Freestanding micropipette made by process scheme 4 using the V-groove surface method of Fig. 2.

it has nearly the same etch rate as bulk silicon in an isotropic etchant like HF-HNO_3 or DRIE. After filling the trench with poly silicon, we observed a perfect seal and no deformation or bending of the wafer.

III. Demonstrators

With the procedures presented in this paper, it is possible to construct many different structures that are relevant for microfluidic systems, like cavities that may serve as reaction chambers or as containers for reactants [see Fig. 8(a)], or crossing channels [see Fig. 8(b)]. For the latter, a sequence of BCT runs has to be applied. Since the etch rate of silicon nitride is very low in most of the etching media that have been discussed here, the deepest structures, which for obvious reasons have to be fabricated first, will have to be sealed with a different material, e.g., with poly-silicon (see Section III).

Another example of a structure fabricated with BCT, i.e., a spiral-shaped channel with a length of 10 m and a diameter of 30 μm, developed for an application in gas chromatography, is shown in Fig. 9(a). The channel is constructed with the aid of process scheme 3. Connectors with a diameter of 300 μm were integrated by multiple-run BCT. The BCT process leaves room for

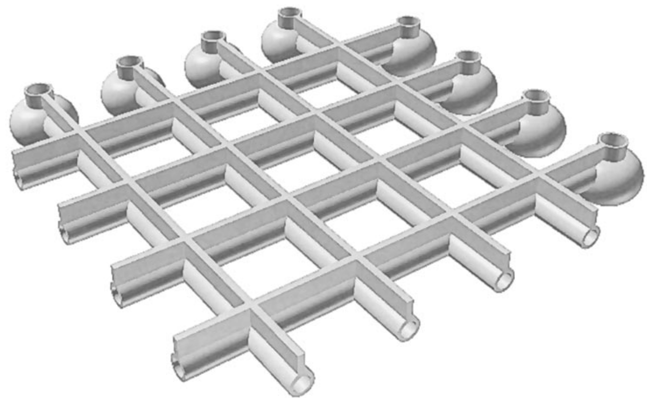


Fig. 10. Array of parallel microreactors consisting of a channel network with capillary connector openings. Such a layout may be useful as a synthesizer in combinatorial chemistry.

the integration of other components that may be required for the development of a complete lab-on-chip, like injectors, filters, and heating elements. Electronic circuitry might also be integrated, although this may require some additional polishing steps to improve the flatness of the substrate surface, but this is not an insurmountable problem, since chemical mechanical polishing steps are common practice in integrated circuit (IC) technology today.

As another example of the feasibility of BCT, Fig. 9(b) shows a freestanding micropipette, made of silicon nitride, to be used for DNA research [33]. The pipette is constructed with process scheme 1 and has a freestanding length of 100 μm with an inside diameter of 3 μm and a entrance diameter of 1 μm. Connector holes and channels were integrated, using one- run BCT. Another application of freestanding capillaries made of silicon nitride or silicon dioxide is capillary zone electrophoresis [34]. Fig. 10 shows an artist impression of a micro reactor system consisting of a network of channels with connectors, that can be fabricated in a single-run BCT process. The diameter of the channels can be downscaled to a few micrometers and may be used, e.g., in the field of combinatorial chemistry and high-throughput screening of leads in pharmaceutical research.

IV. Conclusion

A new method, called BCT, to fabricate micro structures like channels, cavities, and connector holes in bulk silicon, is presented in this paper. Due to the recent developments in deep silicon trench etching with the aid of advanced RIE systems, very narrow structures can be etched in the bulk of silicon substrates, and these trenches are the basis for the fabrication of buried channels. BCT is a process that can be used to fabricate complete micro channels in a single wafer with only one lithographic mask and processing on one side of the wafer, without the need for assembly and bonding. The process leaves a substrate surface with little topography, which easily allows further processing, like the integration of electronic circuits or solid-state sensors. The material surface inside the channel is uniform and reproducible. The buried channels are intrinsically nontransparent because they are embedded in a silicon substrate. However, freestanding optically transparent structures become possible if the buried structures are coated with silicon nitride or silicon dioxide and, subsequently, released by removal of the

substrate material that surrounds the channels. Feasible applications of buried micro channels may be inkjet nozzles, microcoolers, microreactors, and miniaturized chemical analysis systems. A column structure, which may be used in a gas chromatograph, and freestanding micro capillaries, which are suitable for DNA research, were demonstrated.

ACKNOWLEDGMENT

The authors would like to thank the S&A Staff, MESA Clean Room, University of Twente, Enschede, The Netherlands, for their assistance, R. van 't Oever for fruitful discussions, H. Hassink for making the artist impressions, and M. van Doesburg for writing the program to generate chromatography column patterns.

REFERENCES

[1] M. Elwenspoek, T. S. J. Lammerink, R. Miyake, and J. H. J. Fluitman, "Toward integrated micro liquid handling systems," *J. Micromech. Microeng.*, vol. 4, pp. 227–245, 1994.

[2] S. C. Terry, J. J. Jerman, and J. B. Angell, "A gas-chromatographic air analyzer fabricated on a silicon wafer," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 1880–1886, Dec. 1979.

[3] A. Manz, Y. Miyahara, J. Miura, Y. Watanabe, H. Miyagi, and K. Sato, "Design of an open-tubular column liquid chromatograph using silicon chip technology," *Sens. Actuators*, vol. 1, pp. 249–255, 1990.

[4] R. R. Reston and E. S. Kolesar, Jr., "Silicon micromachined gas chromatography system used to separate and detect ammonia and nitrogen dioxide—Part I: Design, fabrication, and integration of the gas chromatography system," *IEEE J. Microelectromech. Syst.*, vol. 3, pp. 134–146, Dec. 1994.

[5] R. Srinivasan, I.-M. Hsing, P. E. Berger, K. F. Jensen, S. L. Firebaugh, M. A. Schmidt, M. P. Harold, J. J. Lerou, and J. F. Ryley, "Micromachined reactors for catalytic partial oxidation reactions," *Amer. Inst. Chem. Eng. J.*, vol. 43, no. 11, pp. 3059–3069, 1997.

[6] A. Weisberg, H. M. Bau, and J. N. Zemel, "Analysis of microchannels for integrated cooling," *Int. J. Heat Mass Transf.*, vol. 35, pp. 2465–2473, 1992.

[7] K. E. Petersen, "Silicon as a mechanical material," *IEEE Trans. Electron Devices*, vol. ED-70, pp. 420–457, May 1982.

[8] D. J. Harrison, K. Fluri, K. Seiler, Z. Fan, C. S. Effenhauser, and A. Manz, "Micromachining a miniaturized capillary electrophoresis-based chemical analysis system on a chip," *Science*, vol. 261, pp. 895–896, 1993.

[9] S. C. Jacobson, R. Hergenröder, L. B. Koutny, R. J. Warmack, and J. M. Ramsey, "Effects of injection schemes and column geometry on the performance of microchip electrophoresis devices," *Anal. Chem.*, vol. 66, pp. 1107–1113, 1994.

[10] A. T. Woolley and R. A. Mathies, "Ultra-high-speed DNA fragment separations using microfabricated capillary array electrophoresis chips," *Proc. Nat. Academy Sci.*, vol. 91, pp. 11 348–11 352, 1994.

[11] A. Manz, E. Verpoorte, C. S. Effenhauser, N. Burggraf, D. E. Raymond, and H. M. Widmer, "Planar chip technology for capillary electrophoresis," *Fresenius J. Anal. Chem.*, vol. 348, pp. 567–571, 1994.

[12] R. W. Tjerkstra, M. J. de Boer, J. W. Berenschot, J. G. E. Gardeniers, M. C. Elwenspoek, and A. van den Berg, "Etching technology for microchannels," in *Proc. IEEE MEMS Workshop*, Nagoya, Japan, Jan. 26–30, 1997, pp. 147–152.

[13] R. T. Howe, "Surface micromachining for micro sensors and micro actuators," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. B6, pp. 1809–1813, 1988.

[14] K. A. Shaw, Z. L. Zhang, and N. C. MacDonal, "SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures," *Sens. Actuators*, vol. 40, pp. 63–70, 1994.

[15] H. F. Winters, J. W. Coburn, and T. J. Chuang, "Surface processes in plasma-assisted etching environments," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 1, pp. 469–480, 1983.

[16] J. Branebjerg, C. J. M. Eijkel, J. G. E. Gardeniers, and F. C. M. van de Pol, "Dopant selective HF anodic etching of silicon for the realization of low-doped monocrystalline silicon micro structures," in *Proc. IEEE MEMS Workshop*, Nara, Japan, Feb. 2, 1991, pp. 221–226.

[17] B. Schwartz and H. Robbins, "Chemical etching of silicon IV: Etching technology," *J. Electrochem. Soc.*, vol. 123, pp. 1903–1909, 1976.

[18] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic etching of crystalline silicon in alkaline solutions; I Orientation dependence and behavior of passivation layers," *J. Electrochem. Soc.*, vol. 137, pp. 3612–3622, 1990.

[19] H. Jansen, M. de Boer, H. Wensink, B. Kloeck, and M. Elwenspoek, "The black silicon method VIII: A study of the performance of etching silicon using SF_6/O_2-based chemistry with cryogenically wafer cooling and a high density ICP source," IEEE J. Microelectromech. Syst., 1999, submitted for publication.

[20] H. V. Jansen, M. J. de Boer, R. Wiegerink, N. Tas, E. J. T. Smulders, C. Neagu, and M. C. Elwenspoek, "RIE lag in high aspect ratio trench etching of silicon," *Microelectron. Eng.*, vol. 35, pp. 45–50, 1997.

[21] H. Wensink, M. J. de Boer, R. J. Wiegerink, R. A. F. Zwijze, and M. C. Elwenspoek, "First micromachined silicon load cell for loads up 1000 kg," in *Proc. SPIE Conf. Micromachined Devices Comp. IV*, Santa Clara, CA, Sept. 20–24, 1998, pp. 424–430.

[22] H. V. Jansen, M. J. de Boer, R. Legtenberg, and M. C. Elwenspoek, "The black silicon method: A universal method for determining the parameter setting of a fluorine based reactive ion etcher in deep silicon trench etching with profile control," *J. Micromech. Microeng.*, vol. 5, pp. 115–120, 1995.

[23] J. G. E. Gardeniers, H. A. C. Tilmans, and C. G. C. Visser, "LPCVD silicon-rich silicon nitride films for applications in micromechanics, studied with statistical experimental design," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 14, pp. 2879–2892, 1996.

[24] S. Rojas, A. Modelli, and W. S. Wu, "Properties of silicon dioxide films prepared by low-pressure chemical vapor deposition from tetraethylorthosilicate," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 8, pp. 1177–1184, 1990.

[25] H. F. Winter, "Phenomena produced by ion bombardment in plasma-assisted etching environments," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 6, pp. 1997–2000, 1988.

[26] J. Liu, L. Huppert, and H. H. Sawin, "Ion bombardment in r.f. plasmas," *J. Appl. Phys.*, vol. 68, pp. 3916–3934, 1990.

[27] A. Manenschijn and W. J. Goedheer, "Angular ion and neutral energy distribution in a collisional r.f.-sheath," *J. Appl. Phys.*, vol. 69, pp. 2923–2930, 1991.

[28] *Handbook of Plasma Etching Technology: Fundamentals, Etching, Deposition, and Surface Interactions*, S. M. Rossnagel, Ed., Noyes, Park Ridge, NJ, 1990.

[29] J. C. Arnold and H. H. Sawin, "Charging of pattern features during plasma etching," *J. Appl. Phys.*, vol. 70, pp. 5314–5317, 1991.

[30] H. V. Jansen, J. G. E. Gardeniers, M. J. de Boer, M. C. Elwenspoek, and J. H. J. Fluitman, "A survey on the reactive ion etching of silicon in microtechnology," *J. Micromech. Microeng.*, vol. 6, pp. 14–28, 1996.

[31] M. Elwenspoek, U. Lindberg, H. Kok, and L. Smith, "Wet chemical etching mechanism of silicon," in *Proc. IEEE MEMS Workshop*, Oiso, Japan, Jan. 25–28, 1994, pp. 223–228.

[32] T. Kamins, *Polycrystalline Silicon for Integrated Circuits and Displays*. Norwell, MA: Kluwer, 1998.

[33] C. Rusu, R. van't Oever, M. de Boer, H. Jansen, E. Berenschot, M. L. Bennink, J. S. Kanger, B. G. de Brooth, M. Elwenspock, J. Greve, A. van den Berg, and J. Brugger, "Fabrication of micromachined pipettes in a flow channel for single molecule handling of DNA," in *Proc. IEEE MEMS Conf.*, Miyazaki, Japan, Jan. 23–27, 2000.

[34] Y. Fintschenko and A. van den Berg, "Silicon microtechnology and micro structures in separation science," *J. Chromatography A*, vol. 819, pp. 3–12, 1998.

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