Improvements of Deposited Interpolysilicon Dielectric Characteristics with RTP N_2O-Anneal

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Abstract— **Nitridation of deposited instead of thermally grown oxides was studied to form high-quality inter-polysilicon dielectric layers for nonvolatile memories. It was found that by optimizing the texture and morphology of the polysilicon layers, and by optimizing the post-dielectric deposition-anneal, very high-quality dielectric layers can be obtained. In this paper, it is shown that not only for deposited gate oxides, but also for deposited inter-polysilicon oxides, rapid thermal annealing leads to previously unpublished improved electrical characteristics, like high charge to breakdown ($Q_{bd} \approx 20$ C/cm^2) and lower leakage currents. Moreover, the annealed dielectrics had less electron trapping when stressed.**

I. Introduction

THE main purpose of this research is to develop a deposited dielectric layer, which can be used as an interpolysilicon dielectric in nonvolatile memories. Conventional interpoly oxides are thermally grown (polyoxides) at very high temperatures. Thermal oxidation of silicon leads to roughening, which cause larger electric fields resulting in low-field tunneling processes and poor data retention. Recently [1], improvements have been shown with interpoly dielectrics thermally grown in pure N_2O. By using deposited instead of thermally grown dielectrics, even more reliable dielectrics can be grown since defects present in the silicon are not incorporated in the deposited layer, and the surface of the polysilicon layer is not roughened (no silicon consumption). This has already been shown for thicker dielectrics [2], but in this paper it is also proven for thinner dielectric layers (≈25 nm). Since as-deposited oxides are not as dense as thermally grown oxides and cause many traps, after-treatments like N_2O annealing are needed to obtain desired electrical characteristics. In [3] and [4], it is shown that N_2O annealing leads to large improvements of oxide layers, which is thought to derive from its incorporation of nitrogen at the oxide-silicon interface. In our application, i.e., the embedded vertical injection punchthrough-based metal oxide semiconductor (VIPMOS) EEPROM [5], erasing is performed by interpoly tunneling. Conflicting demands on the interpoly dielectric exist, namely good data retention (very low leakage currents) for low and moderate applied voltages and good tunneling characteristics for high voltages. This letter reports on deposited interpolysilicon dielectric layers, annealed in N_2O ambient, which can replace polyoxides as interpoly dielectric. It was found that this dielectric has very desirable qualities such as very high charge to breakdown (Q_{bd}) and very low charge trapping. An extra advantage is the low thermal budget which is very attractive for embedded application. It was also remarkable that the J–E characteristics had a reverse preference in polarity, such as a lower leakage current and a higher Q_{bd} when the top electrode was positively biased, which also has been observed for thermally grown N_2O oxides [1].

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II. Experiments

P-type wafers were thermally oxidized to a thickness of 100 nm. Then a 300 nm silicon film (poly 1) with a very flat surface [6] was deposited by means of low-pressure chemical vapor deposition (LPCVD) at 550°C and implanted with phosphorus up to a dose of 8×10^{15} cm^{-2} at 50 keV. The wafers were annealed for 30 min in N_2 ambient to activate the dopant. Then a 25 nm thick dielectric layer was deposited, which consisted of HTO from SiH_2Cl_2 and N_2O at 800°C. This layer simultaneously serves as gate and interpoly dielectric. It was annealed in a rapid thermal processor in N_2O ambient at 950°C for 20 min. For comparison, dielectric layers without annealing were also processed. A second silicon layer (poly 2) of 300 nm was then deposited by means of LPCVD at 625°C. This film was implanted with arsenic up to a dose of 6×10^{15} cm^{-2} at 100 keV. After defining poly 2, all samples received a 200 nm thick CVD oxide as a passivation layer. Contact holes were opened and Al was deposited and patterned to form the capacitor structures. Finally, all devices were sintered at 400°C for 30 min in wet N_2 ambient.

III. Results and Discussion

Due to the rapid thermal N_2O annealing, the dielectric thickness of the interpoly dielectrics increased by about 5% to 260 Å (measured by ellipsometry). Typical J–E curves of N_2O annealed dielectrics are shown in Fig. 1 along with those of as-deposited dielectric layers. It can be seen that the N_2O annealed dielectrics conducted a lower leakage current and started conducting at higher voltages than the as-deposited dielectric when the top electrode (poly 2) was positively biased. Also, a higher breakdown field was observed for the annealed dielectrics.

Fig. 2 shows typical Q_{bd} plots of the samples, from which also the trapping behavior can be determined. The capacitor area was 1×10^{-4} cm^2 and the stress condition was

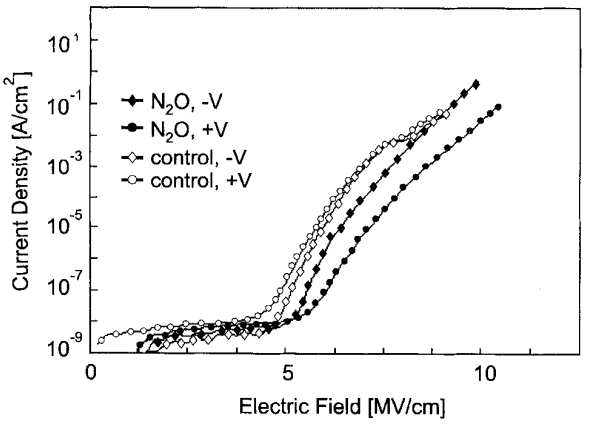

Fig. 1. Typical J–E characteristics of as-deposited and N_2O annealed interpolysilicon dielectric layers under positive and negative applied voltages. The dielectric thickness of all capacitor structures was 25 nm.

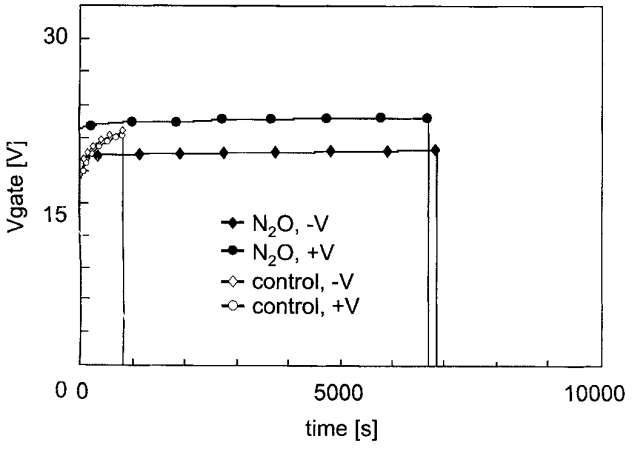

Fig. 2. Typical Q_{BD} characteristics of the as-deposited and N_2O annealed interpolysilicon dielectric layers under positive and negative constant current stress of 2.5 mA/cm^2. The area of the capacitors was 1×10^{-4} cm^2.

2.5 mA/cm^2 constant current injection for both positive and negative bias. It can be seen that the N_2O annealed dielectrics had a much higher Q_{bd} and a much smaller voltage shift (ΔV) than the as-deposited dielectric. This implies that the N_2O annealed dielectric trapped fewer electrons. The N_2O annealed dielectric had slightly different voltage shifts for positive and negative bias, which is ascribed to the nitrogen peak (observed by means of Auger measurements) at the Si–SiO_2 interface. However, when we look at the as-deposited dielectric layers, Q_{BD} results are still very attractive as interpolysilicon dielectric in comparison with interpolysilicon dielectric layers, which were directly grown in N_2O ambient [1].

Fig. 3 shows the Weibull charge to breakdown plot for 100 capacitors under 2.5 mA/cm^2 stress. It is shown that the N_2O annealed dielectric has the largest Q_{bd} with a very narrow distribution. This improvement is due to the reduced electron trapping (as was shown in Fig. 2, where a much lower

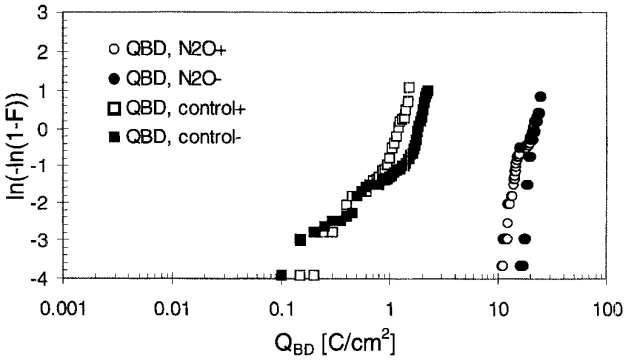

Fig. 3. Typical Weibull plots of the Q_{BD} (charge to breakdown) for the as-deposited and N_2O annealed dielectric layers under positive and negative stress. A constant current density of 2.5 mA/cm^2 was applied to capacitors with an area of 1×10^{-4} cm^{-2}.

ΔV occurred during constant current stress). The as-deposited layers have a broader distribution. The reverse preference in polarity of the J–E characteristics between the N_2O annealed and as-deposited dielectric layer is also remarkable.

IV. Conclusion

In conclusion, the above results show that deposited oxides with additional N_2O anneal are a very attractive alternative for replacing polyoxides as interpoly dielectric for non volatile memory application. Due to the low thermal budget they are very attractive for embedded applications. It has desirable low leakage currents and high E_{bd} for top electrode electron injection, reduced electron trapping (due to the nitrogen incorporation) and a much larger charge to breakdown (Q_{bd}) than the as deposited variant.

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