

# Output Impedance Shaping for Frequency Compensation of MOS Audio Power Amplifiers

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**Abstract**—A frequency compensation technique for MOS audio power amplifiers is presented that allows the frequency compensation capacitors around the power transistors to be smaller than the circuit parasitics without power or stability penalty. Stability is analysed by inspecting the output impedance of the closed loop amplifier, instead of the traditional open-loop gain. By degenerating the gain of the penultimate stage, the output impedance is shaped such that the stability of the audio amplifier is guaranteed for complex loudspeaker loads. The realized amplifier features a THD of 0.005% @ (1 kHz, 10 W), an SNR of 110 dB(A), and stable operation for any passive load up to 50 nF.

**Index Terms**—Audio amplifiers, frequency compensation, Miller compensation, multistage amplifiers, output impedance, power amplifiers.

## I. INTRODUCTION

AUDIO signal processing is increasingly digital, which has led to ever larger dynamic range and tougher distortion requirements. The loudspeaker, however, is still driven by an analog voltage, either by a switching amplifier or a linear amplifier. From an efficiency point of view, switching amplifiers are preferred, but linear amplifiers are still superior in terms of frequency response, integration level and ease of application. But even though linear audio power amplifiers have been around for a long time, the frequency compensation design methodology is not well established.

The design of integrated audio amplifiers has many similarities to general OPAMP design. A low distortion is required, the amplifier needs to be stable for a wide load range, and external stabilization networks -as often used in discrete audio amplifiers- are not acceptable. Frequency compensation schemes for opamps range from traditional Miller compensation to a myriad of alternatives that promise a better trade-off between power consumption, bandwidth and stability [1]–[9]. There are two problems, though, that limit the applicability in the case of audio power amplifiers.

The first issue is that all techniques assume compensation capacitors that are larger than the circuit parasitics [1]–[9]. In audio power amplifiers, however, most of the chip area is occupied by the power transistors, so any compensation capacitor is in fact much smaller than the power transistor's gate-source capacitance. In most cases, the largest compensation capacitor that can be used, is the parasitic gate-drain capacitance ( $C_{ds}$ )

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of the power transistor, which is typically several times smaller than the gate-source capacitance ( $C_{gs}$ ). Although pole splitting still occurs, the achievable bandwidth is reduced and distortion increases.

Another problem lies in the difficulty to assess the suitability of frequency compensation strategies for complex loads. Because the stability of an amplifier is usually derived from its open-loop frequency transfer, the analysis for all possible loads would become very complex. Consequently, the load is usually assumed to be fixed [1]–[4], partly variable [5]–[7] or capacitive in a certain range [8], [9]. This does not provide a full picture of the behavior of the amplifier for complex loads, which is a necessity for audio amplifiers due to the very wide impedance range of real-life loudspeakers [10].

To solve both these issues, we propose a modification to Nested Miller Compensation (NMC) such that we can use compensation capacitors that are smaller than the power transistor parasitics without sacrificing bandwidth or power. We arrive at this result by using an output impedance shaping technique. Adding to [11], we will present a more thorough discussion of this technique, including the mathematics behind it. We will show how this technique reduces mathematical complexity compared to open-loop analysis, and how it gives insight and information about stability for all complex loads. Also, the amplifier is discussed in more detail.

The outline of the paper is as follows: In Section II, the use of output impedance analysis is motivated. Subsequently, in Section III, the output impedance is shaped to design the frequency compensation topology of a MOS audio power amplifier. Sections IV and V discuss the realization and measurements, with conclusions in Section VI.

## II. OUTPUT IMPEDANCE ANALYSIS

### A. Stability

For power amplifiers with varying loads, traditional analysis of the open loop frequency transfer becomes extremely complicated. Alternatively, analysis of the closed-loop output impedance offers several advantages. Refer to Fig. 1 for a classic two-stage Miller compensated opamp in unity-gain feedback and its corresponding closed-loop output impedance. Also sketched in Fig. 1 is the impedance of a possible load capacitor  $C_{load}$ .

An intuitive approach to assess the stability is to notice that the output impedance is almost purely inductive at the frequency where the load is purely capacitive, forming a resonant tank that causes peaking in the frequency response. Also, neither very small, nor very large  $C_{load}$  will cause problems, as  $1/sC_{load}$  will intersect a resistive  $Z_{out}$  in the far right and far left of the

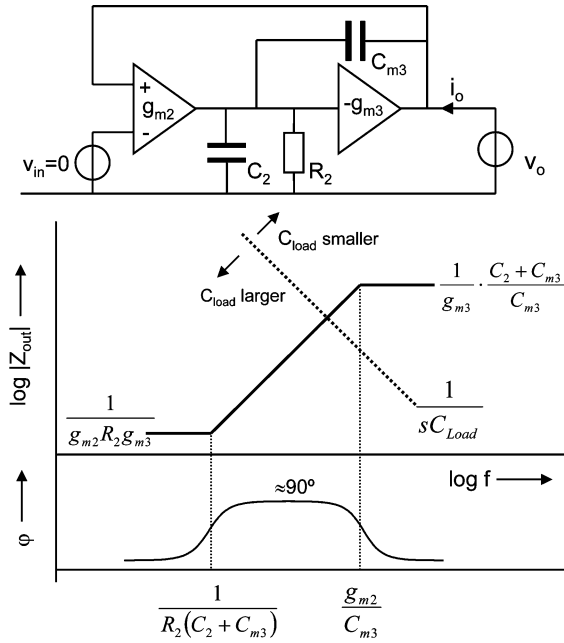


Fig. 1. Output impedance of a 2-stage Miller compensated OPAMP.

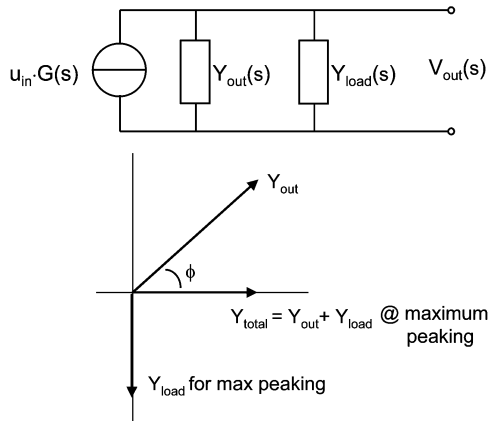


Fig. 2. Norton equivalent of amplifier with output admittance plot.

plot, respectively. This is in line with common knowledge about a Miller-compensated opamp [8], and serves as an illustration of how easy this can be evaluated from  $Z_{out}$ .

To address the issue more quantitatively, let us first ease the analysis by representing the amplifier by a current source with parallel admittances, as shown in Fig. 2. The unloaded amplifier frequency response is  $G(s)/Y_{out}(s)$ . By connecting a load, this changes to  $G(s)/(Y_{out}(s) + Y_{load}(s))$ . If  $|Y_{out} + Y_{load}|$  is smaller than  $|Y_{out}|$ , peaking occurs. A special case is  $Y_{out} + Y_{load} = 0$ , where an input signal is no longer necessary to achieve an output signal, commonly referred to as oscillation. This is only possible if  $\text{Re}(Y_{out}(s)) \leq 0$  for some frequency. In that case, there is always a passive load  $Y_{load} = -Y_{out}$  that can cause the amplifier to oscillate.

For  $\text{Re}(Y_{out}(s)) > 0$ , the amplifier is stable for passive loads, but peaking in the frequency response is possible. Maximum peaking is obtained by minimizing the total admittance  $|Y_{total}| = |Y_{out} + Y_{load}|$ . Given the fact that  $\text{Re}(Y_{load}) > 0$

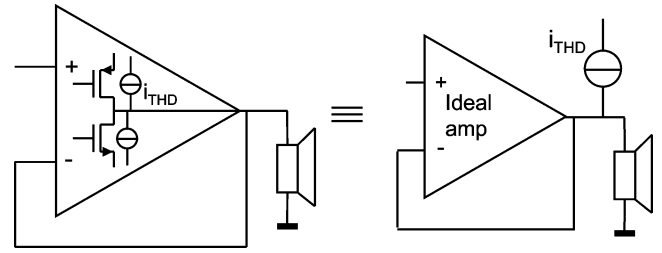


Fig. 3. Distortion modeling.

for any passive load, it quickly becomes clear from Fig. 2 that minimum  $Y_{total} = Y_{min} = \text{Re}(Y_{out}) = |Y_{out}| \cos(\arg(Y_{out}))$ . Since  $\arg(Y_{out}) = -\arg(Z_{out})$  and  $\cos(\phi) = \cos(-\phi)$ , we can rewrite the maximum peaking compared to no load to

$$\text{Maximum peaking} = 20 \log \left( \frac{1}{\cos(\phi)} \right) \text{ [dB]},$$

$$\text{with } \phi = \arg(Z_{out}) \in \left[ -\frac{1}{2}\pi, \frac{1}{2}\pi \right]. \quad (1)$$

### B. Distortion

Another property that can directly be derived from  $Z_{out}$  is the distortion. Most of the distortion in audio power amplifiers is generated by the strong non-linearity of the common-source class-AB biased power transistors. In quiescent, or for small output currents, they operate in weak inversion. For larger output currents they operate in saturated strong inversion, and at the onset of clipping, when the output voltage is near the supply rails, they operate in the linear region. Since this non-linearity is mostly determined by the output voltage and load, we can model the distortion as a distortion current source parallel to the output transistors. As shown in Fig. 3, we can move this THD source outside the amplifier, and conclude that lower closed loop  $Z_{out}$  in the audio band means lower distortion.

## III. OUTPUT IMPEDANCE SHAPING

We will now actively use  $Z_{out}$  in our design procedure to deal with stability and distortion in relation to the limited compensation capacitors in a MOS power amplifier.

### A. Small $C_m$

To clarify the issue with a limited Miller capacitance  $C_m$ , refer to Fig. 1 again. Suppose we decrease  $C_{m3}$  compared to Fig. 1. This means that the high frequency output impedance  $1/g_{m3} * (1 + C_2/C_{m3})$  increases, as well as the pole  $g_{m2}/C_{m3}$  of  $Z_{out}$ . Consequently, the inductive behavior of  $Z_{out}$  extends to a much higher frequency, meaning that instability is reached for smaller load capacitances than originally. To avoid this unwanted effect, we have two options. The first is to increase  $g_{m3}$ , but this comes at the expense of power consumption. The second option is to keep  $g_{m2}/C_{m3}$  at the same frequency. This means the whole  $Z_{out}$  curve shifts up, which leads to a higher distortion. We would like to find a better solution to this trade-off between  $C_m$ , power, distortion and stability.

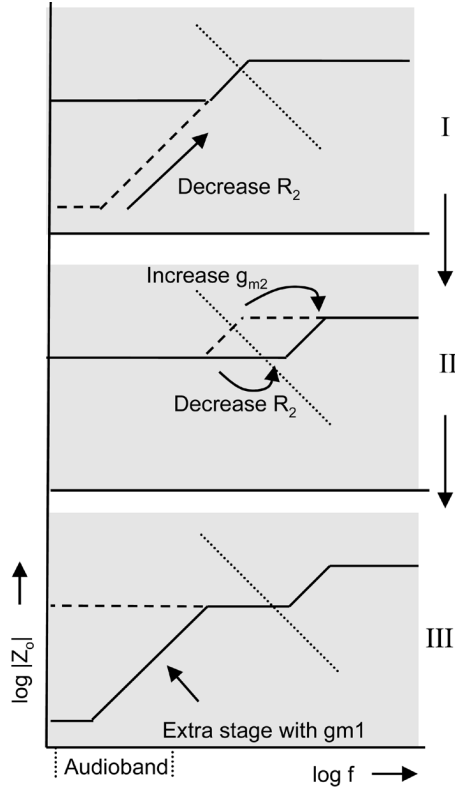


Fig. 4. Shaping the output impedance.

### B. Gain Degeneration

Our solution starts by referring to Fig. 1 again. We decrease the value of  $R_2$  such that the zero in the  $Z_{out}$  plot moves higher, and LF  $Z_{out}$  increases. When the zero and the pole of  $Z_{out}$  are close enough together, the phase change in the frequency range in between is limited, also limiting the maximum peaking. However, the decrease of  $R_2$  has also resulted in a limited LF gain and thus high distortion. This step is shown in step I of Fig. 4. The low LF gain is overcome in [8] by using a very large  $C_m$ . We propose to still use our small  $C_m$ , and decrease  $R_2$  even further while at the same time increasing  $g_{m2}$  (step II in Fig. 4). Finally, we add an extra stage  $g_{m1}$  in front (step III in Fig. 4). Fig. 5 displays the resulting topology. We will discuss the implications of these steps after the following mathematical analysis.

To calculate  $Z_{out}$  in Fig. 5, we neglect the direct contribution of  $C_{m3}$  and  $C_{m2}$  to the output impedance. Since they are small, this is reasonable to assume. Further below we will show that this assumption does not lead to large deviations between calculations and measurements. This yields (2), shown at the bottom of the page.

To get a simple expression for the poles, we assume that  $g_{m1}R_1 \gg 1$  and  $C_{m2} \gg C_1$ . The first assumption says that the DC-gain of the first stage is considerably larger than 1, which

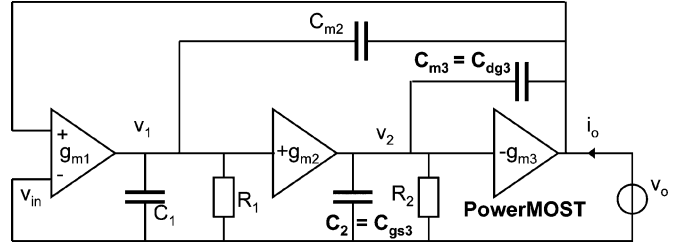


Fig. 5. NMC with low  $R_2$ .

will usually be the case. The second assumption is also easy to satisfy, since  $C_1$ , being the input capacitance of the second stage, is small compared to the much larger capacitances of the final stage. The resulting pole and zero locations of the output impedance are then as follows:

$$\begin{aligned} z_1 &= -\frac{1}{R_1(C_1 + C_{m2})} & z_2 &= -\frac{1}{R_2(C_2 + C_{m3})} \\ p_1 &= -\frac{g_{m2}}{2C_{m3}} \left( 1 + \sqrt{1 - 4\frac{g_{m1}C_{m3}}{g_{m2}C_{m2}}} \right) \\ p_2 &= -\frac{g_{m2}}{2C_{m3}} \left( 1 - \sqrt{1 - 4\frac{g_{m1}C_{m3}}{g_{m2}C_{m2}}} \right). \end{aligned} \quad (3)$$

The crucial aspect of our solution, as discussed above, was to decrease  $R_2$  while increasing  $g_{m2}$ . By increasing  $g_{m2}$  such that  $g_{m2}/C_{m3} \gg g_{m1}/C_{m2}$ , in other words, making the unity-gain frequency (UGF) of the inner loop much larger than the UGF of the outer loop, the pole locations can be approximated with a Taylor expansion and become

$$p_1 = -\frac{g_{m2}}{C_{m3}} \quad p_2 = -\frac{g_{m1}}{C_{m2}}.$$

The resulting output impedance is shown in Fig. 6. As a reference, the output impedance of the original two-stage OPAMP with only  $g_{m2}$  and  $g_{m3}$  is plotted as a dashed line.

To assess the result, let us first consider a very small capacitive load  $C_{L1}$  in Fig. 6. It intersects an almost real output impedance in region I, so for a small load capacitance the amplifier is stable. When  $C_L$  is increased, it will cross the output impedance in an inductive part (II). This constitutes a resonant circuit at that frequency, leading to peaking in the frequency response. The amount of peaking, according to (1), is determined by the maximum phase of  $Z_{out}$  in region II, which is determined by the ratio between the zero and pole that form the borders of region II. This distance is equal to a factor  $g_{m2}R_2(C_2 + C_{m3})/C_{m3}$ , and since  $C_{m3} = C_{dg3} = 20$  pF and  $C_2 = C_{gs3} = 80$  pF are determined by the power transistor, we have  $g_{m2}R_2$  as design freedom. We chose  $g_{m2}R_2 = 1$ , since this is easy to realize as a source follower in the final schematic. It leads to a pole/zero

$$Z_{out} = \frac{v_o}{i_o} = \frac{(1 + sR_1(C_1 + C_{m2}))(1 + sR_2(C_2 + C_{m3}))}{g_{m2}g_{m3}R_1R_2(g_{m1} + sC_{m2}) + g_{m3}R_2sC_{m3}(1 + sR_1(C_1 + C_{m2}))} \quad (2)$$

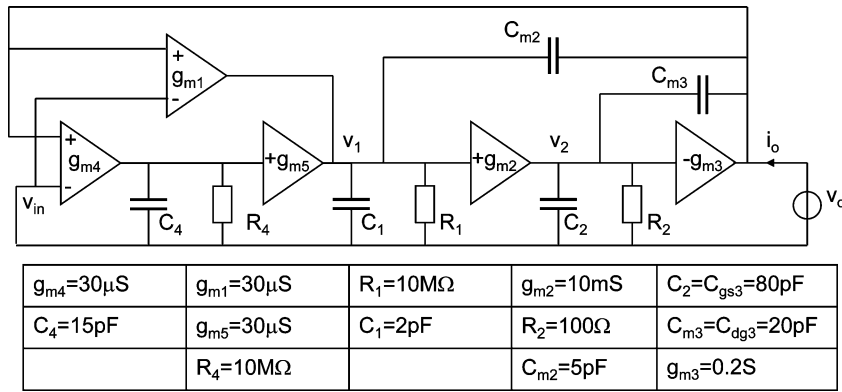
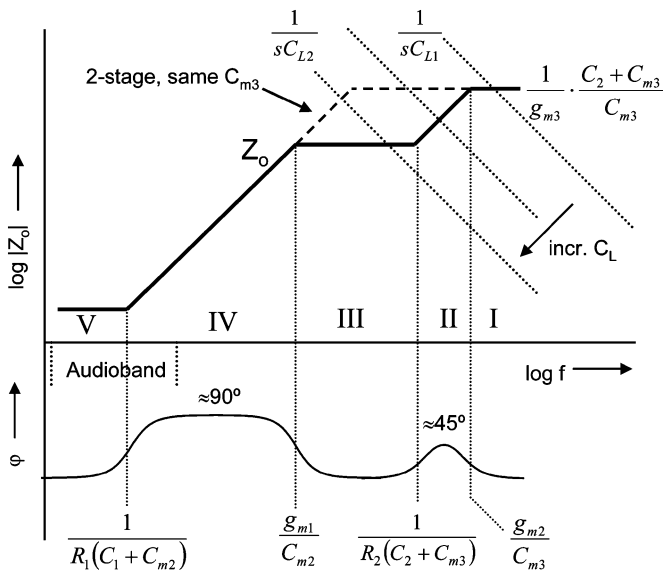

 Fig. 7. Frequency compensation model after adding  $g_{m4,5}$ .


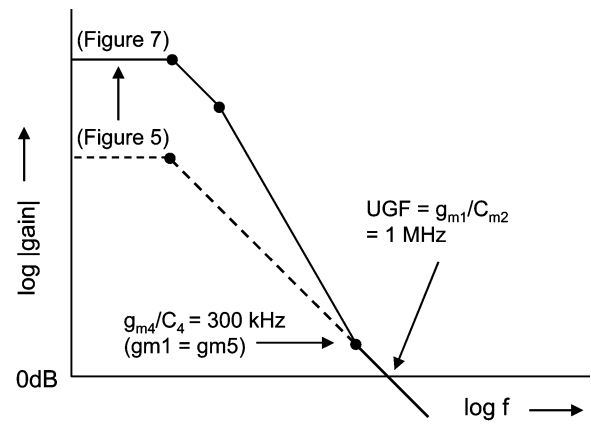
Fig. 6. Output impedance of Fig. 5.

ratio of 5, which gives a maximum phase of  $Z_o$  of  $45^\circ$ , corresponding to a maximum peaking of 3 dB according to (1).

Increasing  $C_L$  further, the system is more stable again (region III), and only for larger  $C_L$  (region IV) stability is compromised. Note that the stability of a two-stage Miller compensated opamp would already be compromised for  $C_L$  larger than  $C_{L2}$  in Fig. 6, which is the same factor of 5 lower than in our new design. Thus, we see that the load limitations imposed by a limited Miller capacitance have been overcome.

Two remarks are in place at this point. First of all, we have used a capacitive load in the reasoning above, while real loudspeakers are RLC loads. We have done this because the maximum amount of peaking for any load is described by (1), but it does not specify for which load it occurs. As illustrated in Fig. 6, the output impedance of our circuit has a positive phase, meaning that only loads with a capacitive component will cause problems, so we used  $C_L$  as worst case.

A second remark relates to  $R_2$ . Because  $R_2$  is small, one might be tempted to look at this structure as simply driving the gates of the power transistors with a low-impedance source, a kind of resistive broadbanding. It is not that simple, however, because a smaller  $C_{m3}$  would then be favorable for stability,


 Fig. 8. Increase of open loop gain by adding  $g_{m4,5}$ .

as it limits the capacitive load seen by  $g_{m2}$ . Our analysis, however, shows that a smaller  $C_{m3}$  will actually decrease the phase margin for capacitive loads in region II in Fig. 6.

### C. Extra Gain Stage

Although one could accept the topology of Fig. 5, or even degenerate the first stage gain too, to achieve stability for all capacitive loads, this is not an option here since the amplifier still has too much distortion for our purpose. An extra gain path is added in parallel to  $g_{m1}$ , consisting of  $g_{m4}$  and  $g_{m5}$  as shown in Fig. 7. This extra path is dimensioned such that it adds gain (and phase shift) only below the UGF of the open loop transfer, as shown in Fig. 8. The extra gain lowers  $Z_{out}$  in the audio band further (Fig. 9), reducing distortion. Fig. 10 shows the more classical open loop frequency response for various loads. In this case, of course, we can only analyse a limited number of loads. For loads of  $4\Omega$  or  $10\text{ k}\Omega$  in parallel to  $10\text{ pF}$  or  $10\text{ nF}$ , the phase margin stays above  $65^\circ$ , and for values in between the picture was similar.

### D. Driving the Load

Up to this point, we have assumed a constant  $g_{m3}$ , whereas in reality  $g_{m3}$  varies strongly depending on the load current and output voltage. The calculations are done for the class AB quiescence current, where  $g_{m3}$  is very low. When the power transistors carry a larger current, expression (2) shows that the  $Z_{out}$  curve in Fig. 9 simply shifts down, only improving the stability

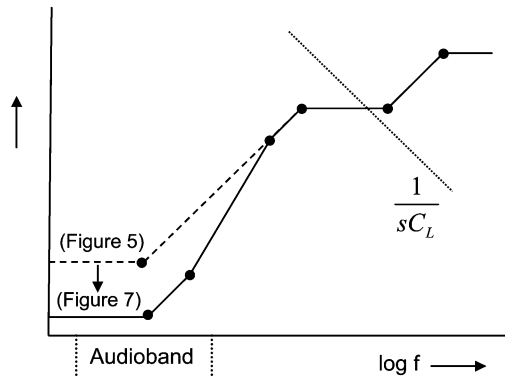
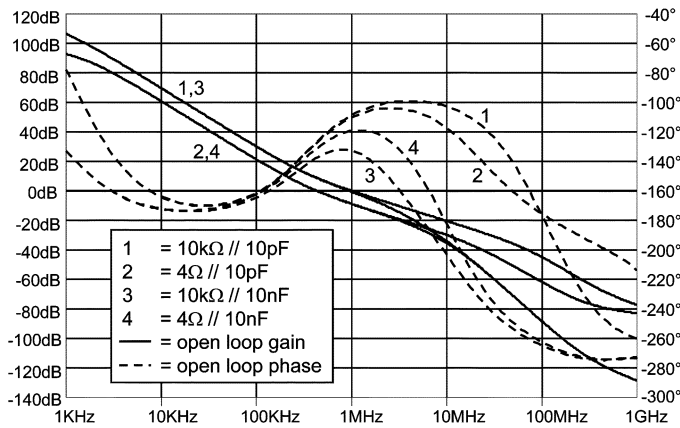
Fig. 9. Decrease of  $Z_{out}$  after adding  $g_{m4,5}$ .

Fig. 10. Open loop response of Fig. 7 for various loads.

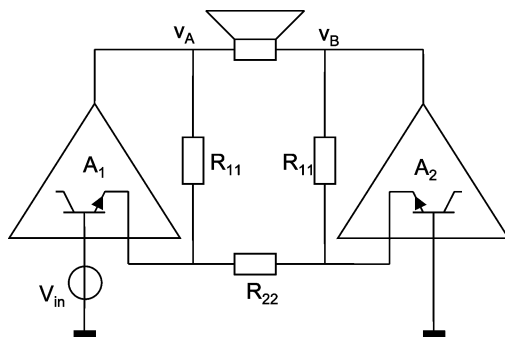


Fig. 11. Current feedback bridge configuration.

of the amplifier. Note that the analysis holds for all possible load impedances. We didn't need to assume  $g_{m3}R_L \gg 1$ , as is usually the case.

#### IV. REALIZATION

The amplifier was realized in the NXP ABCD2 process, an SOI Bipolar-CMOS-DMOS process with  $1 \mu\text{m}$  feature size. The chip is targeted as a quad channel audio amplifier for automotive applications. The four channels drive the loudspeakers in BTL mode, as shown in Fig. 11, and each bridge half has the frequency compensation setup as described above. If the bridge halves would have been equipped with standard differential pair inputs, the common-mode feedback factor would have been unity, considerably larger than the differential feedback

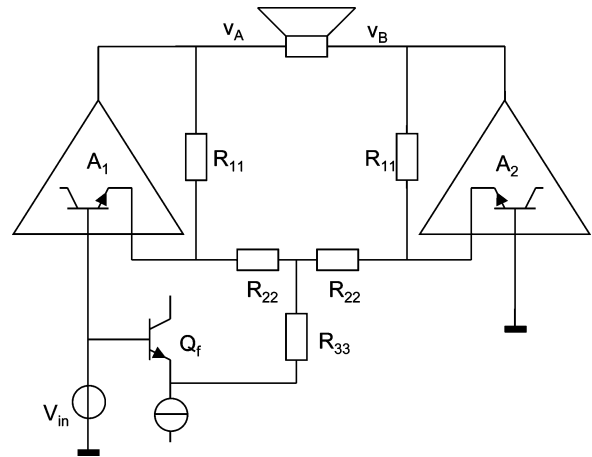


Fig. 12. Topology of one channel.

factor it is designed for, giving rise to stability problems. Using current-mode inputs ensures that the common-mode stability is the same as the differential-mode stability. As a consequence,  $g_{m1}$  and  $g_{m4}$  in Fig. 7 are set by the feedback resistors  $R_{11}$ . Unfortunately, the configuration of Fig. 11 suffers from unequal gains to the two bridge halves:  $v_A/v_{in} = 1 + R_{11}/R_{22}$  and  $v_B/v_{in} = R_{11}/R_{22}$  respectively, which causes asymmetrical clipping and consequently reduced low distortion output power. Simply changing one of the  $R_{11}$ 's is not an option because it would change stability. The solution is shown in Fig. 12, where we apply an extra signal to the "middle" of  $R_{22}$ . The gains of the two bridge halves now become

$$\begin{aligned} \frac{v_A}{v_{in}} &= 1 + \frac{R_{11}}{R_{22}} \left( \frac{R_{33}}{R_{22} + 2R_{33}} \right) \\ \text{and } \frac{v_B}{v_{in}} &= -\frac{R_{11}}{R_{22}} \left( \frac{R_{22} + R_{33}}{R_{22} + 2R_{33}} \right). \end{aligned} \quad (4)$$

For symmetrical clipping, the absolute value of the gains should be equal. From (4) it follows how  $R_{33}$  must be chosen to achieve this:  $R_{33} = (R_{11} - R_{22})/2$ . It can also be shown (although this is easy to see because of the symmetry) that the extra path has the same effect on  $v_A$  and  $v_B$ . Therefore, any distortion caused by  $Q_f$ , which works open-loop and has to drive  $R_{33}$ , only results in a common-mode term, not affecting the differential output voltage.

Fig. 13 shows a simplified circuit schematic of one bridge half, where component numbering corresponds to Fig. 7. As mentioned above, the gain  $g_{m2}R_2$  is chosen equal to 1 and realized by a source follower which behaves like  $g_{m2}R_2 \approx 1$  in the frequency range of interest. To achieve a high value of  $g_{m2}$ ,  $I_2$  must be large, but we need a large  $I_2$  anyway because of the high charge- and discharge currents of the gate of  $M_3$  during crossover and clipping. Class AB control is similar to [12]. The addition of  $M_2$  to drive  $M_3$ , however, would reduce the minimum supply voltage to  $3V_{GS} + V_{DS,sat}$ . We included  $M_{AB2}$  to reduce this value to  $2V_{GS} + 2V_{DS,sat}$ . Integration of  $M_{AB2}$  in the cross-coupled bias circuit instead of realizing it as a separate level shift reduces quiescent current spread. The quiescent current  $I_Q$  is set by the translinear loop of  $M_3$ ,  $M_2$ ,  $M_{AB2}$ ,  $M_{AB1}$  and two stacked  $V_{gs}$  (not shown) that generate  $V_{bias2}$ .  $I_Q$  of  $M_3$

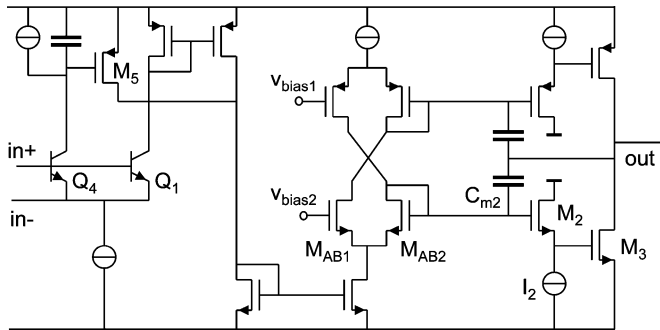
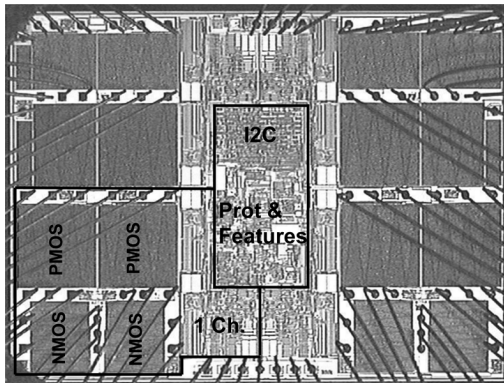
Fig. 13. Simplified schematic of one bridge half ( $A_1$  in Fig. 12).

Fig. 14. Chip photo.

is 20 mA. This is close to weak inversion for this power transistor, and it brings the ratio between quiescent and maximum current close to 200.

The chip photo is shown in Fig. 14. A major selling point for automotive amplifiers is the output power of a saturated square wave output signal. The resistance of the leadframe, bondwires, on-chip metal and transistor  $R_{on}$  all deteriorate this value. Large power transistors, three bondwires per pin and a slew-rate much larger than needed for audio help to reach the measured value of 46 W at 14.4 V supply and a 4  $\Omega$  load. Other features include a low-gain line driver mode, no-plop startup, 10  $\mu$ A standby current, soft mute, load detection, overtemperature protection that gradually decreases the gain with rising temperature, and several other protection features, all accessible by an I2C interface.

## V. MEASUREMENTS

Fig. 15 shows the measured  $Z_{out}$  of the packaged product together with the simulated  $Z_{out}$  of the small signal schematic in Fig. 7. There is a good match, and the stability of the amplifier can be assessed from this figure. First of all, the phase of  $Z_{out}$  does not go below  $0^\circ$  phase shift, meaning that inductive loads can not cause any peaking. Capacitive loads are more dangerous. The phase of  $Z_{out}$  stays below  $45^\circ$  above 1 MHz. At 1 MHz,  $|Z_{out}| \approx 3 \Omega$ , so the maximum capacitive load for 3 dB peaking is 50 nF. For larger  $C_{load}$ , stability quickly deteriorates. Indeed, in extensive measurements with a large number of different complex loads, the amplifier remained stable for any passive load with a capacitive component less than 50 nF, without the use of any external stabilizing network.

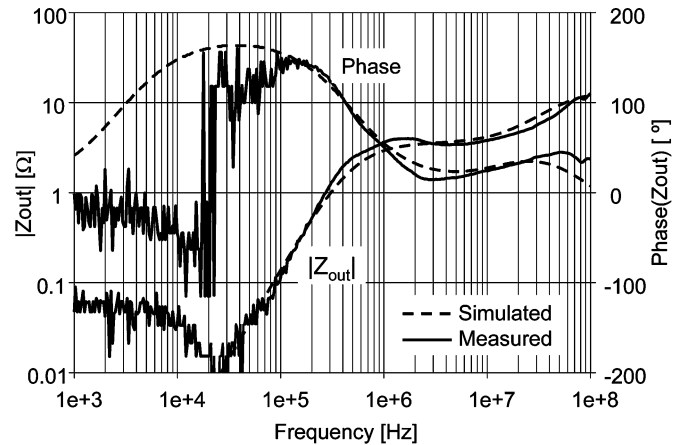


Fig. 15. Measured and simulated (Fig. 7) output impedance.

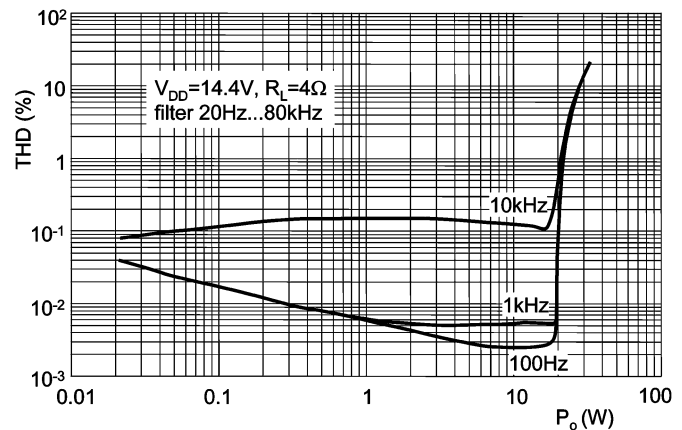


Fig. 16. Measured distortion.

The sole exception is a very small ( $< 100 \text{ m}\Omega$ ) resistive load, because the phase of  $Z_{out}$  approaches  $180^\circ$  for low frequencies, as it would in any amplifier with a second-order open-loop gain. This also causes the notch in  $Z_{out}$  at 20 kHz. The lead frame plus bondwire resistance is positive, and  $Z_o$  is almost purely negative at this frequency. In practice, this means that the amplifier exhibits less stable behavior when it is in a near-short-circuit situation. Any actual instability, however, immediately leads to a large output current because of the low ohmic load, moving the  $Z_{out}$  curve down, increasing stability. In practice, we did not experience any problems with this phenomenon.

Fig. 16 shows the distortion performance. Typical THD +  $N$  is 0.005% @ 1 kHz (10 W, filter 20 Hz–80 kHz), SNR is 110 dB (A).

## VI. CONCLUSION

Output impedance shaping is a technique that allows easy understanding and manipulation of the stability of amplifiers for complex loads. By degenerating the gain of the penultimate stage in a power amplifier, a frequency compensation technique is created that does not need compensation capacitors that are larger than the power transistor parasitics. This is demonstrated by the area-efficient realization of a MOS audio power amplifier that has low THD and good stability over a wide load range.

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