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# Simulation and experimental characterization of reservoir and via layout effects on electromigration lifetime

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**Abstract**

As shrinking of feature sizes in integrated circuits and increasing of packing density continue, it becomes incrementally important to take into account the interconnect layout features which can limit the risk of electromigration failure and improve the reliability of interconnect systems. However, hardly any information is available on the reservoir and via layout effects on electromigration. In this paper, we characterized the influence of via count and current crowding effects on electromigration lifetime in different via and reservoir layouts design through simulation and experiments. We observe a negligible difference in electromigration lifetime for structures having the same reservoir area, irrespective of the contact/via configuration. The effect of current crowding on electromigration lifetime after an increasing of the current density stress was still small. The highest tensile stress point obtained from simulations coincides with the experimentally found void locations. © 2002 Elsevier Science Ltd. All rights reserved.

## 1. Introduction

As device dimensions continue to shrink and clock frequencies continue to increase, the electromigration is becoming an increasingly important aspect of Integrated Circuit (IC) reliability. The electromigration behavior in W-plug/metal stripe structures is different from conventional metal-strip structures because there is a "blocking boundary" which is formed by immobile W-plug in the contact/via. The electromigration failures occur much more readily in near area of W-plug than in metal-strip structures because metal ions are forced away from the contacts/vias by an electrical current, while the metal ions cannot flow through the blocking boundary to fill the vacancies around the contacts/vias area. Much work has reported that the electromigration lifetime of multilevel interconnects is influenced by the presence of a "reservoir" around the contacts/vias. Reservoirs are metal parts not or hardly conducting current and they act as a source to provide atoms for the area around the blocking boundary where the atoms migrate away due to the electrical current. The lifetime of interconnect systems can be prolonged by using reservoirs, which is called "reservoir effect". Several authors have experimentally shown the reservoir effect [1-8,11]. We have developed a simulator that allows modeling of reservoir effects. The simulator is finite element method (FEM). More detail can be found elsewhere [9,10,12]. In previous work[12], we have performed many effect evaluations of reservoir areas using

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the simulator, and results were comparable with published experimental data. In this work, we present electromigration data of simulation and experiment for different via and reservoir layouts in which the simulated and test structures were designed with the same geometries for comparison. The simulated structures were designed with very fine grid in reservoir area that allowed calculating the resistance change. Several via layouts with different number of vias were simulated with different current densities to study the effect of current crowding on electromigration lifetime due to the different layouts. The median-time-to-failure (MTF) of simulation and experiment were normalized for comparison. The results of simulated stress distribution were used to predict the failure location obtained from failure analysis after the electromigration experiments.

## 2. Simulation and test structures

### 2.1. Simulation structures

In this work, the simulation structures were designed with variations in the reservoir area, the reservoir layout (vertical and horizontal), the number of contacts/vias and the contact/via layouts. The structures with number of vias, N equals to 1x1, 1x2, 1x3, 1x4 are named row layouts, and the other structure with number of contacts, N equal to 2x1, 2x1+1, 2x2 are named square layouts. They are shown in Figure 1. Via size is (3.2 x 3.2) $\mu m^2$, the space between two vias is 3.2 μm (on horizontal as well as vertical direction), and the overlap is 0.4 μm. Line length (does not include the reservoir length) and width of all simulation structures are kept the same at 45.2 μm and 3.2 μm respectively. We need to calculate relative resistance change in the reservoir area where it is designed with a much finer grid than in the line. We cannot define a very fine grid for the whole simulation structure due to limited number of nodes and CPU time consumption.

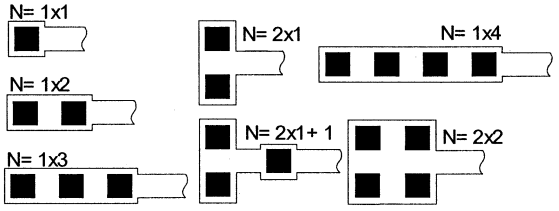


Fig. 1. The different reservoir and via layouts for simulations and experiments.

### 2.2. Test structures

The test structures are designed with the same geometries as simulation structures. However, the dimensions are different. Via size is (0.4 x 0.4)$\mu m^2$, line width and spaces between vias are 0.4 μm. Line length and overlap are 100μm and 0.05μm in case of single via, and are 800μm and 0.08μm in case of multi vias, respectively. These test structures were processed at Infineon Technologies AG.

## 3. Results and discussion

### 3.1. Simulations and experiments for multiple-vias

In this work, we focus on studying the behavior of the reservoir area. Therefore, the total relative resistance change in the reservoir is calculated from the obtained resistance distribution using a so-called P-S model. In the P-S model, the resistance along each row (parallel to the length) is first calculated, and the total resistance is the obtained by treating the rows as being connected in parallel. The equation for relative resistance change calculation using the PS model is as follow;

$$\frac{\Delta R_T(t)}{R_T(0)} = \frac{n_w}{n_l}\sum_{i=1}^{n_l}\left\{\sum_{j=1}^{n_w}\left[1+\left(\frac{\Delta R(t)}{R(0)}\right)_{ij}\right]^{-1}\right\}^{-1} - 1 \qquad (1)$$

Where $\Delta R_T(t)/R_T(0)$ is the total relative resistance change at time, t, $n_l$ and $n_w$ denote the number of node along the length and across the width, respectively.

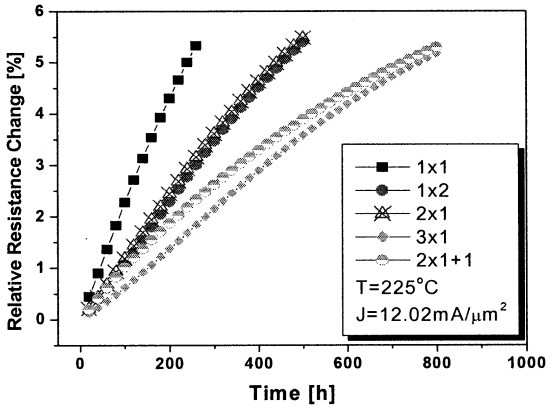


Fig.2. Simulation of relative resistance change versus time of single and multiple-via structures.

$(\Delta R(t)/R(0))_{ij}$ is relative resistance change at the ith and jth node.

The simulated structures were stressed at 225°C with 12.02mA/μm$^2$. The relative resistance change versus time plots for structures with 1, 2 (N=1x2 and N=2x1) and 3 (N=1x3 and N=2x1+1) vias are shown in Figure 2. Simulations show that the evolution of relative resistance change is decreased with increasing of the number of vias, and are only small differences between row and square layouts having the same reservoir area and via number. To estimate MTF in case of the simulation, the failure criterion is an increase of 5% of relative resistance change in the reservoir area only. The results of MTFs are presented in Table 1.

The experiments were carried out the same stress condition with the simulations. Failure time distributions were statistically analyzed assuming a lognormal distribution following JEDEC standards as shown in Figure 3. To calculate the MTF for experimental cases, the failure criterion is set to an increase of relative resistance change of 20% for the entire structure. We missed an experiment of the structure with N=2x1+1 (3 vias in square) at current stress of 12.02 mA/μm$^2$. However, its MTF can be calculated from the MTFs of two different currents stress of 14.9mA/μm$^2$ and 9.13mA/μm using the Arrhenius relation. The results of MTF are shown together with simulation results in Table1. Both simulations and experiments show that the MTFs are increased with increasing of via number. The increasing of MTF is believed to be due to the increasing of the reservoir area, which is noted to delay a void nucleation away from the via. The number of vias did not play any significance in increasing of MTF, because in cases of single and multiple-vias have the same reservoir area, they will have the same lifetime as reported in the previous work [12]. We also find that the MTF of structures with via layouts in square (N=2x1, N=2x1+1) and row (N=1x2, N=1x3) are only slightly different through simulations and experiments, respectively. This means that the via array configurations did not play any significance in improvement of electromigration lifetime, and the effect of current sharing and current crowding can be neglected. A question raises here, the current crowding effect can be neglected or not with a higher current density stress. This will be discussed in next section. The increasing of electromigration lifetime with increasing of via number has been relatively compared through simulations and experiments. For a better comparison between simulation and experiment, we plotted the normalized $MTF_{multiple\text{-}via}/MTF_{single\text{-}via}$ against the normalized area, $S^r_{multiple\text{-}via}/S^r_{single\text{-}via}$ with error bars of 5% as shown in Figure 4. It showed that the maximum error between simulation and experiment is less than 10%. This is acceptable and

Table 1
The results of MTF incases of simulations and experiments

| N | J [mA/μm$^2$] | MTF[h] (Experiment) | MTF[h] (Simulation) | T [°C] |
|---|---|---|---|---|
| **1** | 12.02 | 52.51 | 240 | |
| **1x2** | 12.02 | 131.2 | 454 | |
| **2x1** | 12.02 | 128.2 | 441 | 225 |
| **1x3** | 12.02 | 149.4 | 735 | |
| **2x1+1** | 12.02 | 151.4* | 727 | |
| 1x3 | 14.9 | 204.32 | | |
| 1x3 | 9.13 | 110.54 | | |
| 2x1+1 | 14.9 | 98.6 | | |
| 2x1+1 | 9.13 | 205.2 | | |

* This value is extracted from the other experiments

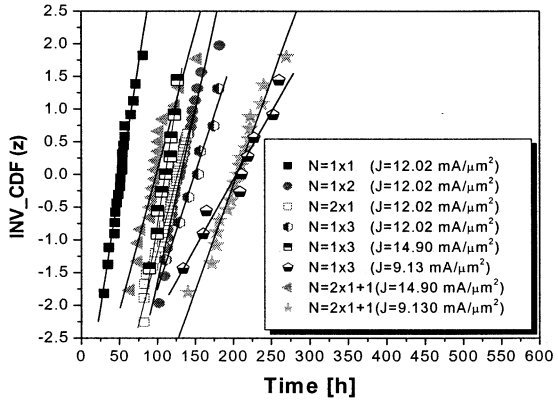


Fig.3. Failure time distributions for single and multiple-via.

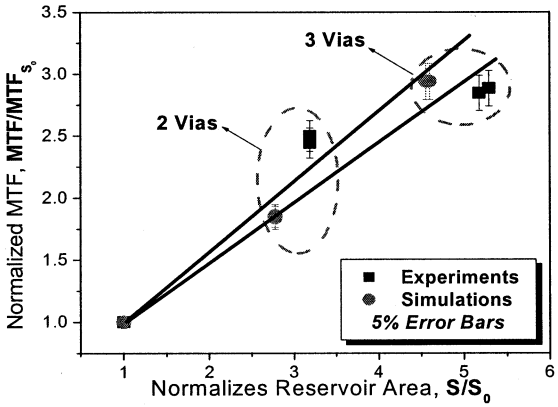


Fig.4. Normalized MTF versus reservoir area for J=12.05 mA/μm$^2$.

could be useful for quickly and cheaply predicted electromigration reliability during IC design.

### 3.2. Effect of current crowding in the via layouts

To study the current crowding effect on the electromigration lifetime due to the different reservoir and via layouts (row and square), we carried out the simulations with a different current stress for structures with 2 vias layout in row and square. When the current density increased from 12.05mA/μm$^2$ to 19.66 A/μm$^2$ (increasing of 63 %), the difference of electromigration lifetime between row and square layouts was still small (see Figure 5). We have carried out another electromigration test, in which the test structures were designed with 4 vias in square and row layouts (see Figure 1 with the structures, N=1x4, and N=2x2). These test structures are different in technology from test structures with 1,2, and 3 vias, which are not discussed in this work. The test structures were stressed at 225°C and with 8.46 and 13.8 mA/μA2.Their lognormal of failure time distributions for these cases are shown in Figure 6. The experiments show that when the current stress is increased from 8.46mA/μm$^2$ to 13.8mA/μA$^2$ (also increasing of 63% like the simulation case), there is a slight increase in the difference of electromigration lifetime between row and square layouts. This means that the current crowding is effecting the electromigration lifetime but it is very small. This effect already presented by K. N. Tu et. al [13]. The simulation results did not show this effect because it was not incorporated in the simulator yet. The well-known equation for vacancy current has been used in the simulator that composes of drift and diffusion current:

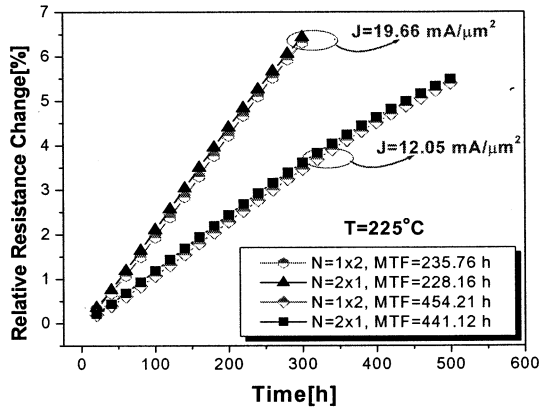


Fig. 5. Relative resistance change versus time simulations for 2 vias layouts (row and square) at different stress current.

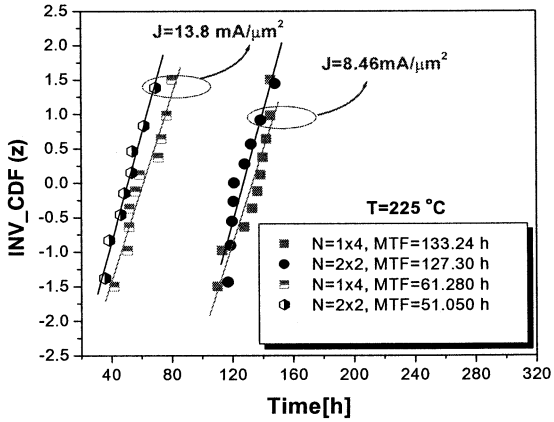


Fig. 6. Failure time distribution of structures 4 vias (in row and square).

$$J_v = -D_v \nabla C_v + \frac{D_v C_v}{kT} Z^* eE \tag{2}$$

Where $C_v$ is the vacancy concentration, $D_v/kT$ is mobility, and $D_v$ is the diffusivity of vacancies in the crystal. In the current crowding region, the vacancy current must be calculated as follow:

$$J_v = -D_v \nabla C_v + \frac{D_v C_v}{kT} Z^* eE + \Delta C_v \left(\frac{D_v}{kT}\right)\left(-\frac{dP}{dr}\right) \tag{3}$$

The third term in equation (3) is due to current crowding driven by the current-density gradient. Where $\Delta C_v$ is the excess vacancy concentration in high current crowding region relative to the constant flux region, (-dP/dr) is the driving force due to current density gradient as in current crowding. The detail calculation of this driving force is given in [13]. Therefore, the current crowding effect will be taken into account for a better simulation. However, the experimental results show that the simulations are qualitatively consistent.

### 3.3. Predicting possible damage locations in a metallization line

The simulator can be used to calculate the stress build-up distribution. Therefore, it can be used to predict the voiding location due to electromigration. In Figure 7, the distributions of tensile stress in the reservoir area are shown associated with voiding from failure analysis by SEM for cases single via and 3 vias in row. We found out that, the voiding will appear at location where we found the maximum of tensile stress

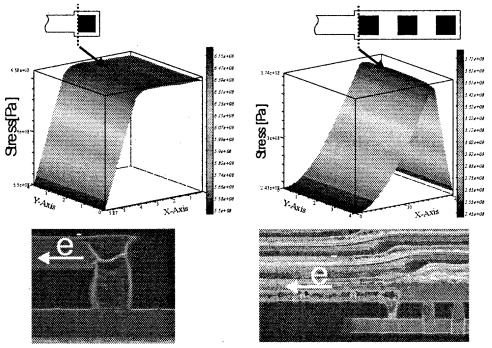


Fig. 7. Stress build-up distribution from simulations and voiding observations.

build-up in simulation. In case of multiple-via, the void occurs only at the vias closest to the line. The failure analysis confirmed that the number of vias does not play significant role in electromigration lifetime but the reservoir area does.

## 4. Conclusions

Both experiments and simulations showed that the reservoir and via layout (square or row) do not play a significant role in electromigration lifetime but the reservoir area does. The current crowding (due to layout) is only slightly affecting electromigration lifetime as shown through experiments. For reliable designs, reservoir areas are therefore more important than number of vias. Furthermore, it can be concluded that simulation can be a good tool to predict reservoir and via configuration effects on electromigration lifetime, and therefore on building-in reliability in the design phase.

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