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Study of crack formation in high-aspect ratio SU-8 structures on silicon

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Abstract

The high-aspect ratio capability of SU-8 photoresist led to the successful use of this epoxy based material in a diversity of microfabricated devices as a construction material as well as for micromolding purposes. Throughout the literature it was noticed that the thermal mismatch of SU-8 and the substrate material silicon generates high film stress in the spin-coated SU-8 causing crack formation in the microstructures. Using baking parameters this crack formation can be minimized but will remain a critical aspect of design. In this study the process was first optimised on non-patterned wafers. Secondly, we transferred this optimised process to a pre-patterned wafer containing deep silicon etch pits to account for a specific application in micromolding. We discuss the behaviour of film stress, number of cracks and crack length. The number of cracks as well as the length of cracks in concave corner designs can be significantly decreased, while round holes resulted even in crack-free microstructures. In the case of pre-patterned wafers no cracks appear around the features, however we observed unsatisfied development within the resist features caused by insufficient solidification in the deep etch pits during Soft Bake. Increased Soft Bake time can overcome these problems but will require more systematic investigations.
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Keywords: SU-8; Micromolding; Crack formation; Post Exposure Bake control

1. Introduction

SU-8 resist is widely used in micromachining as a construction material as well as a material for micromolding, e.g. for AFM cantilever tips and microfluidic chips [1–4]. Several problems with geometry and a crack formation are recognised for the features with a large contact area of SU-8 and a high-aspect ratio. Cracks are formed due to a release of tensile stress in the resist layer. This is strictly dependent not only on intrinsic material properties [5] but also on the design of features formed in SU-8. Since the high-aspect ratio performance of SU-8 can be combined with its molding capabilities to create sophisticate molds on the top of a pre-patterned silicon wafer a better understanding of crack formation and its optimisation is of prime interest. Post Exposure Bake (PEB) and Soft Bake (SB) temperatures were found to be related to tensile stress in the SU-8 films [5]. In literature there are a few systematic studies demonstrating crack formation (stress release) with various designs of SU-8 features. Optimisation routes are still an open question because crack formation is affected not only by process parameters, but also by area of exposure and design of SU-8 features. In our work we will present the influence of process parameters such as Soft Bake, Post Exposure Bake temperatures and cooling rate on crack formation for various designs. The process optimisation considers a number of cracks and maximal crack length.

2. Experimental

In our experiments lithographically formed SU-8 patches with a diameter of 10 mm remain evenly distributed on a 4-in. silicon wafer. Each patch contains groups of microholes of various shapes, as shown in Fig. 1. A total area of exposed SU-8 is about 20% of the wafer area. SU-8 100 is spin-coated to a thickness of 200 μm. During SB wafers are hold at 80 and 90 °C for 120 and 70 min, respectively. The hot-plate is switched off and wafers are allowed

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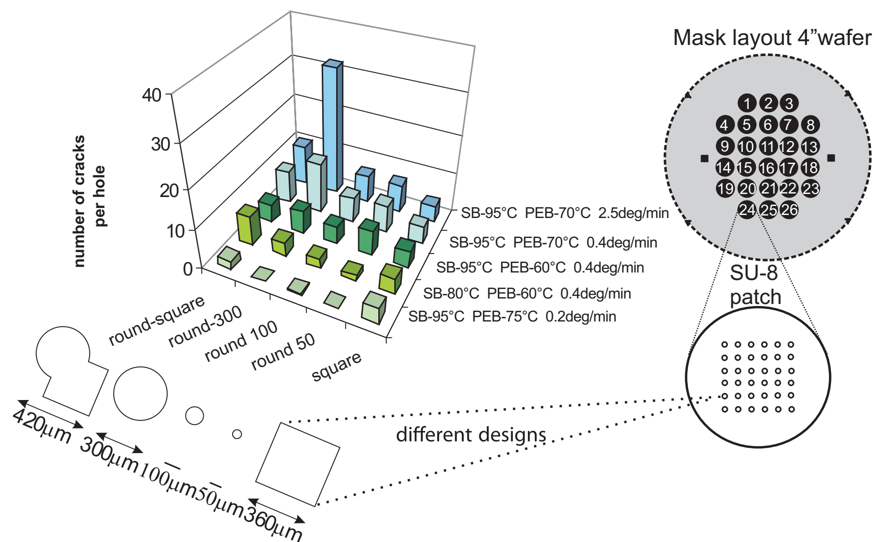

Fig. 1. Number of cracks per opening for different designs and SB, PEB temperatures and cooling rate after PEB step. Mask layout and sketch of SU-8 patch are included.

to cool down to room temperature. After exposure for 90 s PEB control holds the wafers for 40 min at 60, 70 and 75 °C prior to cooling at rates of 0.2, 0.4 and 2.5 deg/min. Development is performed under continuous flow of RER600. Cracks are counted on an area of 5 mm^2 with arrays of 3×3 holes. Two crack parameters, i.e. number of cracks and maximum crack length, are studied on the non-patterned wafers to optimise process parameters. After PEB, stress is determined with curvature measurements using a mechanical stylus across the 4-in. wafer with a scanning length of 80 mm. The optimised process has been transferred to KOH-pre-patterned wafers with etch-depth of 370 μm, that is required for our application.

Fig. 1 shows the number of cracks per hole related to the tested baking conditions for different designs on non-patterned (flat wafers). The number of cracks for designs with concave corners, such as squared holes, hardly changes with the baking conditions. Stress is released predominately within the corner. The number of cracks for designs with round holes decreases with lower SB and PEB temperatures at cooling rate of 0.4 deg/min. As SB temperature decreases from 95 °C to 80 °C, average number of cracks reduces by a factor of 1.6, i.e. from 5.8 to 3.6. As PEB temperature decreases from 70 °C to 60 °C, average number of cracks reduces by a factor of 2.3, i.e. from 13.1 to 5.8. If cooling rate decreases from 2.5 down to 0.2 deg/min, the number of cracks diminishes from 32 to zero. Fig. 2 presents an optical micrograph of SU-8 resist, comparing a "crack-full" and a "crack-free" microhole formed under cooling down at 2.5 and 0.2 deg/min, respectively. Thus, cooling rate is the most significant factor for the number of cracks formed.

The lower SB, PEB temperatures and cooling rate the less stress is built in the resist film. The value of measured stress is close to published data [5], e.g. in the range

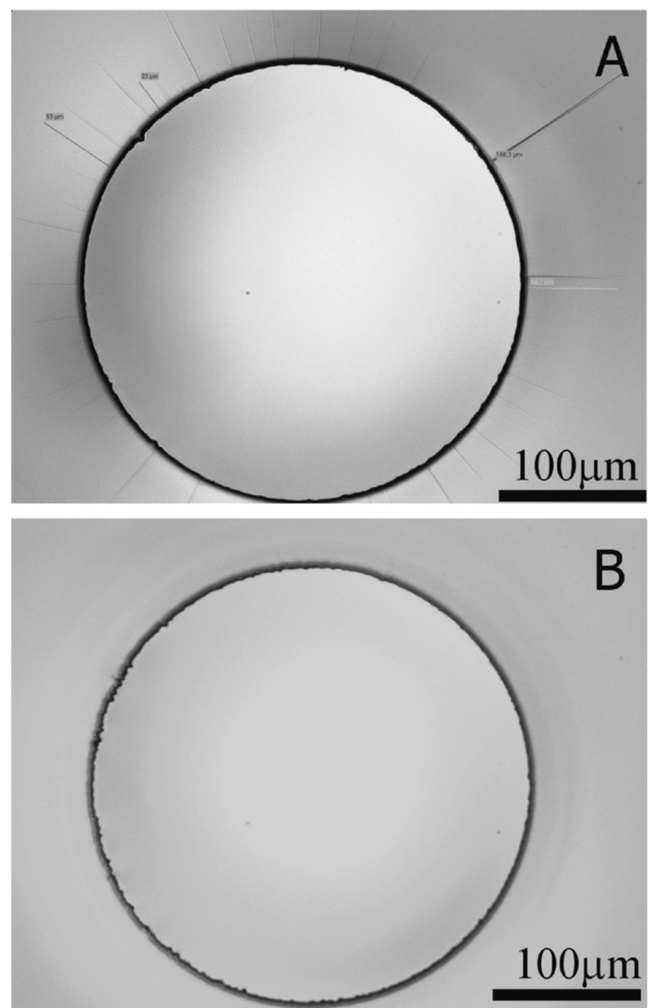

Fig. 2. Microhole in 200 μm SU-8 layer on non-patterned Si-wafer: (A) PEB at 70 °C and cooling rate of 2.5 deg/min; (B) PEB at 75 °C and cooling rate of 0.2 deg/min.

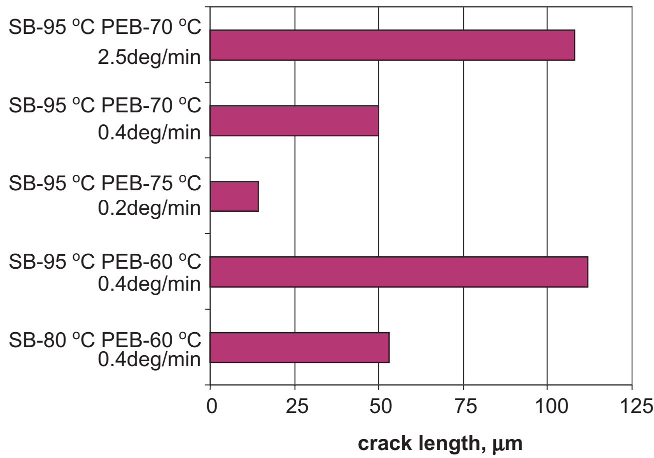

Fig. 3. Maximum length of cracks around a square hole in SU-8 200 μm layer for different baking conditions.

between 1.9 and 6.2 MPa. Although it has to be expected, no drastic increase of stress is observed for a faster cooling of 2.5 deg/min. This can be explained because of inaccuracy of measurements due to an edge bead of SU-8 and/or a deviation of measurements caused by the manual handling of wafers.

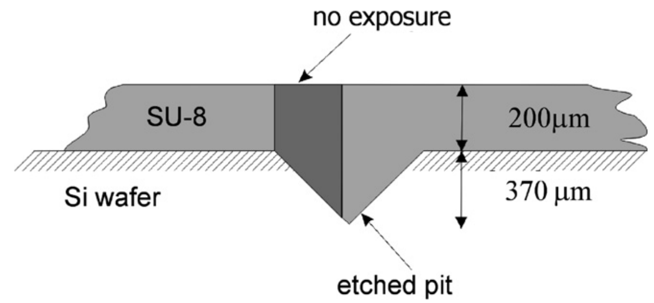

Fig. 4. Sketch of the cross-section of Si-pre-patterned wafer coated with SU-8 resist.

The maximal length of cracks for designs with square holes is the second optimisation factor. This crack length is plotted for various SB, PEB temperatures and cooling rates in Fig. 3. At a PEB temperature of 70° and 75 °C maximum crack length decreases with a slower cooling, e.g. 108, 50 to 14 μm at cooling rate of 2.5, 0.4 and 0.2 deg/min, respectively. Lowering of PEB temperature from 70° down to 60 °C does not make the cracks shorter; in opposite the length increases by a factor of 2.2. Decrease of SB temperature from 95° to 80 °C results in a decrease of

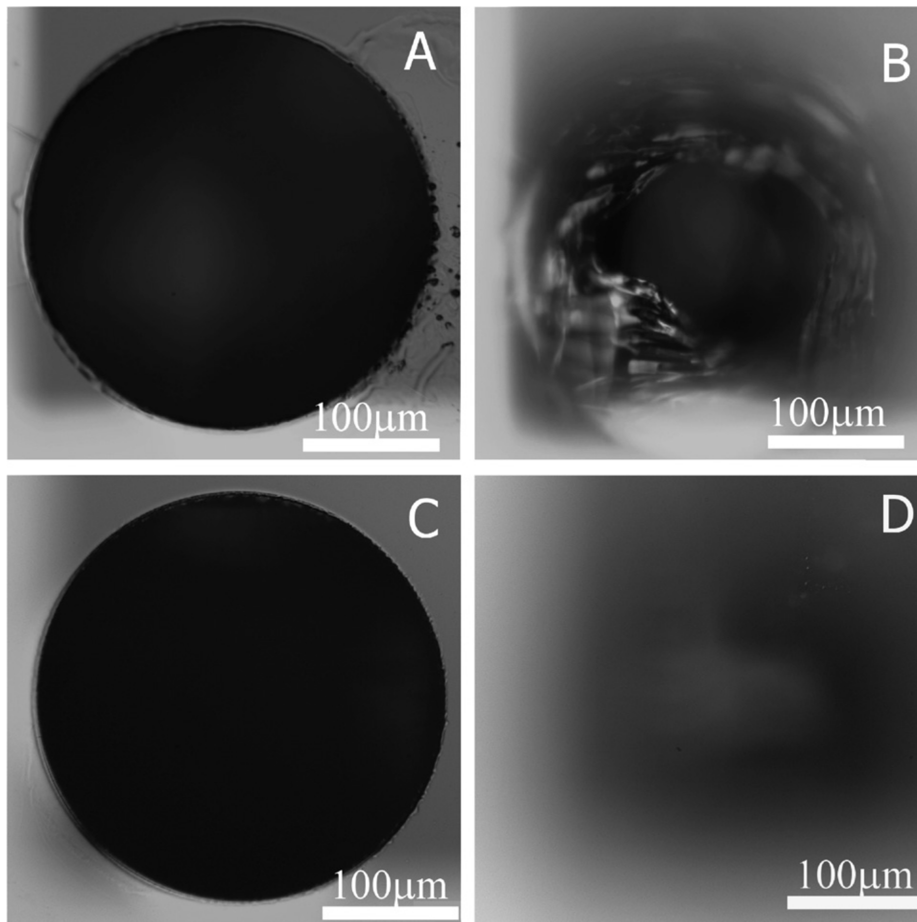

Fig. 5. Micrograph of a microhole in 200 μm SU-8 layer on pre-patterned wafer. PEB at 75 °C with cooling rate of 0.2 deg/min and SB for 70 min (A) above and (B) inside the pyramidal etch pits in the silicon; SB for 210 min (C) above and (D) inside the pyramidal etch pit in the silicon.

crack length by a factor of 2.1. Crack length depends on both SB and PEB temperature, which are parameters that determine the degree of crosslinking of SU-8 and thus its mechanical properties. However, cooling rate shows the largest effect on the crack length at the fixed SB and PEB temperatures. The cracks become shorter with slower cooling.

To optimise the SU-8 process we need to find conditions with minimum number of cracks and minimum crack length. The slower cooling the less number of cracks for designs with round holes and the shorter the maximum length of cracks for designs with square holes at PEB temperature of 75 °C. Based on results of our crack study we have chosen the process with SB temperature of 95 °C for 70 min, PEB temperature of 75 °C for 40 min and a cooling rate after PEB of 0.2 grad/min to minimize both the crack length and number of cracks for our designs. Optimised on non-patterned wafers (PEB temperature at 70–75 °C and cooling at 0.2 deg/min) this SU-8 process has been transferred to pre-patterned silicon wafers that are required in our application of SU-8 structures for micromolding purposes.

In this study we deal with a non-uniform resist thickness throughout the mask layout as shown in Fig. 4 leading non-solidified resist inside the etch pit. The cause of this is that acid photoactivated during lithography can diffuse faster into these incompletely cured regions during PEB, thus the previously optimised SB time for a non-patterned wafer is not sufficient and results in residue inside pyramidal-shaped etch pits in the silicon, as it can be seen in Fig. 5A and B. The SB time has to be increased from 70 min to 210 min to compensate for the thickness variations of SU-8 in the silicon etch pit. Fig. 5C and D shows a micrograph of a microhole for the process with the optimised SB time. No resist residue has been observed inside etch pit in silicon.

3. Conclusions

The influence of SU-8 baking parameters on stress and cracking of 200 μm SU-8 film (SU-8 100) is presented. PEB control resulted in crack-free SU-8 structures for round microholes with a diameter of 50, 100 and 300 μm in SU-8 film on non-patterned wafers, when postbaked at 75 °C for 40 min and cooled down at 0.2 deg/min. Concave corners in the design remained crack sensitive. Crack length for square holes has been reduced down to 14 μm. With a longer SB time (prolonged from 70 min to 210 min) the optimised process can be successfully transferred from non-patterned to pre-patterned wafers with minimized number of cracks.

Acknowledgements

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