High Energy Implanted Transistor Fabrication*

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Abstract

High energy ion implantation forms, together with submicron lithography, trench technology, rapid thermal multiprocessing and simulation programs, are a powerful means of fabricating the tiny transistor structures of the future. Several cross-sections of silicon devices, some of which are already known from the literature, are discussed. The benefits of implantations at energies between 200 and 2000 keV are shown.

1. Introduction

High energy ion implantation is not yet accepted as a standard technique in semiconductor manufacturing. The main reason for this is that experienced technologists feel that the damage caused by high energy ion implantation is more difficult to anneal than the damage caused at lower energies. However, this fear is not justified for doses below the amorphization level. The stopping mechanism gives no indication that at higher energies the damage is of a different nature and Oosterhoff and Middelhoek [1] have experimentally shown that an anneal of the damage is sufficient.

The second reason for the late introduction of high energy ion implantation is the limited availability of suitable equipment. The use of doubly charged ions is not attractive. Decharging of doubly charged to singly charged ions mostly takes place at the entrance of the accelerator tube and these singly charged ions can only be removed by an extra mass separator behind the ion accelerator. The decharging depends on the conditions of the machine and is not reproducible [2].

The special advantages of using higher energies compared with conventional ion implantation can be summarized as follows.

(1) The required dopant concentration distribution can be obtained without drive-in diffusion.

(2) The dimensions in the lateral and perpendicular directions of the semiconductor devices can be minimized.

(3) The devices can be optimized by "profile engineering".

(4) The mutual interaction between process steps is reduced.

(5) Shallow buried layers can be made at precise depths; this is difficult to achieve with epitaxy.

Also some limitations of using higher energies should be mentioned.

(1) Only shallow layers can be fabricated.

(2) The ratio of the maximum concentration to the concentration at the surface is in practice only 500.

(3) Deep implantations also require thick masking layers.

An overview of the literature on the physics and applications of megaelectronvolt ion implantations can be found in refs. 3 and 4.

2. Essential features of implanted ion distributions

The projected ranges R_p in silicon of boron and phosphorus even at 1 MeV are small. The R_p for boron is 1.65 μm and for phosphorus 1.15 μm [5]. The ratio of the maximum concentration to the concentration at the surface is in practice only 500. These two features limit the application to shallow devices for low voltage operation.

In Fig. 1, two concentration distributions are shown. The curve labelled poly is determined experimentally with secondary ion mass spectrometry and complies with the theoretical pre-

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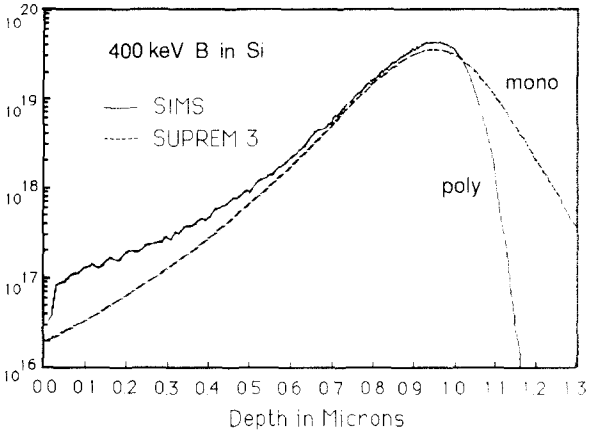

Fig. 1. 400 keV boron implantation for polycrystalline and single-crystal silicon.

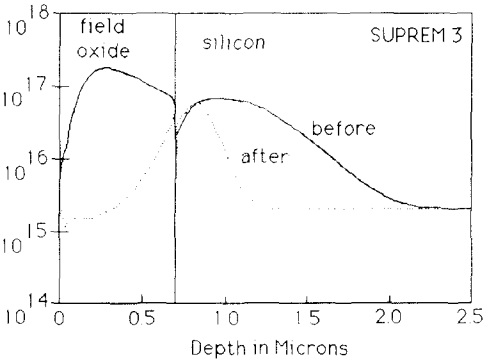

Fig. 2. Field implantation before and after oxidation.

dictions. The curve labelled mono is a curve fit of the experimental results of Oosterhoff [5]. The curves differ in essential points. Beyond the maximum the curve labelled mono displays the consequences of channelling. The reason why the front of the curve labelled poly shows higher concentrations is not obvious. Channelling might also be the explanation in this case. Single-crystal silicon would then allow more channelling from the beginning whereas this phenomenon is absent for polycrystalline silicon.

3. Applications

3.1. Field doping

In standard processes the field doping is carried out before the oxidation. In this case in-diffusion, out-diffusion and also segregation at the interface takes place. The final doping concentration at the interface depends strongly on the oxidation conditions. High energies allow implantation through the thick field oxide which is used in metal-oxide-semiconductor (MOS)

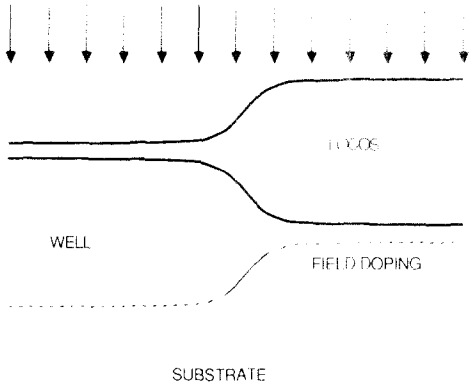

Fig. 3. Combined well and field implantation in CMOS technology.

transistor processing. An independent control of the doping concentration at the interface is obtained (Fig. 2) [6].

A very useful application is found in complementary metal-oxide-semiconductor (CMOS) processing (Fig. 3). The field and well implantation can be combined. With just one implantation the well and the field doping are achieved [6].

This technique has wider applications in semiconductor fabrication. A layer can be a mask for low energy implantation but not for high energy implantation.

3.2. Complementary metal-oxide-semiconductor processing with retrograde wells

The well in standard CMOS processing is obtained by a time-consuming drive-in diffusion at high temperatures. This well is deep and extends itself also in the lateral direction. This is necessary because parasitic n-p-n-p structures are formed which cause so-called latch-up. At an occasional voltage pulse an undesired conductive path is formed; this is prevented by forming long base transistors. This effect can also be prevented by a retrograde doping profile as obtained by high energy implantation. Then the parasitic transistor is spoiled by a large Gummel factor. Figure 4 shows a cross-section of a twin-well CMOS process with retrograde wells. Three integrated-circuit manufacturers are now using this technique. A high temperature step is made superfluous and in some cases one or two photomasks are also saved [6].

3.3. Buried bit line dynamic random access memory

High energy implantation forms a maximum concentration at a reproducible distance from the

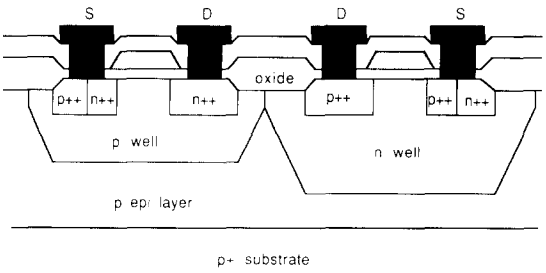

Fig. 4. CMOS with retrograde wells.

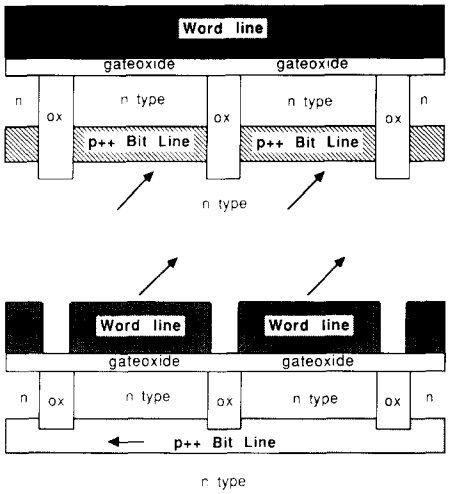

Fig. 5. Buried bit line DRAM cross-point cell.

surface of the wafer. It would be very difficult to use epitaxy to form a buried layer at such a small and reproducible distance from the surface. This feature is essential for the construction of the buried bit line cell (Fig. 5). At the cross-point of the word line and the bit line a MOS structure is present. An inversion layer can be formed at a suitable pair of voltages. This is the writing action. At another pair of voltages the inversion layer charge can be transferred to the bit line. The working principle of this dynamic random access memory (DRAM) cell has been demonstrated by Mouthaan and Vertregt [7].

This cross-point memory cell is very attractive because it can be scaled down to the photolithographic limits. However, the conductance of the bit line is too low to make this cell feasible. Buried silicides might offer a solution to this conductance problem. The recent results with cobalt silicide are very promising [8, 9].

3.4. Duo-photodiode

The fabrication of a duo-photodiode is the most straightforward application of a shallow

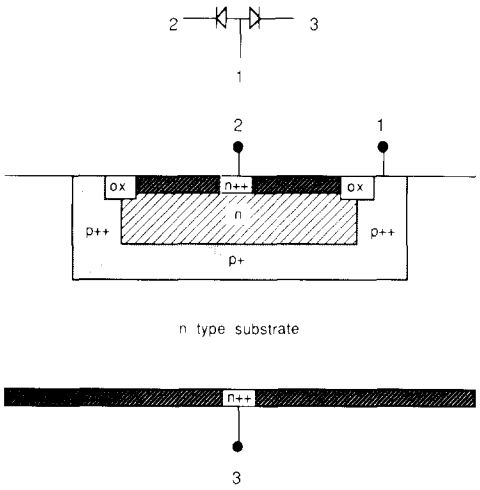

Fig. 6. Duo-photodiode made with deep implanted p^{++} layer.

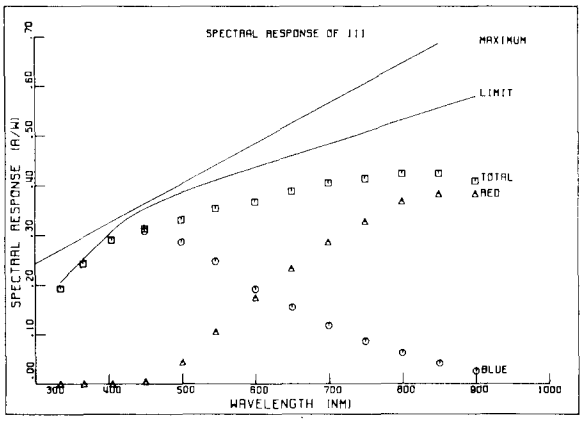

Fig. 7. Spectral response of a duo-photodiode.

implanted buried layer (Fig. 6). Two photosensitive diodes are formed, whose spectral responses are different. The upper diode is also sensitive to the blue part of the visible spectrum, while the lower diode is only sensitive in the longer-wavelength range. The spectral response is shown in Fig. 7. A "poor man's" spectrophotometer can be made with this diode [10].

3.5. Vertically integrated injection logic

Most semiconductor structures require a four-layer structure. If the ion profiles were of a simple gaussian form, an all-implanted four-layer structure could be easily made. Actual profiles (Fig. 1) do not allow much variation in the doping distributions. A practical combination of doping doses and implantation energies is shown in Fig. 8. These layers are suitable for bipolar structures. One of the most promising is the vertically integrated injection logic cell (Fig. 9). Both n-p-n

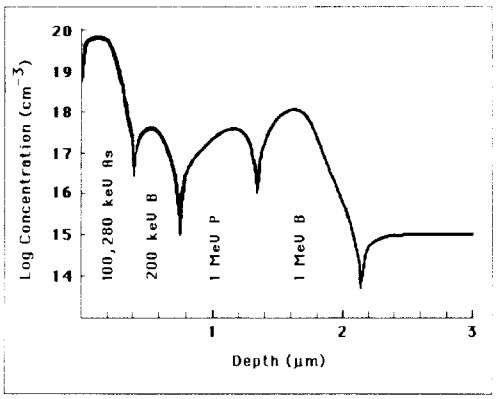

Fig. 8. All-implanted four-layer structure for device applications.

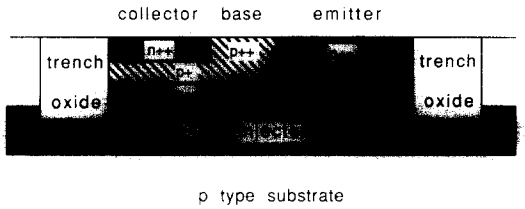

Fig. 9. Vertically integrated injection logic using deep ion implantation.

and p–n–p transistors have small transit times allowing delays below 1 ns. The usual advantages of vertical injection logic, such as lay-out facilitation and absence of power lines on the silicon surface are present [11].

Since ion implantation is the only source of doping, high device reproducibility is achieved and fine tuning is possible to optimize the device characteristics. This same process realizes low voltage vertical p–n–p and n–p–n transistors with moderate gain but small transit times without extra masks [12].

3.6. A lateral n–p–n bipolar transistor

High energy ion implantation offers so many new ways to realize semiconductor structures that it is necessary to reconsider all the reasons why standard devices are made in the usual way. Lateral p–n–p transistors have a poor performance. The proposal of a lateral n–p–n transistor is therefore adventurous (Fig. 10). The structure of a lateral n–p–n transistor is completely different from that of a conventional p–n–p transistor, however. The base is made by implantation through the same window as the emitter, in a similar way to the doubly diffused MOS transistors. Precise values for the lateral straggle are

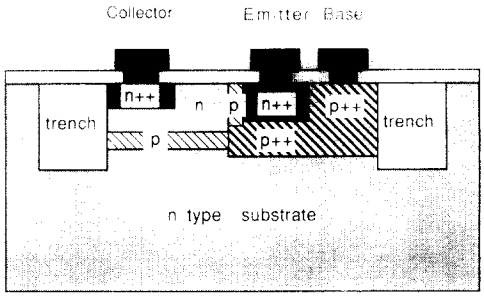

Fig. 10. All-implanted lateral n–p–n transistor.

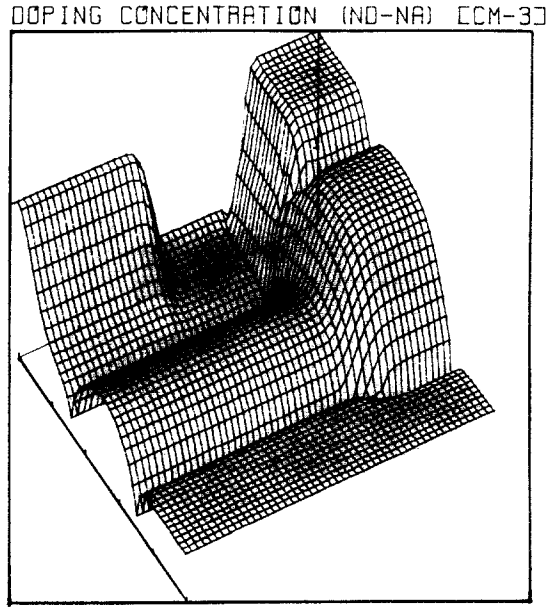

Fig. 11. Two-dimensional simulation of doping distributions of a lateral n–p–n transistor.

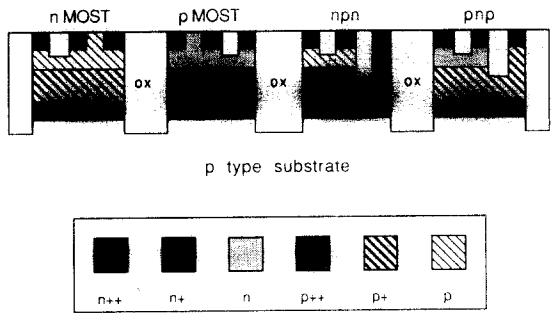

Fig. 12. All-implanted CMOS and bipolar structures.

required. This year, Van Schie of our laboratory hopes to present experimental data on the depth-dependent lateral straggle.

The base is also isolated from the n-type substrate. The parasitic transistor with the substrate

is prevented by a p^{++}-type layer under the emitter. The collector and the base resistance are small and the transit time is minimum. Some knowledge of the lateral straggle is required. Two-dimensional simulation is essential for the preparation and fine tuning of the process (Fig. 11).

3.7. Complementary metal–oxide–semiconductor and bipolar processing

The ideal of the technologist is to develop a process in which MOS transistors of both types and bipolar transistors of both types can be made. Digital as well as analogue signal processing should be possible. The process should be able to be scaled down to the photolithographic limits of the moment. The lay-out and design rules of all four transistors should be the same. The designer would then have complete freedom. Figure 12 shows a cross-section of such all-implanted ideal device structures.

4. Conclusion

Implanters for the energy range 200 keV–2 MeV offer the process engineeer a tool which fits the trend towards smaller and shallower devices very well. Precise experimental values of ranges and straggles and two-dimensional simulation programs, which make these data operational, are a prerequisite for exploring new applications of the "deep implants". "Profile engineering" becomes possible; that is to say, fine tuning of ion distributions so that optimum device characteristics can be obtained.

References

1 S. Oosterhoff and J. Middelhoek, *Solid-State Electron., 28* (1985) 427.
2 P. Spinelli, J. Escaron, A. Soubie and M. Bruel, *Nucl. Instrum. Methods B, 6* (1985) 283.
3 J. F. Ziegler, *Nucl. Instrum. Methods B, 6* (1985) 270.
4 D. Pramanik and M. Current, *Solid-State Technol., 27* (1984) 211.
5 S. Oosterhoff, *Nucl. Instrum. Methods B, 30* (1988) 1.
6 A. Stolmeijer, *IEEE Trans. Electron Devices, 33* (1986) 450.
7 A. J. Mouthaan and M. Vertregt, *Solid-State Electron., 29* (1986) 1289.
8 A. E. White, K. T. Short, R. C. Dynes, J. P. Garno and J. M. Gibson, *Appl. Phys. Lett., 50* (1987) 95.
9 A. H. van Ommen, J. J. M. Ottenheim, A. M. L. Theunissen and A. G. Mouwen, submitted to *Appl. Phys. Lett.*
10 S. Oosterhoff and Th. A. H. M. Scholten, in P. Bergveld (ed.), *Proc. Conf. on Sensors and Actuators*, Kluwer, Deventer, 1984, p. 137.
11 V. Blatt, P. S. Walsh and L. W. Kennedy, *IEEE J. Solid-State Circuits, 10* (1975) 336.
12 A. J. Mouthaan, *Ph.D. Thesis*, University of Twente, 1986.