A Nonvolatile Analog Programmable Voltage Source Using the VIPMOS EEPROM Structure

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***Abstract*—A programmable voltage source using the vertical-injection-punchthrough-based MOS (VIPMOS) EEPROM structure has been developed. The circuit operates at a single 5-V supply and the output voltage is continuously available also during programming. The effect of programming is linearly dependent on the programming time. During programming no crosstalk from the enable pulses and only a little crosstalk from the program current is observed. If a decreasing program current is used, the output of the circuit can be set to its desired value without the need of an iterative program process.**

I. Introduction

In recent years several attempts have been made for nonvolatile analog data storage on EEPROM's. Examples of applications are offset compensation in op amps [1], analog weight storage for neural networks [2], and analog recording of speech [3]. In all these applications, the EEPROM's utilize tunneling for both programming and erasing. For programming high-voltage pulses are applied to the control gate and the floating gate follows due to the capacitive coupling to the control gate. During erasing the high-voltage erase pulses are capacitively coupled to the floating gate. During programming and erasing the floating-gate potential differs from the potential during reading, so monitoring of the floating-gate potential during programming and erasing is not possible. Hence, programming of an analog value requires the iterative application of a program pulse and reading of the device. During reading the output signal is compared to the desired output value. The iteration process stops after the EEPROM output signal has approximated the desired value sufficiently close. In contrast, the vertical-injection-punchthrough-based MOS (VIPMOS) EEPROM structure [4] can be programmed in a single step without high control gate pulses.

In this paper a programmable voltage source using the VIPMOS EEPROM is presented. This circuit has the ability to monitor the output voltage during programming. In Section II the VIPMOS structure is explained. In Section III the circuit is introduced. The voltage source can, for instance, be used to set the multiplication factor of a multiplier in a programmable filter or to set the weight factor in a synapse of a neural network. Section IV describes the operation of the circuit while in Section V measurement results are presented. In Section VI some conclusions are given.

Manuscript received December 4, 1992; revised March 2, 1993. This work was supported by Philips Research Laboratories, Eindhoven, The Netherlands.

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IEEE Log Number 9208996.

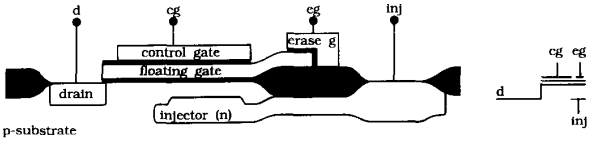

Fig. 1. The VIPMOS EEPROM structure and circuit scheme.

II. The VIPMOS EEPROM

The VIPMOS EEPROM structure is given in Fig. 1 and has been described in [4] and [5]. The structure is based on an NMOS transistor. The source of the transistor has been omitted, the gate is left floating, and a control gate is placed on top of the floating gate. An n-type buried injector is formed under the floating gate by high-energy ion implantation.

In the program mode of the VIPMOS, a channel is present under the floating gate. The channel potential is controlled by the drain voltage V_d. For a sufficiently high drain-injector voltage, called the punchthrough voltage V_{pt}, the depletion layer between the channel and the buried injector reaches punchthrough. Further increase causes a punchthrough current I_{pt} flowing from the channel to the injector according to:

$$I_{pt} = I_0 \exp \frac{q(V_d - V_{inj} - V_{pt})}{nkT} \tag{1}$$

where n is the nonideality factor, V_d is the drain potential, V_{inj} is the injector potential, V_{pt} is the punchthrough voltage, and I_0 is the reverse saturation current. The nonideality factor, reverse saturation current, and punchthrough voltage are device parameters that are mainly determined by the doping profiles of the injector and the substrate and by the gate oxide thickness. A fraction of the electrons, flowing from the injector towards the channel, becomes hot and will be injected through the gate oxide into the floating gate. The others are collected by the drain. The ratio between the current through the gate oxide and the punchthrough current is called the injection probability P_{inj}. This probability depends on the floating-gate potential [6], [7] and the injector current. Connecting the injector to the supply voltage prohibits the punchthrough conditions and disables programming.

A SPICE model of the VIPMOS transistor has been used for simulation. This model is given in Fig. 2. The current I_{pt} models the punchthrough current according to (1). The controlled current source I_{fg} is equal to the product of the punchthrough current and the injection probability. I_{tun} models the tunnel current by a standard Fowler–Nordheim relation [8].

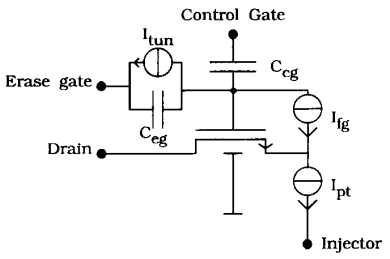

Fig. 2. SPICE model of the VIPMOST.

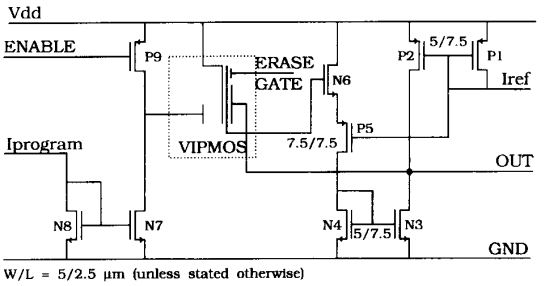

Fig. 3. The programmable voltage source.

The injector current is provided by a controlled current source. Since a channel has to be present under the floating gate, the floating-gate potential has to exceed the threshold voltage of the VIPMOS. The potential of the channel is above the punchthrough voltage, so the threshold voltage of the VIPMOS is increased by the body effect. A high voltage, applied to the erase gate, removes the electrons by tunneling through the interpoly oxide and erases the VIPMOS.

III. The Programmable Voltage Source

The floating gate can only have connections to other gates since it has to be floating. To sense the potential of the floating gate, a separate sense transistor can be used as shown in Fig. 3. If a channel is present under both the VIPMOS structure and the sense transistor, the potential of the floating gate is

$$V_{fg} = V_{cg}\frac{C_{cg}}{C_{tot}} + V_{eg}\frac{C_{eg}}{C_{tot}} + V_{ch}\frac{C_{ch}}{C_{tot}} + V_{chs}\frac{C_{chs}}{C_{tot}} + V_p\frac{C_p}{C_{tot}} + \frac{Q_{fg}}{C_{tot}} \tag{2}$$

where

V_{cg}, C_{cg} control gate potential and capacitance,
V_{eg}, C_{eg} erase gate potential and capacitance,
V_{ch}, C_{ch} channel potential and capacitance,
V_{cgs}, C_{cgs} channel potential and capacitance of the sense transistor,
C_p, V_p parasitic capacitance and potential of the nodes connected to the parasitic capacitance,
Q_{fg} amount of stored charge,

and

$$C_{tot} = C_{cg} + C_{eg} + C_{ch} + C_p + C_{chs}.$$

The parasitic capacitances are the overlap capacitances of the VIPMOS and the sense transistor and the capacitances to the substrate. The potentials are referred to the substrate and the capacitances are defined as the capacitance between the floating gate and the named node.

For constant potentials of the erase gate, the nodes connected to the parasitic capacitances and the channels, the floating-gate potential is only dependent on the control-gate potential and the stored charge. If the floating-gate potential is kept constant, for instance by a feedback loop, the control-gate potential is linearly dependent on the charge. The injection probability is constant for a constant floating-gate potential, so the amount of stored charge is linearly dependent on the program current I_{prog} and program time t_{prog}. The change in the control gate potential is

$$\Delta V_{cg} = \frac{I_{prog} t_{prog} P_{inj}}{C_{cg}}. \tag{3}$$

The parasitic capacitances do not influence the program behavior.

Fig. 3 shows the scheme of a circuit keeping the floating-gate potential constant [10]. The floating gate is connected to the gate of the sense transistor N_6. The constant gate voltage of $P1$ is used by $P5$ to bias the sense transistor at a constant drain–source potential. The sense current is mirrored by $N4, N3$ and compared to a reference current that is mirrored by $P1, P2$. A difference in these currents results in a change of the output potential. The output is connected to the control gate of the VIPMOS. If the sense current is smaller than the reference current, the output potential increases, the floating-gate potential increases and the sense current will increase. Since in equilibrium the reference current and the sense current are equal, the W/L ratio of $P5$ has to be larger than the W/L ratio of $P1$ to provide a proper bias voltage for $N6$. The transfer function of the floating-gate potential to the sense current is

$$\frac{i_{sense}}{v_{fg}} = g_{m_s}\frac{g_{m_b}}{g_{m_s} + g_{m_b}} \tag{4}$$

where g_{m_s} is the transconductance of the sense transistor and g_{m_b} is the transconductance of the bias transistor. The current mirror $N7, N8$ mirrors the program current into the injector and the enable transistor $P9$ connects the injector to the supply voltage if programming is disabled.

The output impedance of the circuit is formed by the parallel connection of the drain transconductances of the N- and P-mirror. If the output is only connected to gates, this high impedance is not a problem, but if the output has to deliver a current, a buffer [9] is necessary.

The minimum supply voltage for the circuit is dependent on the V_{pt} of the VIPMOS. The minimum injector potential is the saturation voltage of transistor $N7$. From (1) the minimum drain voltage can be calculated. The minimum and maximum output voltages are determined by the saturation voltages of $N3$ and $P2$. The high voltage, needed for erasing, can be provided by an on-chip charge-pump circuit, since the erase voltage is only connected to the high-impedance erase gate.

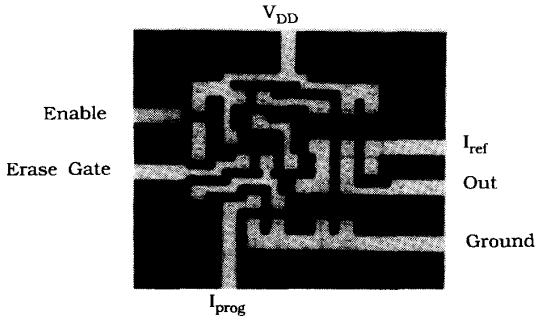

Fig. 4. Photo of the circuit.

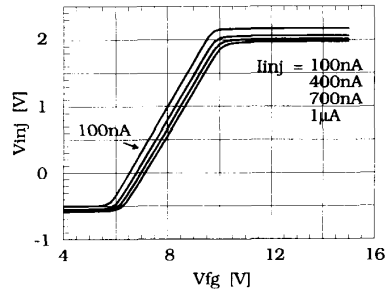

Fig. 5. Injector potential versus floating-gate potential for different injector currents ($V_{drain} = 5$ V).

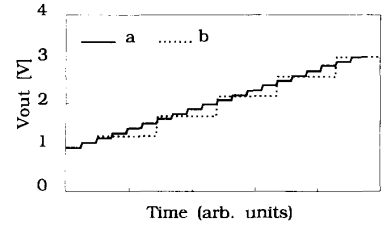

Fig. 6. Programming characteristics.

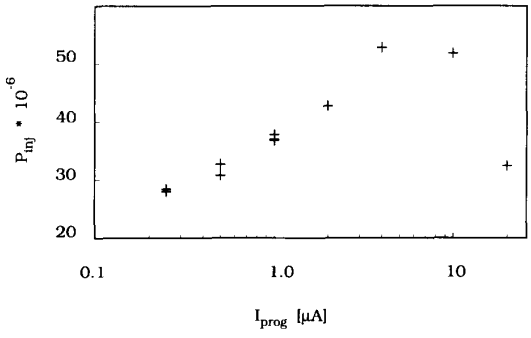

Fig. 7. Injection probability versus program current.

IV. Circuit Operation

During normal operation only the supply voltage and the reference current have to be supplied to the circuit and the ENABLE input has to be connected to ground. For programming, a program current has to be supplied and the ENABLE input should be connected to the supply voltage. Before the feedback loop can become active, erasing is necessary.

The stability of the feedback loop has been investigated by simulations. The open-loop gain is 27.3 dB, the unity-gain frequency is 6.8 MHz, and the phase margin is 87°. A capacitive load on the output lowers the first pole, so a capacitive load does not lead to instabilities. For a 100-pF load the simulation results are a unity-gain frequency of 7.1 kHz and a phase margin of 92°.

V. Measurement Results

Fig. 4 shows a photograph of the chip. The circuit has been realized in the 2.5-μm CMOS process of the MESA Research Institute. The area consumption is $65 \cdot 56 = 3640\,\mu\text{m}^2$.

In Fig. 5 the injector potential, as a function of the floating-gate potential, is shown for different injector currents and a constant drain voltage of 5 V. A single VIPMOS structure with a contacted "floating gate" has been used for these measurements. A current was forced into the injector and the injector potential was measured as a function of the floating-gate potential. For floating-gate potentials below 6 V no punchthrough occurs. The injector–substrate junction is forward biased and the injector current flows into the substrate (note that this condition only occurs in the test setup). If V_{fg} exceeds 10 V an inversion layer is present under the floating gate and the injector potential is independent on the floating-gate potential. The punchthrough voltage is the potential difference between the channel and the injector and is 3 V. At a supply voltage of 5 V the injector voltage is 2 V, which is above the saturation voltage of transistor $N7$, so the circuit can operate at a single 5-V supply.

Fig. 6 shows two different programming characteristics, measured on a complete circuit. The circuit has been erased by an off-chip high voltage of 25 V. The program current was 1 μA and the reference current was 10 μA. For curve a enable pulses of 250 μs have been applied to the enable input. For curve b the pulse length was 1 ms. The figure does not show the actual transient behavior but only the effect of the program pulses, so the time scale is arbitrary. The average ΔV_{out} is 109 mV for curve a and 448 mV for curve b. The variance in the step size is 2% and measurements for different program currents and times all showed a variance of maximal 2%. Since the program current has to discharge the injector–substrate capacitance before programming, the average ΔV_{out} for 1-ms pulses is a little larger compared to four 250-μs pulses. The control gate capacitance is 85 fF, which gives, according to (3), an injection probability of $37 \cdot 10^{-6}$ for a program current of 1 μA.

The injection probability is dependent on the program current. Using the above-described method, the probability has been determined for several values of the program current. Fig. 7 shows the results. For program currents below 5 μA, the injection probability increases for an increasing current. If the program current exceeds 5 μA, the injector voltage becomes less than the saturation voltage of transistor $N7$. The program current is not mirrored properly and the injector current is not equal to the program current.

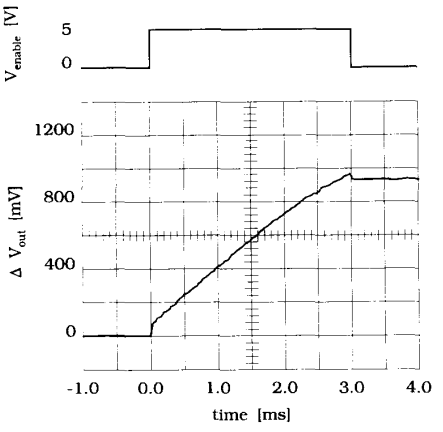

Fig. 8. Transient program behavior with a constant program current.

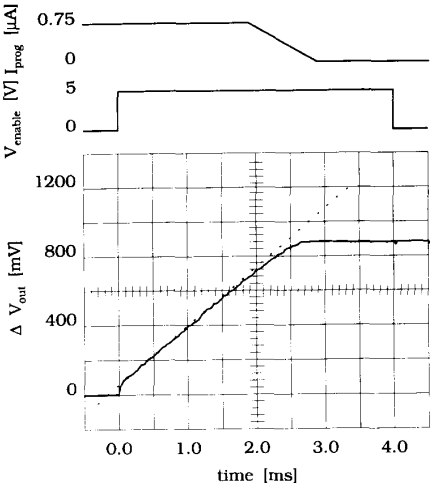

Fig. 9. Transient program behavior with a decreasing program current.

The transient behavior of the output voltage during programming is shown in Fig. 8. At $t = 0$ ms an enable pulse of 3 ms has been given. The program current was 750 nA. Fig. 8 shows that the output voltage can be monitored during programming. At $t = 0$ ms and $t = 3$ ms crosstalk is visible at the output. The program current causes a voltage drop over the channel of the VIPMOS structure. According to (2) this voltage drop will influence the control-gate potential, if the floating-gate potential is kept constant. The measured crosstalk is 30 mV at the start and at the end of programming. The voltage drop over the channel is linearly dependent on the program current. In Fig. 9 the transient behavior is given if the program current decreases during programming. At $t = 0$ ms an enable pulse of 4 ms is given. The program current is 750 nA at the begin of programming. At $t = 2$ ms the program current starts to decrease and is zero at $t = 3$ ms. The crosstalk at the start of the program pulse is equal to the crosstalk of Fig. 8, but at the end of the program pulse no significant crosstalk is observed. Measurements at a program current of 1 nA showed no measurable crosstalk of the enable signal to the output (<2 mV).

VI. Conclusions

A 5-V-only nonvolatile analog programmable voltage source has been developed. The circuit can be programmed by current control. The output voltage is continuously available also during programming and is linearly dependent on the program time. During programming only crosstalk of the program current and not of the enable pulse is measured on the output. This makes it possible to program the circuit with a feedback loop. The program current has to be made dependent on the difference of the measured and desired output potential. After the desired output potential is reached, programming can be disabled.

Acknowledgment

The authors would like to thank A. Kooy for mask fabrication, T. Aarnink for processing the chip, and H. de Vries and K. Lippe for assistance with the measurements.

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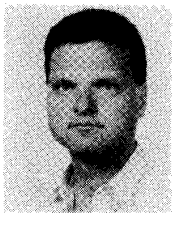

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