Errata to:

An In-Band Full-Duplex Radio Receiver with a Passive Vector Modulator Downmixer for Self-Interference Cancellation:

Two minor errata apply to the body of this paper as it appears below and in IEEE Journal of Solid-State Circuits.

Section III-C:

"Therefore, every 1 dB of cancellation of the SI would result in a 2 dB reduction of the SI-induced IM3, boosting the effective IIP3 by 1 dB."

This is incorrect, it should be:

*"Therefore, every 1 dB of cancellation of the SI would result in a **3 dB** reduction of the SI-induced IM3, boosting the effective IIP3 by **1.5 dB.**"*

Section IV-C:

"The fact that the IIP3 does not increase by the full 27 dB indicates that the linearity bottleneck has moved from the TIA to the nonlinear RX and VM switches."

This should be, in correspondence with the previous correction:

*"The fact that the IIP3 does not increase by the full **1.5 x 27 dB (section III-C)** indicates that the linearity bottleneck has moved from the TIA to the nonlinear RX and VM switches."*

An In-Band Full-Duplex Radio Receiver with a Passive Vector Modulator Downmixer for Self-Interference Cancellation

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Abstract

In-band full-duplex wireless, i.e. simultaneous transmission and reception at the same frequency, introduces strong self-interference (SI) that masks the signal to be received. This paper proposes a receiver in which a copy of the transmit signal is fed through a switched-resistor vector modulator that provides simultaneous downmixing, phase shift and amplitude scaling and subtracts it in the analog baseband for up to 27dB SI-cancellation. Cancelling before active baseband amplification avoids self-blocking, and highly linear mixers keep SI-induced distortion low, for a receiver SI-to-Noise-and-Distortion-Ratio (SINDR) of up to 71.5dB in 16.25MHz BW. When combined with a two-port antenna with only 20dB isolation, the low RX distortion theoretically allows sufficient digital cancellation for over 90dB link budget, sufficient for short-range, low-power full-duplex links.

Index Terms

Full-Duplex, Self-Interference, Receiver, Vector Modulator, Distortion, Interference Cancellation

I. Introduction

In-band full-duplex (FD) wireless communication is an emerging, unconventional scheme for radio links: Transmission and reception occur simultaneously at the same frequency, thus

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utilizing the same spectral resources in two directions at once. In the physical layer, full-duplex obviously promises up to 2x spectral efficiency. In higher network layers, further advantages are being explored such as collision prevention, low latency and security [1]. Additionally, FD simplifies frequency planning.

The main issue in achieving FD wireless is strong in-band (same-channel) crosstalk from transmitter to receiver, referred to as self-interference (SI), see figure 1a [2]. Recovering the (much weaker) desired signal from a remote transmitter necessitates SI isolation and cancellation. Cancellation uses knowledge of the transmit signal from various points in the TX chain to subtract SI in the RX chain (figure 1b).

From this generic view, many types of SI-cancellation can be conceived, and to some extent freely combined, ranging from RF to analog BB, to digital BB and even cross-domain cancellation. Figure 2 shows four recent approaches to SI-cancellation:

a) High isolation can be obtained at the antenna by design, e.g. using cross-polarization [3]. However, it is difficult to achieve high isolation in compact hand-held devices with a varying antenna near-field. Such variations can be addressed using tuneable coupling between antennas [4] which recently showed integration potential and wideband cancellation at 60GHz [5]. Another approach is electrical balance duplexing [3], which can be tuneable and frequency-agile, but has extreme linearity requirements only demonstrated in SOI CMOS [6].
b) Direct crosstalk as well as part of the reflected SI can be cancelled using an analog multi-tap filter at RF, combined with digital cancellation [7], [8]. This requires nanosecond-scale analog delays in its analog filter [7], which have only recently been integrated in the form of N-path filters [8]. This approach has potential to compete with high-end (802.11-style) half-duplex links [7], however, silicon / PCB area and power consumption remain high.
c) A replica TX chain can be used to regenerate the SI in the digital BB and cancel it at RF, combined with digital cancellation [9]. However, its ultimate cancellation performance is limited by uncorrelated noise and distortion sources between the two TX chains, and by phase noise if separate LO signals are used for the TX chains [10].
d) A mixer-first transceiver with baseband noise-cancelling, duplexing LNA's can be used that intrinsically copy a transmit signal to their antenna port, while rejecting it in their output [11]. Placing the LNA's in the baseband allows complex signal processing to tune their SI-

rejection. Although very suitable for integration and capable of operating with a single-port antenna, the duplexing LNA's have limited capability to work with high TX powers [11] and the TX performance will be limited by the loss of the mixers.

As an alternative method, in [12] we demonstrated an SI-cancelling receiver for frequency-agile, low-power, short-range full-duplex. This paper provides more background information, implementation details, performance analysis and modelling of the presented design. It is structured as follows: First, we briefly review system considerations for FD and show how the proposed receiver topology emerges. Next, section III describes the implementation of the prototype SI-cancelling receiver. Section IV describes the measured performance and relates it to FD link capabilities. Section V concludes this work.

II. System Considerations and Proposed Architecture

The SI-cancelling receiver developed here aims to bring full-duplex to low-power, short-range communication devices. For this purpose, a TX power of 0dBm is assumed, a bandwidth of 16.25MHz (the active bandwidth of WLAN) and a 10dB RX noise figure. This results in an RX noise floor of roughly -90 dBm. Thus, in order not to degrade the noise floor, isolation and cancellation mechanisms combined should reliably reject the SI by at least 90dB. Furthermore, we assume that a compact antenna solution in a changing near-field can achieve a worst-case isolation of only 20dB, requiring 90-20 = 70dB from cancellation.

Figure 3a visualises an attempt to cancel the remaining SI after antenna isolation all in the digital domain. Assuming digital cancellation can only cancel the deterministic, linear part of the self-interference, TX EVM and SI-induced RX noise and distortion may still mask the desired signal [2]. To prevent this, roughly 70dB TX EVM and 70dB RX dynamic range (DR) would be required, which is not feasible in a low-power FD node.

Introducing a frequency-flat phase shift / attenuation based canceller at RF can improve RF SI-rejection to a level limited by the frequency-selectivity of the antenna interface, environment and the desired bandwidth (figure 3b). To further cope with frequency-selectivity in this architecture, the canceller would need to incorporate multi-nanosecond time or group delay (i.e. a non-flat phase response) [8], which may become costly in silicon area. However, in an indoor scenario, the reflections in the 2.4GHz ISM band are reportedly present at -40 to -50dB [13]. For an antenna interface with limited additional frequency-selectivity, a frequency-flat canceller at RF

may therefore reduce requirements on TX EVM, RX DR and digital cancellation to 90 - {40 to 50} = 40 to 50dB, which is much more feasible than 70dB.

As such, the useful attenuation range for the canceller in this system with respect to the TX power ranges from 20dB (worst-case SI from the antenna) to 50dB (best-case level of the reflections). As for the phase shift, a full 360° range is desirable since the absolute phase of the SI can assume any value depending on the antenna configuration. So the canceller may consist of 20dB fixed attenuation, about 30dB variable attenuation, and a full 360° phase shift.

For a frequency-flat canceller, the tolerable group delay δ of the antenna solution can be evaluated mathematically. Assuming optimum cancellation in the center of bandwidth BW, the phase error at the band edge equals $\phi_e = \delta \times 2\pi\text{BW}/2$, resulting in an SI-cancellation at the band edge of $\text{SIC} = -20\log_{10}(2\sin(\phi_e/2))$. Rewriting yields the tolerable group delay

$$\delta = \frac{2}{\pi\text{BW}}\sin^{-1}(\frac{10^{-\frac{\text{SIC}}{20}}}{2}) \approx \frac{10^{-\frac{\text{SIC}}{20}}}{\pi\text{BW}} \tag{1}$$

using a small-angle approximation. Here, SIC is the desired *worst-case* SI-cancellation (at the band edge). Similarly, it can be shown that when *band-integrated* cancellation is considered, the tolerable group delay increases by a factor $\sqrt{3}$. For the aforementioned 20 to 30dB SIC on top of 20dB isolation integrated over 16.25MHz BW, the tolerable group delay is 3.4 to 1.1ns. For the following system design considerations, such values are assumed feasible.

The focus of this paper is on the receiver. A full-duplex RX should realize a reasonable compromise between noise and SI-induced distortion. In other words, its SI-to-noise-and-distortion-ratio (SINDR) should be high for an optimum full-duplex link budget. SINDR is depicted in figure 3b.

Maintaining high in-band linearity under strong SI is crucial to obtain a high SINDR, which motivates interchanging the LNA and mixer and moving to a mixer-first architecture (figure 4a). Subsequently, the cancellation node may be moved to the analog baseband and the phase shift, attenuation and down-mixing can be combined in a single component, i.e. a Vector Modulator (VM) downmixer (figure 4b).

This topology taps the TX signal at the TX RF output, thus including TX impairments in the cancellation, relaxing TX EVM requirements by the amount of cancellation achieved. It cancels SI before the baseband amplifiers and ADC, relaxing their dynamic range requirements by the same amount. A fixed attenuator is added to match the VM range to the worst-case isolation of the chosen antenna solution and kept external for versatility.

The topology in figure 4b has high integration potential and as discussed, it is applicable to low-power, short-range full-duplex nodes. The following section discusses implementation details of the receiver prototype.

III. Implementation of an SI-Cancelling Receiver

This section describes the implementation of an SI-cancelling receiver in 65nm CMOS according to the topology of figure 4b. As explained in section II, to allow cancellation of residual SI, including delayed SI-components, in digital and uncover the desired signal, the RX should have very high SINDR, and thus high in-band linearity under cancellation of strong SI. This prevents the SI from inducing distortion that raises the RX noise floor and masks the desired signal. In the proposed topology, this puts very strict in-band linearity requirements on both downmixers, as they both have to process the maximum TX leakage at their inputs. Furthermore, to prevent RX clipping under strong SI, cancellation has to take place before amplification. Contrary to traditional systems, there is no TX-RX frequency separation, so filtering cannot be used.

Hence, both the main RX and the VM are based on highly linear passive mixers with series resistors into virtual ground nodes provided by transimpedance amplifiers (TIAs) [14]. Figure 5 shows an overview of the implemented receiver. The VM is a sliced version of the main RX, followed by static phase rotator switches that route the current of each slice into the four virtual grounds. This way, the SI currents are diverted through highly linear passive networks and only the residue is amplified. The number of slices and other design details are motivated next.

A. Resolution

The sliced VM principle is similar to the constant-g_m vector modulator presented in [15], but implemented with *resistors to a virtual ground* rather than *active transconductors*. The amount of slices of the VM determines the number of phase / amplitude constellation points it can cover and thus the amount of cancellation that can be achieved due to quantization effects. This is illustrated in figure 6. For n slices, the constellation consists of $n+1$ by $n+1$ points. The maximum quantization error occurs when the actual SI phase and amplitude represents a point right in the center of four VM constellation points. Normalizing the constellation to a square of 1x1, the quantization error has a magnitude of $q_e = \frac{\sqrt{2}}{2n}$. Since the VM has to cover a full circle of phase shifts, the cancellation range is the largest circle that can be drawn through the

constellation with maximum error q_e, which has a radius of $1/2 + 1/(2n)$. Thus, the worst-case cancellation given a number of slices is given by

$$\text{SIC [dB]} = 20 * \log_{10} \frac{\frac{1}{2} + \frac{1}{2n}}{\frac{\sqrt{2}}{2n}} = 20 * \log_{10}(n+1) - 3\text{dB} \quad (2)$$

As discussed in section II, a cancellation up to 30dB allows reducing the direct crosstalk to levels where frequency-selective components dominate the SI. Combined with practical constraints, a resolution of $n = 31$ slices was chosen, allowing 27.1dB cancellation[1]. 31 slices can be conveniently segmented and controlled with 5 bits.

B. Noise

Designs based on 50Ω resistive termination and 4-phase, 25% duty cycle mixing have a noise figure (NF) that is fundamentally limited to 3.9dB [16]. However, in the proposed design, the VM injects considerable noise current into the virtual ground nodes without contributing desired signal. Its noise contribution could be lowered by designing a weak TX coupler and scaling the VM impedance up from the 50Ω standard (i.e. weaker coupling of the SI into the RX path [8]), but in order to use standard external equipment, 50Ω matching was maintained also for the VM.

The VM noise depends on its setting. Analyzing this for all possible VM settings is mathematically involved, since each setting is a complex mapping of resistors and switches into each of the virtual ground nodes. However, three extremes can be analyzed to obtain upper and lower bounds for the NF:

1) The VM is disabled: the system acts as a conventional mixer-first receiver;
2) The VM is set to an I/Q corner of the constellation, i.e. all slices are configured equally and the VM essentially behaves like a regular mixer;
3) The VM is set to minimum amplitude, i.e. the center of the constellation, where half of the slices is set 180^o out of phase with the other half.

The latter point cannot be reached in practice, due to the odd number of slices, but given sufficient VM resolution it can be well approximated. Similarly, the second point (maximum amplitude) is not used in practice, since the VM will only use the highest amplitude it can achieve over the desired full phase circle (section III-A). However, both points provide useful bounds for the NF. Figure 7 depicts single-ended equivalent circuits in these three configurations, and their

[1]Slightly less than the 28.5dB mentioned in [12] as a result of more accurate calculation.

equivalent in-band LTI models for noise analysis according to [16]. For this analysis to be valid in-band, the time constants $(R_s + R_m + R_{sw})(1 + A)C_f$ and $R_f C_f$ are assumed much larger than $1/f_{LO}$, which is typically the case in this design. Out-of-band, the C_b shield the TIAs from high frequency IF components. For simplicity, the source impedances are considered resistive and frequency independent. Only thermal noise is considered.

In situation 1), the mixer can be represented by a resistor R_m+R_{sw}, due to the non-overlapping nature of the LO signals. The noise and impedance folding effects of the linear time-variant circuit are represented by a shunt resistance $R_{sh} = \frac{4\gamma}{1-4\gamma}(R_m + R_{sw})$ in the LTI equivalent [16]. Here, $\gamma = 2/\pi^2$. The feedback amplifier is modeled by a noiseless amplifier preceded by its input impedance $R_b = R_f/(1+A)$ and two correlated noise voltages $v_{n,amp}$ and $i_{n,amp}R_b$ Where $i^2_{n,amp}R^2_b = \frac{4kTR_f}{(A+1)^2} + \frac{v^2_{n,amp}}{(A+1)^2}$ [16]. The noise factor is then given by [16]:

$$F = 1 + \frac{R_m + R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left(\frac{R_s + R_m + R_{sw}}{R_{sh}}\right)^2 + \gamma\frac{R_f}{R_s}\left(\frac{R_s + R_m + R_{sw}}{\gamma R_f}\right) + \gamma\frac{v^2_{n,amp}}{4kTR_s} \times \left(\frac{R_s + R_m + R_{sw}}{\gamma R_f} + \frac{R_s + R_m + R_{sw} + R_{sh}}{R_{sh}}\right)^2 \quad (3)$$

In situation 2), the VM can be represented like the main mixer by a source resistance R_{s2}, a switch and matching resistance $R_{m2}+R_{sw2}$ and a shunt resistance $R_{sh2} = \frac{4\gamma}{1-4\gamma}(R_{s2}+R_{m2}+R_{sw2})$ accounting for the time variant effects. This network is effectively in parallel with the original shunt resistance, so we can replace R_{sh} in equation 3 by an equivalent resistor

$$R_{eq} = R_{sh}//R_{sh2}//(R_{sw2} + R_{m2} + R_{s2}) \quad (4)$$

In situation 3), the input of the VM can be considered a differential ground: the source resistance R_{s2} does not contribute any noise in this case, but the VM itself directly acts as a shunt resistor with value $R_{m2} + R_{sw2}$, which can be modeled in the LTI circuit as $R_{sh2} = \frac{4\gamma}{1-4\gamma}(R_{m2} + R_{sw2})$. The equivalent total shunt resistance now equals:

$$R_{eq} = R_{sh}//R_{sh2}//(R_{sw2} + R_{m2}) \quad (5)$$

The noise figure can be evaluated for the three scenarios by introducing practical values. R_s was kept at 50Ω for both inputs. R_f is chosen $1.5k\Omega$ for 24dB overall receiver gain. A two-stage, telescopic op-amp was used with $A = 1000\times$ open loop gain. The main noise contributors

of the op-amp are the input pair ($g_{m1} = 2 \times 23.4$mS) and the active loads of the input stage ($g_{m2} = 2 \times 12.8$mS). Assuming a noise excess factor of 1, the input-referred op-amp noise can be calculated as $v_{n,amp}^2 = 4kT(g_{m1} + g_{m2})/(g_{m1}^2)$. Taking into account a non-zero baseband impedance due to finite op-amp gain, matching is achieved by setting $R_{sw} + R_m = 48\Omega$ and $R_{sw2} + R_{m2} = 48\Omega$. The results are listed in table I.

Beside the analysis, simulations were performed at 2.5GHz LO frequency, with the real baseband amplifier, but ideal mixers, resistors and sources. C_f was chosen 8pF for 13MHz BW and $C_b = 10$pF capacitors were put on the virtual grounds to filter higher harmonics. Table I lists the simulated NF at 10MHz offset, to minimize the influence of flicker noise. Analysis and simulation are in close agreement. In conclusion, the VM contributes the largest amount of noise at small amplitude settings, and enabling the cancellation path degrades the system NF by up to roughly 6dB.

C. Linearity

This work considers SI-induced RX distortion as limiting for digital cancellation, since cancelling this in digital requires precise models of the TX, the channel and the RX distortion behavior, as well as added signal processing. Hence we target minimizing the SI-induced distortion. In this FD mixer-first design, both SI-induced second-order non-linearity (IM2) and third-order intermodulation (IM3) fall directly in the band of interest and deteriorate the system noise+distortion floor for desired signals. Thus, we aim for sufficient in-band IIP2 and IIP3 by design. Given the targeted 16.25MHz BW, 20dB worst-case isolation, and 12.3dB NF, figure 8a plots the required in-band IIP2 and IIP3 to keep the SI-induced IM2 and IM3 equal to the system noise floor, as a function of transmit power. For illustrative purposes, the case for a 6dB NF is also drawn. As motivated in section II, this work targets at least 0dBm TX power, resulting in in-band IIP2 and IIP3 requirements of roughly 20dBm and 50dBm, respectively. Note that we aim for sufficiently low distortion to achieve analog cancellation while preserving the noise floor. We do not pursue sufficiently low distortion to further increase the TX power, as this would again put unfeasible requirements on the TX EVM and TIA / ADC DR (see section II).

Ideally, for 0Ω switches and a perfectly linear 50Ω matching resistor, there is no signal swing across the switches and therefore no IM3-currents are induced by the SI before cancellation. The only source of IM3 are the TIAs that process residual SI and the (usually weaker) desired signal.

Therefore, every 1dB of cancellation of the SI would result in a 2dB reduction of the SI-induced IM3, boosting the effective IIP3 by 1dB. However, low-ohmic mixer switches are power-hungry to drive, resulting in a trade-off between power consumption and IIP3 for switched-resistor mixers. Assuming simple square-law behavior of the switch devices and ideal virtual grounds, the in-band linear and third order components can be computed to be $a_1 = (R_s + R_m + R_{sw})^{-1}$ and $a_3 = (-R_s R_{sw}^2)/(2V_{OD}^2(R_{sw} + R_s)^5)$, where V_{OD} is the overdrive voltage of the switches [17]. Then IIP3 $= \sqrt{(3/4)|a_1/a_3|}$. Using $V_{OD} = 800$mV and taking $R_s = 50\Omega$ and $(R_m + R_{sw}) = 50\Omega$, the IIP3 is plotted as a function of R_{sw} in figure 8b. For >20dBm IIP3, the design was implemented with 25Ω resistors, with the remaining 25Ω distributed over the switch resistance, virtual ground impedance and routing parasitics. The bulk of the mixer switches was tied to the baseband side for reduced on-resistance and better linearity. The multiplexer switches of the VM were sized wide and low-ohmic, since parasitics are absorbed in the baseband capacitance and since they are driven by static control signals. This allows negligible increase of the virtual ground impedance.

For low IM2, a fully differential structure was adopted for both mixers with carefully balanced parasitics, and a common centroid layout scheme was used for the VM slices.

The TIAs were not specifically designed for linearity, and therefore will dominate the system IM3 performance when cancellation is deactivated. However, they perform such that under 27dB cancellation, the mixers will dominate the IM3 performance by a large margin. In addition, the TIAs were further linearized by a differential negative conductance at their inputs [14]. While not strictly necessary for this application, it allows us to eliminate the TIA as a linearity bottleneck in measurements and study the raw linearity achieved by the mixers, even with cancellation disabled. Figure 9 shows an implementation detail of one fully differential VM slice for one LO phase, and one of the negative-conductance-assisted TIA's. The TIA's are implemented as high-gain, two-stage OTA's with a telescopic input stage and a push-pull output stage [14].

D. LO generation and input matching

The 25% duty cycle LO is generated by an on-chip divide-by-two and logic operations on the four resulting phases. The final stages of LO drivers are AC-coupled to the mixer switches to allow level shifting the LO signals for reduced switch on-resistance. Figure 10 shows the level shifting circuit for two clock phases and two switches. The AC coupling capacitors are slowly

charged by small switches during the intervals where the LO is low. The level shift voltage is set between 0V and mid-supply by a 5-bit R-2R DAC, allowing digital control of input matching. This allows good input matching over process spread. Independent DACs are used for the VM and the main mixer, to overcome any differences in e.g. layout parasitics. In measurements, the RX and VM were tuned for matching once and the resulting DAC values were used throughout.

IV. Measurement results

The design was implemented in 65nm CMOS; a die photo is shown in figure 11. This section describes the measured performance of the prototype.

A. Cancellation

The cancellation performance of the circuit was evaluated using an 802.11g-like TX signal of 52 tones with random phases in 16.25MHz centered at 2.5GHz. The SI channel was emulated by a commercial high-resolution vector modulator. Over 100 arbitrarily chosen phase / amplitude points were evaluated within the cancellation range of the VM, as shown in figure 12a. An iterative search algorithm based on received power minimization was used to find the VM setting for best cancellation for each point, shown in figure 12b. The residual SI power was measured for each point, relative to the maximum power the VM could cancel (i.e. the gray circle in figures 12a/b. The results, plotted in figure 12c, show better than 27dB cancellation which is very close to the calculated 27.1dB from section III-A. This is expected, since despite the minimal practical sizing of the VM slices, matching was found to be much better than strictly required for the 31-slice VM.

B. Noise

In the thermal noise limited region, a noise figure was measured of 6.3dB without cancellation enabled; 10.3dB with cancellation set for maximum SI (i.e. the VM is set to a point on the maximum circle it can cover) and 12.3dB when set for small SI (i.e. the VM is set to a minimum amplitude). These values correspond very well with analysis and simulation as listed in table I. The 1/f noise corner of the RX was measured to reside at roughly 2MHz.

C. Linearity

For a symmetrical point-to-point link based on this design, the available link budget[2] will at first increase linearly with increasing transmit power (i.e. an increasing SINDR, see section II). However, at some point the increasing SI will induce distortion in the RX that raises the noise floor, limits digital cancellation, and thus decreases the link budget again. This also holds under cancellation, due to the finite linearity of the RX and VM mixers. In other words, there is an optimum SI power for which the system achieves the highest SINDR and thus the largest link budget. To find this optimum, a two-tone self-interferer was applied and its power was swept under cancellation.

First, the IM3 products were observed. Under cancellation, an effective in-band IIP3 can be defined with respect to the SI [3]. The peak SINDR can then be calculated as:

$$\text{SINDR [dB]} = \frac{2}{3}(\text{Effective IIP3 [dBm]} - \text{Noise Floor [dBm]}) - 3 \text{ dB} \quad (6)$$

where the 3dB is due to the RX noise floor and SI-induced IM3 products adding as powers.

Due to the discrete nature of the VM, it is difficult to guarantee exactly 27dB cancellation, therefore the measurement was performed under 26dB cancellation, in order not to be optimistic. Figure 13a shows the results without cancellation. Drawing a noise floor in 16.25MHz allows deriving the SINDR. Figure 13b shows how the results change under 26dB cancellation. Again, the RX noise floor can be included to derive the SINDR (figure 13c). Both SINDRs are shown in figure 13d. Note that the performance has improved slightly with respect to [12], to reflect the most recent measurements. The peak SINDR of the system increases from 66.5dB without cancellation, to 71.5dB under cancellation, indicating a 5dB increase in link budget when cancellation is enabled. The point of maximum link budget has moved from -27.6dBm to -16.4dBm SI at the RX input. Also, if the system operates slightly above the optimum amount of SI (e.g. the external attenuator is chosen conservatively or the TX power is slightly larger than expected), the link budget degrades smoothly, whereas the original RX would suffer from output stage clipping (figure 13d).

[2] 'Link budget' in this work assumes 0dB SNR at the receiver and does not include any fading and AGC margins, to obtain a standard-independent metric.

[3] Effective in-band IIP3 is similar to effective out-of-band IIP3, as used in interference-cancelling FDD systems, e.g. [18]

The measurements show that the IIP3 increases from 9dBm to an effective 21.5dBm when cancellation is enabled: an increase of 12.5dB. The fact that the IIP3 does not increase by the full 27dB indicates that the linearity bottleneck has moved from the TIA to the nonlinear RX and VM switches. Since enabling the cancellation increases the effective IIP3 by 12.5dB but also increases the noise floor by 6dB, equation 6 shows why the 27dB cancellation only yields a 5dB link budget increase.

However, the main intention of the canceller was *not to improve link budget, but to relax TX EVM, TIA / ADC dynamic range and digital cancellation requirements*, and all of these are still relaxed by the full 27dB of cancellation, minus the 5dB link budget increase. Table II summarizes the effect of the cancellation on the link budget of the system, under the assumption of 20dB antenna isolation. Its main merit is bringing the digital cancellation, TX EVM and TIA / ADC dynamic range requirements down from an unfeasible 66.5dB to a realistic 44.5dB.

Given the optimum TX power based on IM3, the IM2 was evaluated. Referring to figure 8 at 3.6dBm TX power, 56dBm IIP2 would be required for IM2 equal to the noise floor. Measuring the beat component of two in-band tones, +60dBm IIP2 was measured, which is sufficient by some margin and similar to that achieved in other mixer-first designs. Note that in this mixer-first design, IM2 is dominated by the mixers and therefore is not reduced by cancellation. As such, defining an effective IIP2 is not useful. Since the design required a post-production routing fix, a limited number of functional samples was available and the IIP2 was not characterized over multiple samples.

In figure 13c, to find the SINDR, the fundamentals were extrapolated from the case without cancellation. This assumes that under cancellation, the SI does not compress the RX for the SI power range of interest. This can be validated by applying a third tone, representing the desired signal, and monitoring its conversion gain. Figure 14 shows the result: under cancellation, the RX can handle in excess of 1.5dBm of SI before the desired signal is compressed; at this point, the residual SI is strong enough to saturate the TIA, despite the cancellation. This is 24dB higher SI than without cancellation and justifies the extrapolation made in figure 13b/c.

As mentioned in section III-C, the TIAs can also be eliminated as linearity bottleneck by enabling the differential negative conductance present at their inputs. With the cancellation disabled, this allows us to observe the raw linearity of the main RX mixer, which results in an IIP3 of 19dBm. The fact that the effective IIP3 under cancellation is even 2.5dB higher, can

be explained by two phenomena: 1) distortion cancellation mechanisms occurring between the RX and VM; 2) the fact that cancelled SI does not cause signal swing on the virtual grounds, whereas received signal does. Note that the measurements in figure 13 and 14 were performed without negative conductance.

D. Broadband performance

Although the aforementioned results were obtained at 2.5GHz LO frequency, the receiver employs frequency-agile operation and cancellation principles. Figure 15 shows several performance characteristics over a broad range of LO frequencies. NF and RX gain are reasonably flat over the entire operating range from 0.15 to 3.5GHz. Due to the discrete nature of the VM, the cancellation performance varies, as expected, but always exceeds 27dB. Power consumption increases linearly with frequency with a static component, as expected.

E. Transmitter

The co-integrated transmitter is discussed separately in [19]. Like the RX, it features frequency-agile operation. For a 0dBm 802.11a output at 2.5GHz, it achieves -40dB EVM, which almost meets the 44.5dB requirement at 3.6dBm output as listed in table II. Further improving its EVM by e.g. pre-distortion is part of ongoing research.

F. Phase noise

Phase noise (PN) can be troublesome for FD [2], [10]: In our design, uncorrelated PN between the RX and the VM mixer would induce a noise floor relative to the SI power before cancellation. Assuming a typical PLL with e.g. -110dBc/Hz PN in 10MHz BW, its integrated in-band PN of -40dBc would hamper digital cancellation. A shared clock for RX and VM solves this issue, but if the TX mixer remains uncorrelated, a noise floor would still appear below the SI after cancellation. Therefore, all mixers in the system share a common LO source, resulting in PN rejection. Experiments detailed in [19] and subsequent analysis with different SI path loss models suggest sufficient PN rejection to realize the proposed 90dB link budget with a commercially available PLL, even in very reflective environments.

G. Image rejection

A concern of the proposed topology is image rejection: The RX and the VM process the full SI power, but ideally, the received image of the SI should be below the noise floor. As such, about 71dB image rejection is required from the mixers, which is not a feasible value. However, if the image rejection is over 27dB, it does not limit analog cancellation, and the residual image can be dealt with in digital cancellation [20]. The prototype achieves 37dB image rejection, sufficient for analog cancellation by a margin of 10dB, but the image must be accounted for in digital to reach the full 44.5dB digital cancellation potential.

H. Comparison

Table III compares this work to two previously published integrated FD receivers. For fair comparison, no antenna isolation is assumed for all designs. The peak SINDR of the other works was calculated using equation 6. The SI power at which the peak SINDR occurs is given by:

$$\begin{aligned}\text{SI [dBm]} = \text{Effective IIP3 [dBm]} \\ - 1/3 * (\text{Effective IIP3 [dBm]} - \text{Noise Floor [dBm]})\end{aligned} \quad (7)$$

where the noise floor depends on the NF and RX BW. Although this work features the highest peak SINDR, and thus the highest link budget potential given a fixed amount of antenna isolation, it should be noted that the architecture of [8] can theoretically achieve significant cancellation over a wide bandwidth even when the initial antenna isolation is high, thanks to its ability to address delayed SI components. Although the gain of this design is relatively low due to limited range of the BB feedback network, experiments using an external 10kΩ feedback network resulted in 39.3dB gain at the cost of a reduced compression level, but without compromising the peak SINDR.

I. Antenna experiments

To verify the claims of 20dB as a representative worst-case antenna isolation and -40 to -50dB as the level where frequency-selective components dominate the SI in 16.25 MHz BW, some experiments were performed with the transceiver, using a crossed pair of commercial WLAN dipoles as a simple FD TX/RX antenna pair. Connections were kept short to avoid introducing unnecessary propagation delay. Initial results are described in [21]. In a lab environment without

special precautions, this antenna solution provides typically 25dB isolation with 4ns peak group delay and 2.5dB amplitude variation. A typical measurement when combined with the proposed front-end showed 46dB combined effect of band-integrated isolation and cancellation (40.6dB at the worst band edge), with the remaining SI clearly dominated by frequency-selectivity and not limited by the cancellation potential of the receiver. Given sufficient TX EVM and ADC DR as discussed, these components can be further cancelled in digital. Also, heavily influencing the antenna near-field with a hand showed that 20dB is a reasonable worst-case isolation for this FD antenna. Further characterization of the transceiver in real-world scenarios and implementing digital cancellation is part of ongoing research.

J. Design improvements

Several improvements can be envisioned over this research-oriented design. Firstly, the 50Ω-matched VM, preceded by a fixed attenuator, injects considerable noise into the TIAs, which can be reduced by scaling the VM impedance up for similar attenuation. This also reduces the power tapped from the TX. Secondly, the BB feedback network can be easily modified to achieve more gain as mentioned in section IV-H. Furthermore, the high 1/f-noise corner decreases SNR for low-offset carriers in an OFDM system, but can be improved by e.g. scaling the TIA input stages.

V. CONCLUSION

This work presented an integrated self-interference (SI) cancelling receiver, aiming to bring in-band full-duplex wireless communication to compact low-power devices. Starting from full-duplex system considerations, we found that a phase / amplitude based SI-canceller in the analog domain is useful to improve upon low and varying antenna isolation.

The proposed receiver takes an attenuated copy of the transmit signal, and provides simultaneous tuneable phase shift, amplitude scaling and downmixing using a vector modulator (VM) downmixer, for SI-cancellation in the RX analog baseband. The main RX and VM are based on a highly linear switched-resistor mixer-first architecture, to cancel SI with highly linear passive circuits, prior to amplification of the residue. This keeps SI-induced distortion low and thus maximizes the digital cancellation and link budget potentials.

For the sliced VM, the cancellation performance was derived as a function of the number of slices. We also show how to analytically obtain upper and lower bounds for the setting-dependent noise performance of the receiver including VM. Other design choices, such as the vector modulator resolution, were also motivated. The SI-to-noise-and-distortion ratio (SINDR) of the system was defined as a crucial figure for link budget performance.

With only 20 dB isolation from the antenna, the prototype with 31-slice VM achieves up to 27 dB cancellation at 3.6 dBm TX power, without introducing distortion above the RX noise floor. Given its 12.3 dB worst-case noise figure with cancellation enabled, this results in up to 91.5dB link budget in a 16.25MHz bandwidth, enough for short-range links. Since the TX is inside the cancellation loop, and cancellation occurs before amplification, the 27dB cancellation reduces the requirements on TX EVM, baseband amplifiers and ADC to feasible levels. The entire system offers frequency-agile operation and cancellation from 0.15 to 3.5GHz LO frequency.

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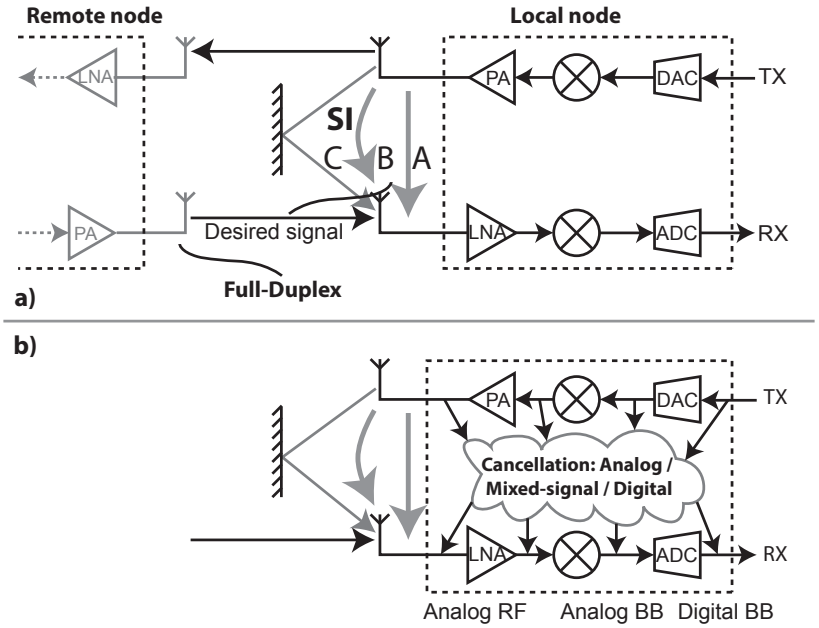

Fig. 1. a) Generic view of a full-duplex link between a local and a remote node, subject to 3 types of self-interference: A) Electrical crosstalk between TX and RX, B) RF coupling due to limited antenna isolation and a varying antenna near-field, C) SI reflected by the environment. b) Generic view of SI-cancellation in a single FD node, from various points in the TX chain to various points in the RX chain.

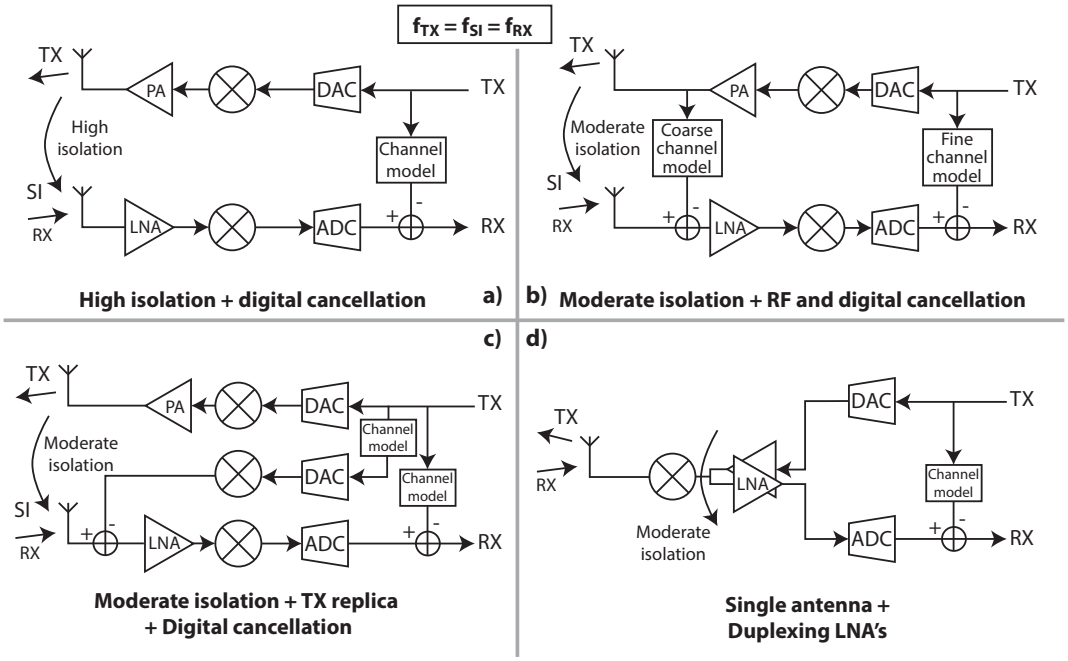

Fig. 2. Four recent self-interference cancelling topologies for integrated full-duplex radios.

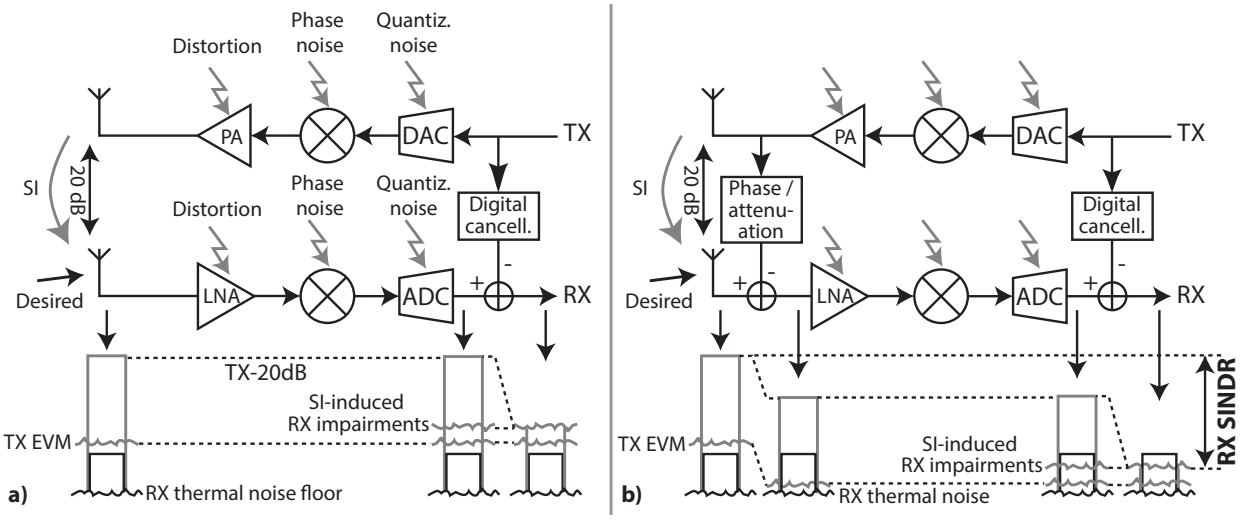

Fig. 3. Full-duplex nodes assuming a moderate 20dB antenna isolation: a) The SI is affected by transmitter and receiver imperfections, which limit cancellation in the digital domain. b) A phase / amplitude based canceller can enhance a moderately isolating antenna in the analog domain, relaxing TX EVM, RX dynamic range and digital cancellation requirements.

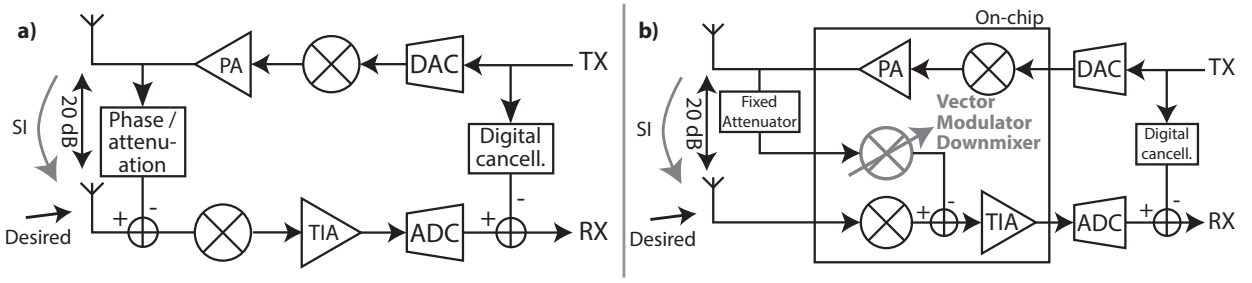

Fig. 4. a) A generic phase shift/attenuation based canceller preceding a mixer-first receiver; b) The cancellation node is moved to the analog baseband and the phase shift, attenuation and down-mixing are combined into a vector modulator (VM) downmixer.

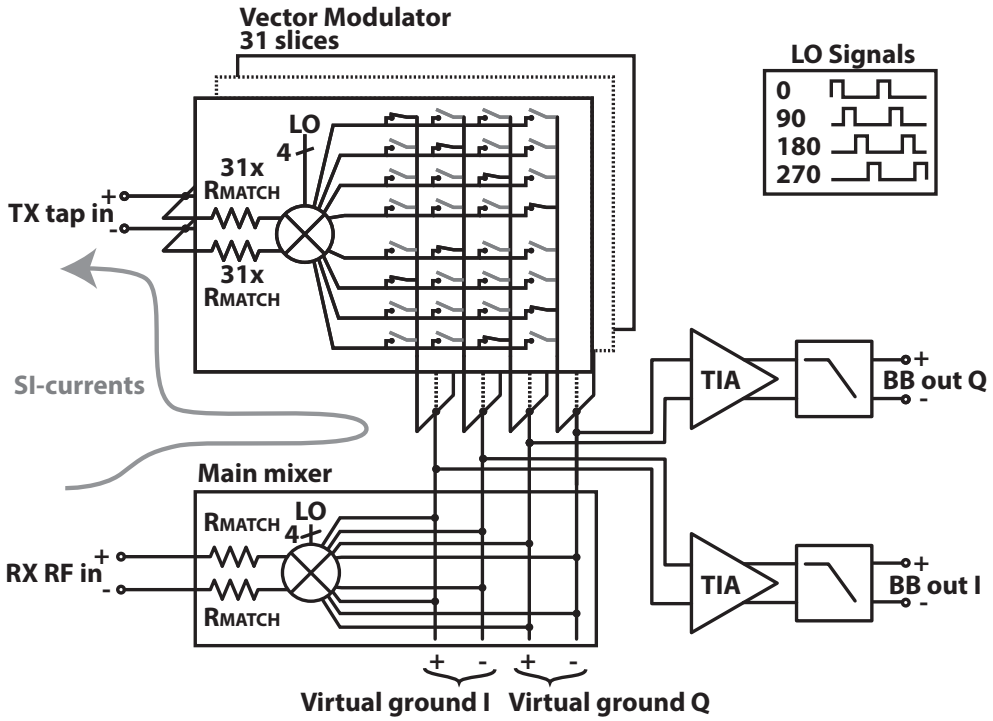

Fig. 5. Implementation details of the SI-cancelling receiver. The vector modulator (top) is a 31-slice version of the main receiver (bottom), each slice followed by static phase rotator switches. The VM diverts self-interference currents through linear passive networks before amplification.

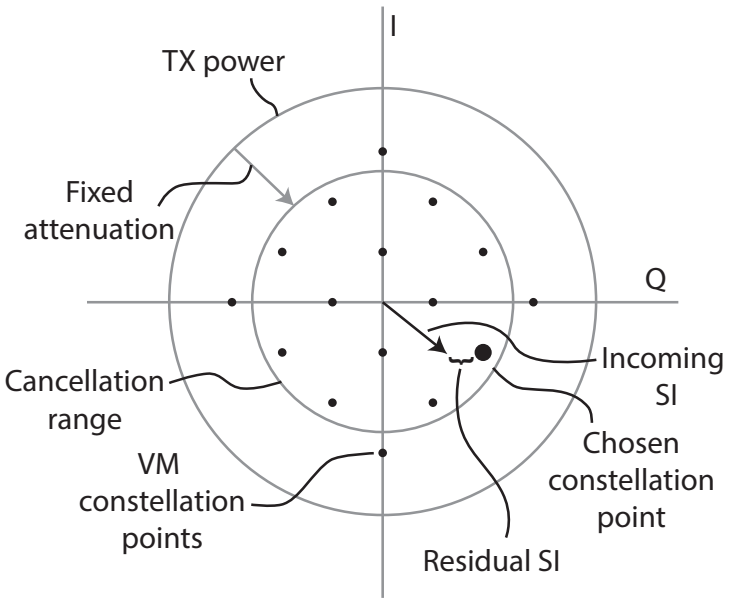

Fig. 6. The cancellation principle explained using a 3-slice VM (i.e. a 4-by-4 constellation): a fixed attenuation maps the VM cancellation range on the worst-case expected SI, the VM selects the phase / amplitude point closest to the incoming SI and some residual SI remains due to quantization effects.

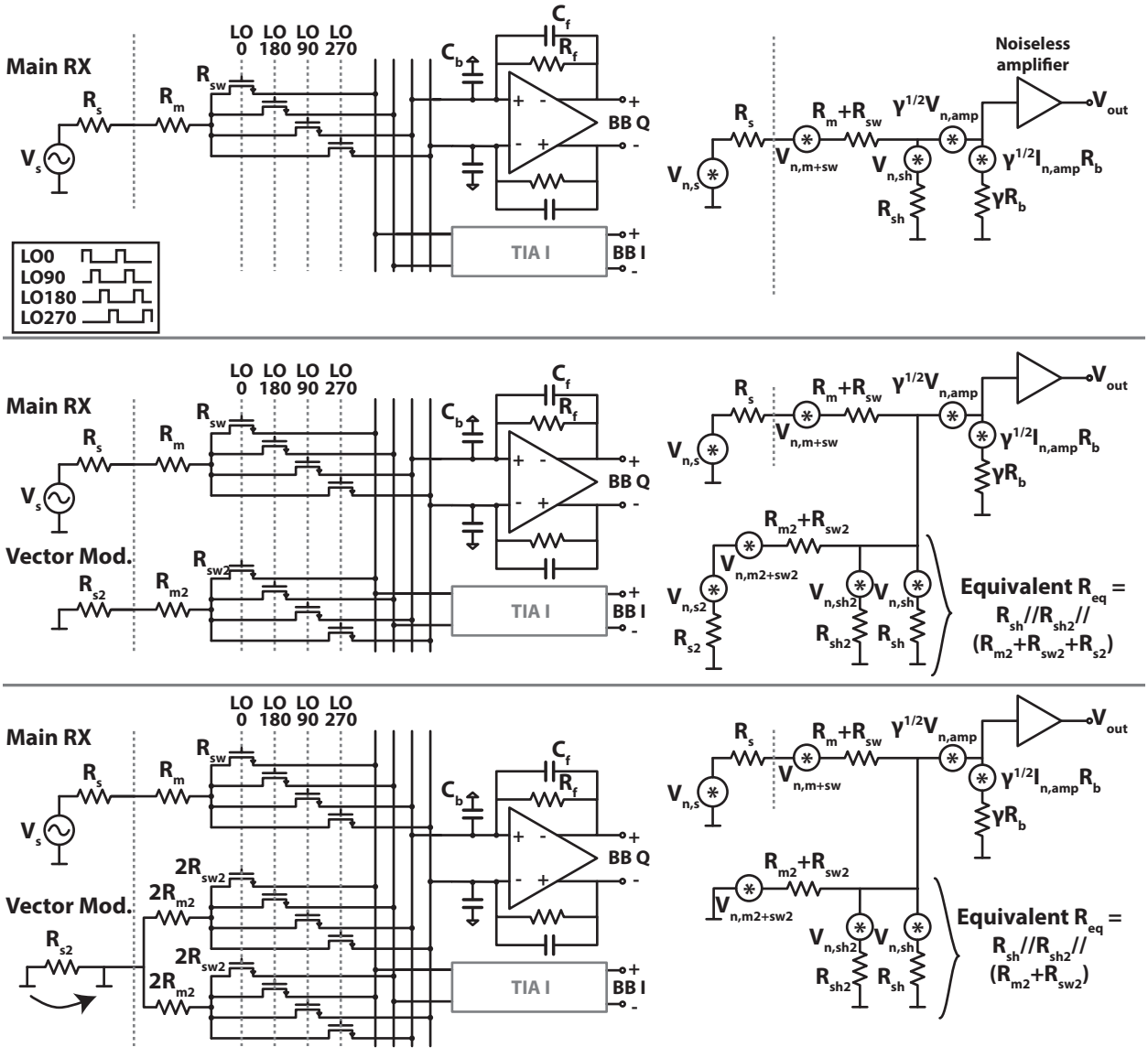

Fig. 7. Left: single-ended representations of the receiver in three configurations, Right: their equivalent noise models following the approach of [16]. Top: cancellation path disabled; Center: VM set to maximum amplitude; Bottom: VM set to minimum amplitude.

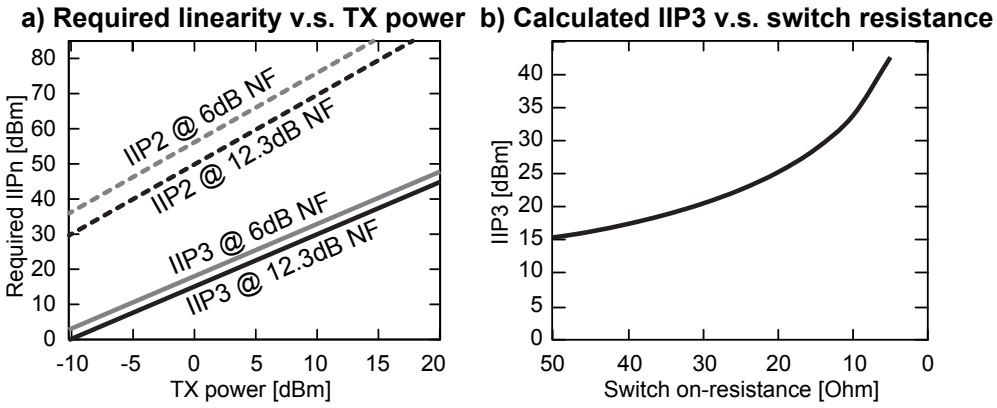

Fig. 8. a) Required IIP2 and IIP3 to keep the SI-induced IM2 and IM3 equal to the system thermal noise floor, as a function of TX power, assuming 16.25MHz BW, 20dB isolation and 12.3dB or 6dB NF; b) Theoretical IIP3 as a function of switch on-resistance.

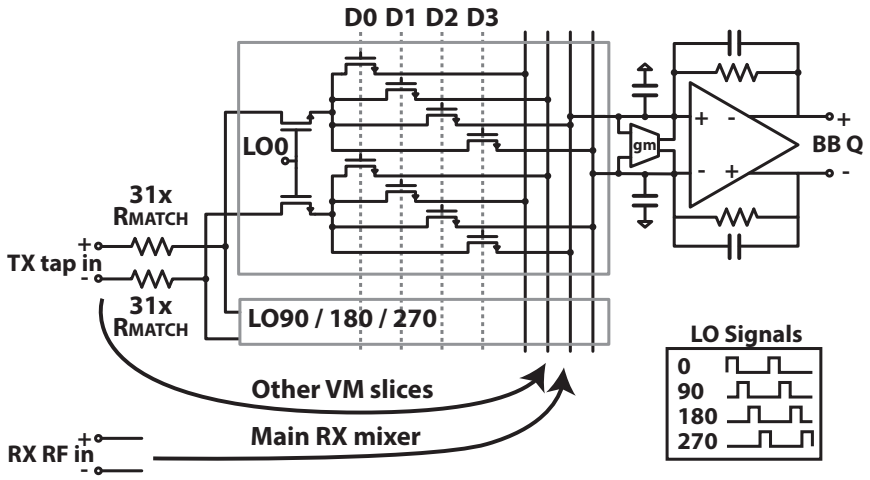

Fig. 9. Implementation details of one VM slice for one LO phase, and the TIA linearized by negative conductance.

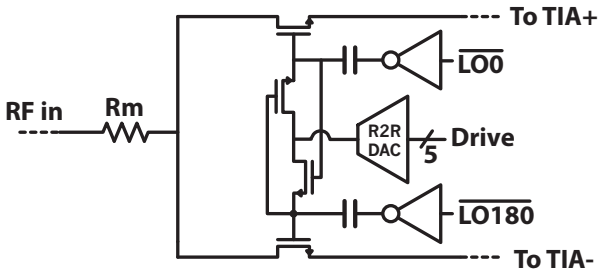

Fig. 10. 5-bit tuneable level shifting of the LO for tuneable input matching.

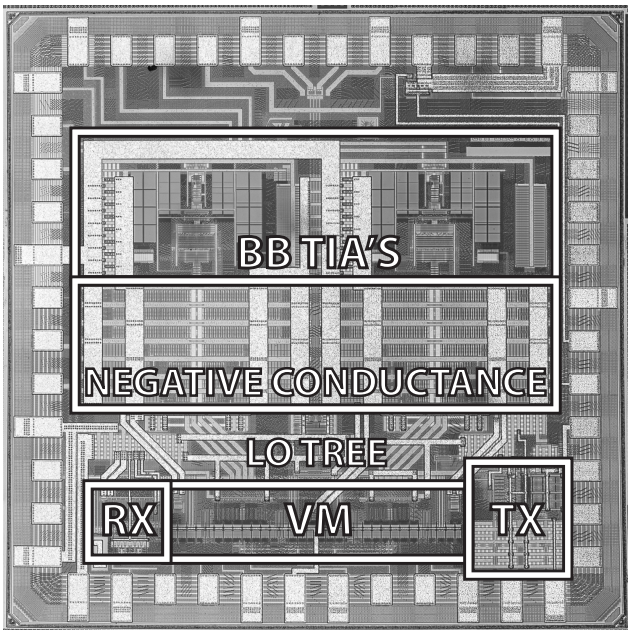

Fig. 11. Die photo with relevant blocks indicated. The 65nm design measures 1.4×1.4mm.

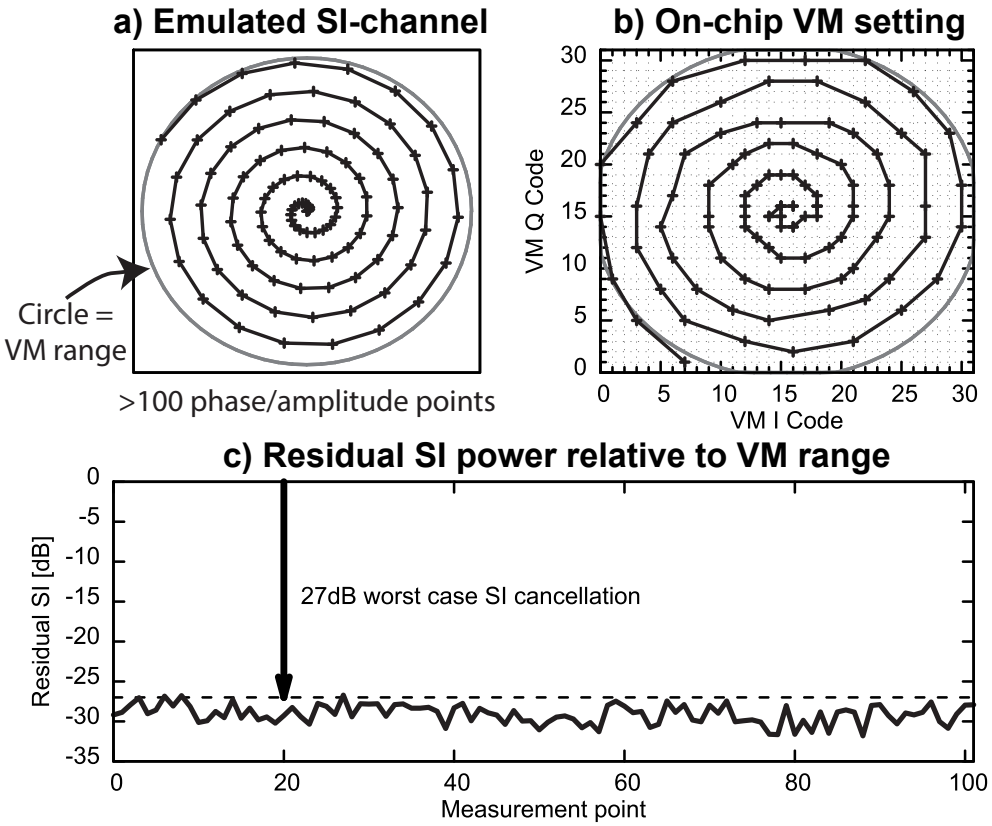

Fig. 12. a) Over 100 arbitrary, spiral-shaped phase/amplitude points emulate the SI channel; b) The on-chip VM finds the corresponding setting for best cancellation; c) The residual SI is always at least 27dB below the VM range (circle).

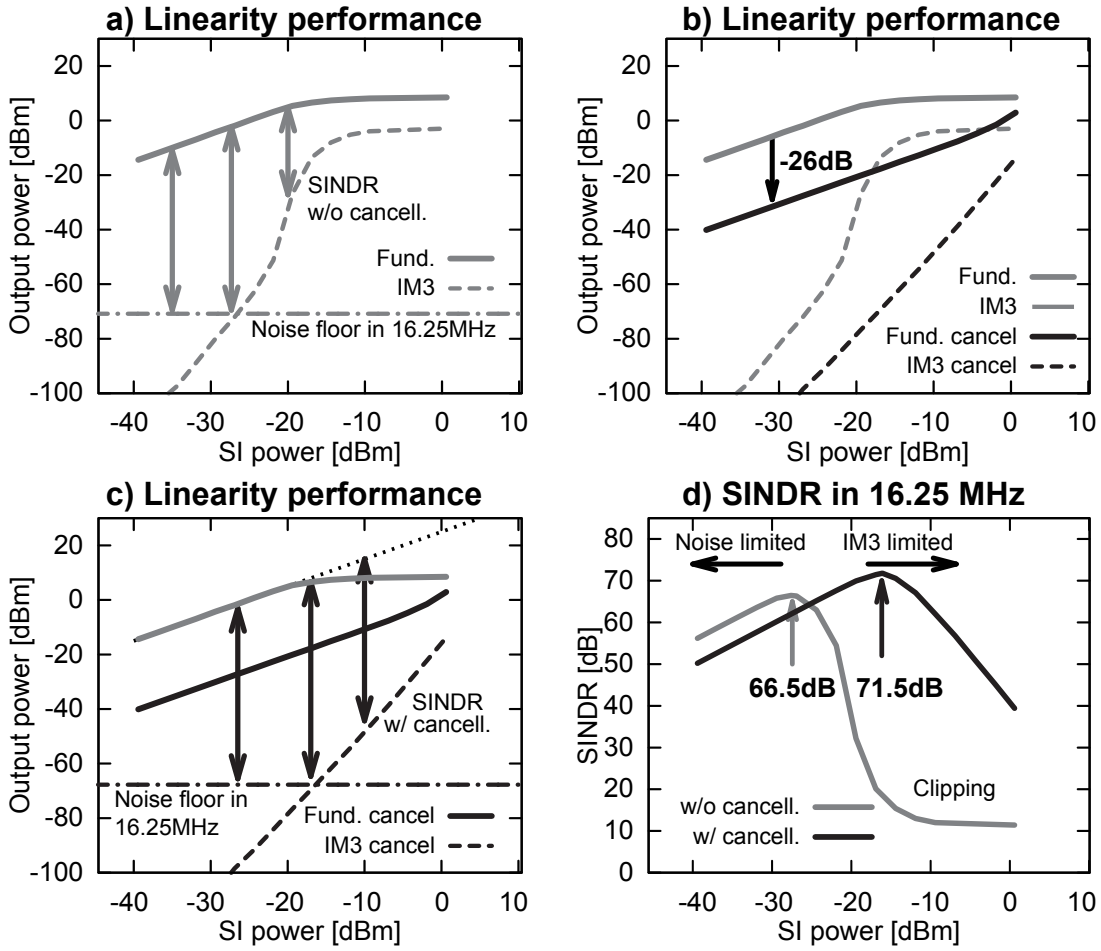

Fig. 13. Results of a two-tone linearity test: a) Cancellation disabled, including 16.25MHz noise floor and defining SINDR; b) Cancellation enabled; c) Cancellation enabled, including noise floor and SINDR; d) SINDR with and without cancellation for various SI powers. Note that the performance has improved slightly with respect to [12], to reflect the most recent measurements.

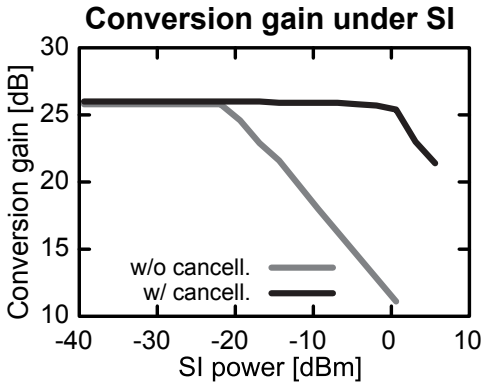

Fig. 14. Conversion gain for desired signal with increasing SI, without and with cancellation.

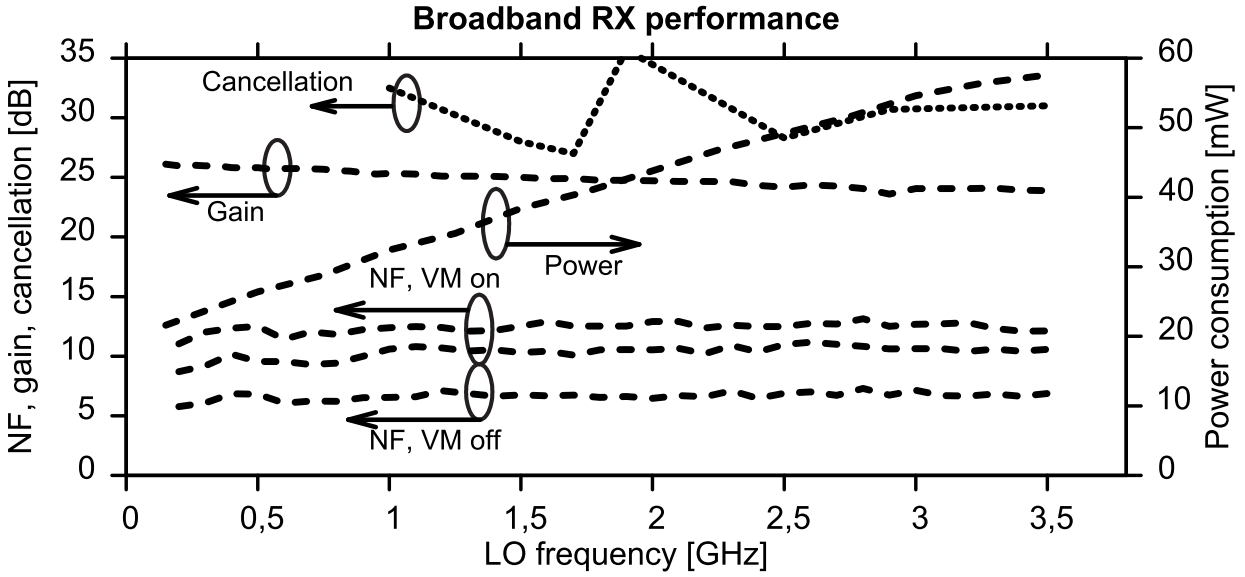

Fig. 15. Performance of the receiver over a wide range of LO frequencies.

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	Analysis	Simulation
VM disabled	6.4 dB	6.2 dB
VM maximum	9.8 dB	9.9 dB
VM minimum	12.3 dB	12.5 dB

TABLE I
CALCULATED AND SIMULATED RX NOISE FIGURE.

	Without cancell.	With cancell.
Maximum link budget (SINDR + Isolation)	86.5 dB	91.5 dB
Digital cancellation requirement (SINDR - Cancellation)	66.5 dB	**44.5 dB**
TX power @ max. link budget (SI + Isolation)	-7.6 dBm	3.6 dBm

TABLE II
SUMMARY OF CANCELLATION, NOISE AND LINEARITY EFFECTS ON OVERALL FULL-DUPLEX LINK PERFORMANCE, ASSUMING 20 DB ANTENNA ISOLATION.

	[8]	[11]	This work
Topology	Dual-port N-path filter based canceller + noise-cancelling receiver	Mixer-first architecture + Noise-cancelling duplexer LNA's	Mixer-first receiver + SI-cancelling VM-downmixer
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS
Supply	N/R	1.2V (LO) / 2.5V (BB)	1.2V
Operating freq.	0.8-1.4 GHz	0.1-1.5 GHz	0.15-3.5 GHz
Max. gain	42 dB	51-55 dB	24 dB
NF	5.7 - 6.3 dB (4.8 in HD)	5.5 dB	10.3-12.3 dB (6.3 in HD)
Power consumption	63 - 69 mW (RX) + 44 - 182mW (Canc.)	43 - 56 mW (incl. TX)	22 - 46 mW (RX) + 1 - 10 mW (Canc.)[1)]
Baseband BW	>30 MHz (-15 to +15)	6-192 MHz	24 MHz (-12 to +12)
In-band IIP3	-20 dBm	-32.7 dBm	+9 / +19 dBm (Neg. conductance off / on)[2)]
Effective in-band IIP3 with respect to SI	2 dBm	-0.7 dBm[3)]	21.5 dBm
SINDR in 16.25 MHz BW	62.5 dB peak @ -30.7 dBm SI	60.8 dB peak @-32.6 dBm SI	**71.5 dB peak @ -16.4 dBm SI**
Out-of-band IIP3	17 dBm	22.5 dBm	22.0 dBm
Resolution-limited SI Cancellation	N/R	N/A	27 dB
SI power @ 1dB RX compression	$\gg$-8 dBm	-17.3 dBm	>+1.5 dBm[4)]
In-band IIP2	+10 dBm	+7 dBm[5)]	+60 dBm
Effective in-band IIP2 with respect to SI	+68 dBm	+24 dBm[5)]	+60 dBm
1/f Noise corner	N/R	N/A	2 MHz
Practical cancellation details	20 dB worst-case in 25 MHz BW, 34 dB initial iso. from 1.4 GHz dipole pair, 8 ns peak group delay [6)]	33.5 dB in ~1 MHz BW[7)], with single-port antenna	15.6 dB worst-case, 21 dB integrated in ~16 MHz BW, 25 dB initial iso. from crossed 2.5 GHz dipoles, 4 ns peak group delay
Area	4.8 mm^2	1.5 mm^2	2 mm^2

Notes: Several values of [11] and this work were updated with respect to [12] to reflect the most recent data sets.
1) The transmitter adds 129mW at 2.5GHz, as detailed in [19]
2) Negative conductance gives about 1.5dB NF penalty [14]
3) From -38.7 dBm IIP3 and 38 dB IIP3 improvement @33.5 dB isolation
4) 135 kHz spacing [11], under 27 dB cancellation
5) Estimated from [11], figure 31
6) Cancellation was optimized for wide bandwidth
7) From [11], figure 25

TABLE III
COMPARISON WITH OTHER INTEGRATED FD TRANSCEIVERS, ASSUMING NO ANTENNA ISOLATION.