On the Trade-Off Between Quality Factor and Tuning Ratio in Tunable High-Frequency Capacitors

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***Abstract*—A benchmark of tunable and switchable devices at microwave frequencies is presented on the basis of physical limitations to show their potential for reconfigurable cellular applications. Performance limitations are outlined for each given technology focusing on the quality factor (Q) and tuning ratio (η) as figures of merit. The state of the art in terms of these figures of merit of several tunable and switchable technologies is visualized and discussed. If the performance of these criteria is not met, the application will not be feasible. The quality factor can typically be traded off for tuning ratio. The benchmark of tunable capacitor technologies shows that transistor-switched capacitors, varactor diodes, and ferroelectric varactors perform well at 2 GHz for tuning ratios below 3, with an advantage for GaAs varactor diodes. Planar microelectromechanical capacitive switches have the potential to outperform all other technologies at tuning ratios higher than 8. Capacitors based on tunable dielectrics have the highest miniaturization potential, whereas semiconductor devices benefit from the existing manufacturing infrastructure.**

***Index Terms*—Ferroelectric capacitors, field-effect transistor, losses, MEMS, microswitches, microwave technology, semiconductor devices, tuning, varactors.**

I. Introduction

MODERN versatile cellular systems support a large number of standards and frequency bands [1]. For multiband operation multiple nontunable circuits can be placed in parallel. However, to save precious space on a printed circuit board, a single electronic circuit with at least one tunable component can be designed. Tunable components can decrease the dimensions of electronic circuits by exploiting the circuits' reconfigurability. Reconfigurable circuits can tune in on multiple frequencies and can support different standards. The choice of a specific tunable technology involves many trade-offs such as cost, size, weight, performance, or availability.

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The aim of this paper is to compare relevant tunable capacitor technologies on the base of physical limitations to show their potential for future applications. The following technologies play an important role for this benchmark paper because of their miniaturization and low-power potential: dielectric varactors, varactor diodes (varicaps), micromachined capacitors radio frequency micromachined electromechanical systems (RF-MEMSs), integrated transistor-switched capacitors complementary metal–oxide–semiconductor (CMOS), and pseudomorphic high-electron mobility transistors (pHEMTs). This paper focuses on the following two crucial performance parameters: 1) the quality factor and 2) the amount of capacitive tuning (tuning ratio). If the performance for these criteria is not met, the application will not be feasible. Topics such as linearity, power handling, and temperature stability are important, but they can not be handled on such a general basis yet and still require a case-by-case study.

This paper will discuss the trade-off between loss (inverse quality factor Q) and maximum tuning ratio $\eta = C_{\max}/C_{\min}$ at frequencies mainly between 0.5 and 2 GHz for different tunable or switchable devices. In order to beat this trade-off new ideas could be essential. Simple 1-D device models are employed, assuming the devices have been optimized, with key data of Q and η from the literature of each device technology, to present the state of the art. Devices and technologies are difficult to compare: measurement conditions and design vary from case to case. $Q(\eta)$ curves for various conditions (breakdown, frequency or voltage) are presented here. However, we give generic comparison figures based on general physical principles wherever possible. The state of the art figure of merit ($Q(\eta)$) of each technology will be given in the discussion. This paper is subdivided as follows. In Section II, we discuss the operation principle, the corresponding loss model and design considerations to improve the device performance with key $Q(\eta)$ data from the literature. The lowest quality factor over the tuning range is given throughout this paper. In Section III the state of the art $Q(\eta)$ of each technology is given. All technologies are compared and discussed followed by the conclusions in Section IV.

II. Technologies

For each technology in this paper, parallel-plate capacitors are employed. The parallel-plate capacitance is expressed by

$$C = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A}{d} \tag{1}$$

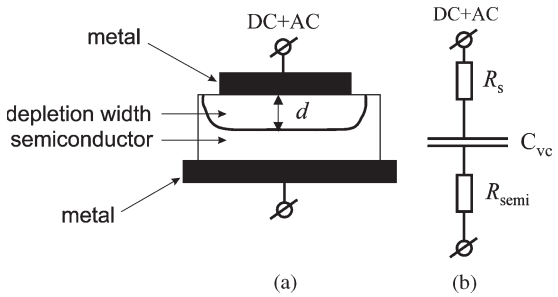

Fig. 1. (a) Schematic cross section of a Schottky varicap. The depletion layer d is controlled by the electric field and determines the capacitance value. (b) Loss model based on physical operation principles. The interconnect losses and electrode losses are given by $R_{\rm s}$, the capacitance of the varicap by $C_{\rm vc}$, and the resistance of the semiconductor by $R_{\rm semi}$.

with the permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, relative permittivity $\varepsilon_{\rm r}$, plate area A, and plate distance d. The capacitance can be varied as follows:

1) in dielectric varactors through a change in $\varepsilon_{\rm r}$;
2) in varicaps via a change in the depletion layer width d in the semiconductor;
3) in RF-MEMS capacitors by a change in the distance d between the two electrodes (planar capacitor) or a change in the effective electrode overlapping area A (comb-like structures), or by a moveable dielectric;
4) by a combination of switches and capacitors.

In the following sections, these four approaches are detailed further.

A. Varicaps

Varicaps or varactor diodes are the most widely used type of electrically continuously tunable capacitors. The capacitance can be tuned by varying the depletion layer width d due to a change in the dc bias, which is superimposed on an ac signal. A schematic cross section is depicted in Fig. 1(a), and the loss model based on the physical operation principles is shown in Fig. 1(b). The interconnect losses and electrode losses are given by $R_{\rm s}$, the capacitance of the varicap by $C_{\rm vc}$, and the resistance of the semiconductor by $R_{\rm semi}$.

An increase in dc bias increases the depletion layer width, reducing the capacitance. A large tuning range requires a large change in d and, thus, a large series resistance (low Q due to the lowly doped semiconductor) for the minimum depletion state. This trade-off becomes

$$\frac{1}{Q} = \omega C_{\rm vc,max} R_{\rm semi} = \frac{\omega \varepsilon_0 \varepsilon_{\rm r}}{d_{\rm min}} \int_{d_{\rm min}}^{d_{\rm max}} \rho(x)\, dx \qquad (2)$$

where ω is the circular frequency, $C_{\rm vc,max}$ is the maximum capacitance of the varicap at minimum depletion layer width $d_{\rm min}$, $R_{\rm semi}$ is the resistance of the semiconductor, $d_{\rm max}$ is the maximum depletion layer width, and ρ is the resistivity of the epilayer.

The loss is modeled by $R_{\rm s}$, $R_{\rm semi}$, and a capacitor [see Fig. 1(b)]. $R_{\rm s}$ can be minimized by using thick metals and substrate-transfer techniques [2]. $R_{\rm semi}$ is obtained by integrating ρ over the depth x of the doping profile from $d_{\rm min}$ to the backside electrode. The well-conducting backside electrode should begin at $d_{\rm max}$. Equation (2) yields $1/Q = \omega \varepsilon_0 \varepsilon_{\rm r} \rho (\eta - 1)$, where $\eta = (C_{\rm max}/C_{\rm min}) = (d_{\rm max}/d_{\rm min})$ for a uniformly doped varicap. The minimum and maximum depletion layer widths $d_{\rm min}$ and $d_{\rm max}$ both scale with the inverse square root of the dopant concentration. The maximum tuning ratio is thus independent of the dopant concentration for a homogeneous doping profile. $C_{\rm max}$ and the tuning ratio both increase for a doping profile that has the highest doping at the junction [6].

Inserting a power-law doping profile $\rho(x) \sim x^n$ in equation (2) results in

$$Q^{-1} = \omega \varepsilon_0 \varepsilon_{\rm r} \rho(d_{\rm min}) \frac{(\eta^{n+1} - 1)}{(n+1)} \quad \text{with } \eta = \frac{C_{\rm max}}{C_{\rm min}} = \frac{d_{\rm max}}{d_{\rm min}}. \qquad (3)$$

A uniform, i.e., abrupt, doping profile is obtained for $n = 0$, and a hyperabrupt for $n > 0$. A hyperabrupt profile $n > 0$ allows for a larger tuning range than a uniform doping profile due to a thinner depletion layer at 0 V.

The breakdown is determined by the critical electric field near the junction, provided that the doping distribution of the hyperabrupt profile does not vary too much. This critical electric field is affected by the doping at the junction as well. This dopant dependence in the critical field is used in our $Q(\eta)$ calculations described further in this section.

An exponent of $n = 2$ yields low distortions when two varactors are used in an antiseries configuration [3]. The product $\varepsilon_0 \varepsilon_{\rm r} \rho(d_{\rm min})$ can be regarded as a figure of merit, which is similar to the case of the semiconductor switches. The (maximum) conductivity $\rho(d_{\rm min})$ is limited by the maximum achievable dopant concentration before breakdown or tunneling occurs (see further in this section). An excellent value of $\varepsilon_0 \varepsilon_{\rm r} \rho(d_{\rm min}) = 4$ fs seems achievable with very high peak doping levels of up to 10^{18} cm^{-3} in Si [3].

Equation (3) gives the $Q(\eta)$ function for a given doping profile. The tuning range of a given diode can be traded for quality factor if only a part of the tuning range is used, namely, between breakdown and a nonzero reverse bias. Another option is to connect a high-quality-factor fixed capacitor in series as is anyhow needed in many applications for the application of the bias-voltage. In this case, the trade-off has the same shape as (3) with $n = 0$ for any doping profile. However, the best trade-off $Q(\eta)$ will be obtained if the dopant concentration is optimized for each maximum tuning ratio $\eta_{\rm max}$ separately. The following paragraph describes the calculation for abrupt $(n = 0)$ Si and GaAs varactors based on the dependence of the breakdown field and conductivity on the dopant concentration.

The conductivity was calculated from the mobility using the empirical model by Masetti *et al.* [4, eq. (1)] for arsenic doping in Si (highest mobility). The same model was fitted to the data for GaAs, taken from [5, Fig. 18]. The obtained fit parameters are $\mu_0 = 1900$ cm^2/V $\cdot$ s and $\mu_{\rm max} = 7600$ cm^2/V $\cdot$ s. The remaining mobility parameters in the model were left constant as in [4]. The minimum and maximum depletion layer width and the breakdown voltages were calculated using the formulas given by Sze and Ng [5, eqs. (23), (101), (102), and (104)]. Finally, the dependences can be inserted in eq. (3). The results are the dependences of the quality factor Q and

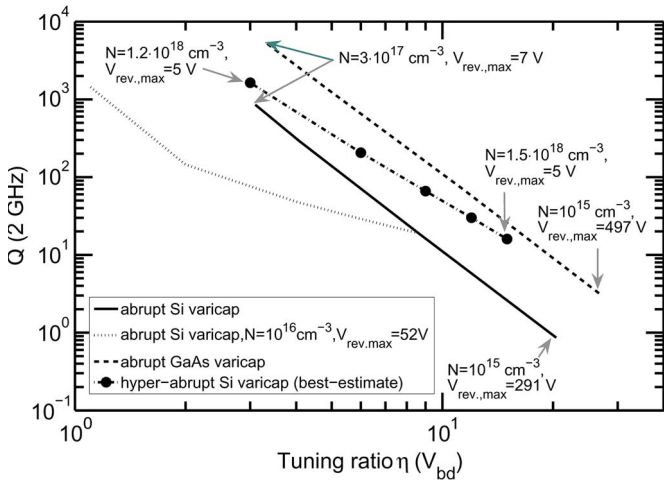

Fig. 2. Trade-off between quality factor Q and maximum tuning ratio η calculated for idealized 1-D varactor diodes at 2 GHz. (Solid line), Abrupt Si varactors (Dashed line), Abrupt GaAs varactors (Dash-dotted line) and Hyperabrupt varactors. The corresponding dopant concentrations N and reverse breakdown voltages $V_{\mathrm{rev,max}}$ are indicated to selected points on the lines. The dotted line shows an abrupt Si varactor with fixed dopant concentration of 10^{16} cm^{-3}, in which only a part of the tuning range is used by demanding a minimum bias voltage.

the maximum tuning ratio η on the dopant concentration N, which are parametrically plotted in Fig. 2 for abrupt Si and GaAs diodes. Increasing the dopant concentration increases the quality factor but lowers the breakdown voltage and, hence, reduces the tuning range. If the dopant concentration is very high, tunneling can occur at the junction so that the tuning range is further reduced. In Si(Ge), this will occur above $N > 3 \times 10^{17}$ cm^{-3} [6]. The plots are therefore not plotted beyond this level. The lowest dopant concentration was chosen so that Q was in the range of 1–10. The calculated $Q(\eta)$ data for Si are close to what is postulated by the International Technology Roadmap for Semiconductors from 2012 [7]: $Q >$ 50 at 5 GHz (corresponds to $Q > 125$ at 2 GHz) for $\eta > 5.5$.

The functional dependence of $Q(\eta)$ can be approximated by $1/Q \sim \eta^{n_a+1}$, with $n_a = 2.6$ for Si for $\eta \approx 4$–10 and $n_a = 8/3$ for GaAs for $\eta > 4$. It is obtained by fitting the dependence of the mobility on the dopant concentration with a power law and assuming large tuning ratios. It should therefore fit best to low dopant concentrations. Although eq. (3) does not include the optimization of the breakdown voltage, it can fit the results by using a modified exponent $n \approx 2.6$ instead of $n = 0$ for abrupt varactor diodes. This, again, confirms that the choice of optimizing a diode for the needed tuning range is better than reducing the tuning range by using only a part of the $C(V)$ curve. The second case is also plotted in Fig. 2.

Hyperabrupt varactor diodes can be optimized for the maximum tuning range not only by the doping level, but also by the shape of the doping profile. Such a study was done by Huang *et al.* for $n = 2$ [3]. The best reported values for a constant reverse breakdown voltage of 5 V are plotted in Fig. 2. All data points have a maximum dopant concentration of approximately 10^{18} cm^{-3} at the junction. A higher reverse voltage does not lead to a better $Q(\eta)$ trade-off for the higher tuning ratios [3]. The resulting $Q(\eta)$ curve can also be fitted by (3), with $n \approx 2$ and $\varepsilon_0 \varepsilon_r \rho(d_{\min}) \approx 4$ fs. Hyperabrupt varactors

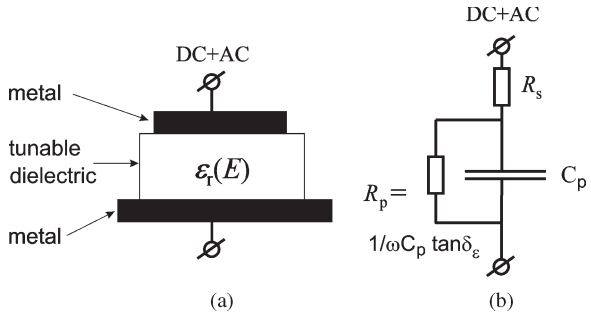

Fig. 3. (a) Schematic cross section of a metal–ferroelectric–metal capacitor. A change in the electric field E between the parallel metal plates affects the ε_r of the ferroelectric. (b) Loss model. The series resistance of the interconnect loss and electrodes is given by R_s, the inverse of the conductivity of the dielectric by R_p, and the ferroelectric capacitance by C_p.

can have a better $Q(\eta)$ trade-off, but the functional shape of the trade-off is similar to that of Si diodes. The performance of hyperabrupt GaAs varactor is expected to be higher than that of Si, which is analogous to abrupt varactor diodes. It should be noted that for high quality factors ($Q > 100$), additional losses from the electrode connections become important.

B. Dielectric Varactors

Another type of continuously tunable capacitors are dielectric varactors. The permittivity changes when a voltage is applied to the capacitor. Dielectric varactors are the smallest tunable capacitors due to their high permittivity. Parallel plate metal–insulator–metal (MIM) capacitors (see Fig. 3) have low fringing fields, a high capacitance density, and a low tuning voltage.

The relative permittivity of some materials, notably those with a high permittivity like ferroelectrics, e.g., $Ba_xSr_{1-x}TiO_3$ (BST), change by applying a nonzero dc bias field due to the saturation of the dielectric polarization [8]. A higher electric field decreases the permittivity. Nonferroelectric but, nevertheless, tunable dielectrics with a high permittivity exist, e.g., with a pyrochlore phase like $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN). Liquid crystals are representative of a tunable dielectric with a low dielectric constant [9]. However, the tuning ratio is limited to the low maximum permittivity since the minimum permittivity is above 1. The tuning ratio in these components is $\varepsilon_{\max}/\varepsilon_{\min}$.

The capacitance of the tunable dielectric C_p is not ideal. The dielectric loss $(\tan \delta_\varepsilon)$ and the interconnect and resistive electrode loss (R_s) cause dissipation (Fig. 3). The series resistance of the interconnects can be minimized by small patterns and thick metals with a high conductivity. The latter also holds for the electrodes. Within the dielectric, the coupling of ion displacements to the electrical field cause losses. Ferroelectric materials are mainly used in their paraelectric state in the temperature region above the Curie temperature because of lower losses. The tuning ratio in the ferroelectric phase, which exists in the temperature region below the Curie temperature, is higher, at the cost of higher losses due to irreversible domain wall movements. Since ferroelectric materials have piezoelectric or electrostrictive properties, a bulk acoustic wave will be exited if a dc electric field is applied. The layers of the capacitor should be chosen in such a way that the acoustic

wave is suppressed at the operating frequency. Alternatively, the materials can be used for acoustic filters [10], which could even be tunable [11]–[13].

The high nonlinear permittivity of most tunable dielectrics is caused by atomic displacements. Acoustic losses due to the phonon excitation by the atomic movements are the limiting (intrinsic) loss factor. First, a simple model for the intrinsic losses is given. Then a phenomenological $Q(\eta)$ is proposed based on literature data that includes extrinsic losses, e.g., by defects in the thin layers.

Assuming a bias-field-induced quasi-Debye mechanism for the intrinsic losses [14, eq. (3.34)], a trade-off, given by

$$Q^{-1} = \omega\tau_d(\eta - 1), \quad \text{with } \tau_d = AI(E_0) \tag{4}$$

can be derived between the quality factor Q and the tuning ratio η. The angular frequency ω should be well below the phonon damping frequency (ca. 100 GHz) [14]. The parameter I [14] depends on the tuning field E_0 and is in the order of 1 for small fields (tuning ratio η close to 1). The parameter A is expected to be in the order of magnitude of 1000 fs [14]. The measured literature data from Fig. 4 above 1 GHz correspond to values of $\tau_d = 100$–2000 fs. Equation (4) predicts the highest losses at a high tuning field because, then, the acoustic coupling is strongest. Single crystals often follow this behavior. However, many thin-film measurements show the opposite dependence: the losses are lowered at high fields. Defects, stress distributions, interfaces, and a resistive electrode design are possible root causes. Some "defects" such as ferroelectric domains will not contribute to losses if fully polarized and oriented. In general, careful processing measures should be taken to minimize bad interface layers to the film, porosity, and cracks, which could decrease Q. A thin dead layer (low-k dielectric layer between the electrodes and the high-k dielectric) also reduces the tuning ratio. The capacitive test structures should be small in physical size to increase the Q of high permittivity ferroelectric capacitors, as discussed in [15]. The time-dependent polarization relaxation in the Curie-von Schweidler law exhibits itself (after Fourier transform) as a dispersion in quality factor with respect to frequency $Q \sim \omega^{-\beta}$, and is a less severe frequency dependence than predicted by a Debye model. Limited experimental data for BST and BZN show frequency dependences β even below 0.33 [16], [17], [21]. Therefore, a phenomenological approach was chosen.

Data on thin-film ferroelectrics, using different deposition techniques, which have resulted in a high tunability and low losses, were collected for parallel-plate MIM capacitors at 1 MHz for $Ba_xSr_{1-x}TiO_3$ (BST) [17]–[25]. Data of BST between 1 and 10 GHz are given in [17] and [21]. For the nonferroelectric dielectric BZN, data are indicated in [26] and [27]. Many other papers exist on microwave losses in thin dielectric films, but the authors have chosen only the papers with the best $Q(\eta)$ values of parallel-plate MIM capacitors with electrodes that are realistic for miniaturized devices. If we assume that the losses of dielectric varactors will only slightly increase with frequency following a Curie–van-Schweidler law after Fourier transform, then the low-frequency results pose an upper limit to the high-frequency performance (see Fig. 4).

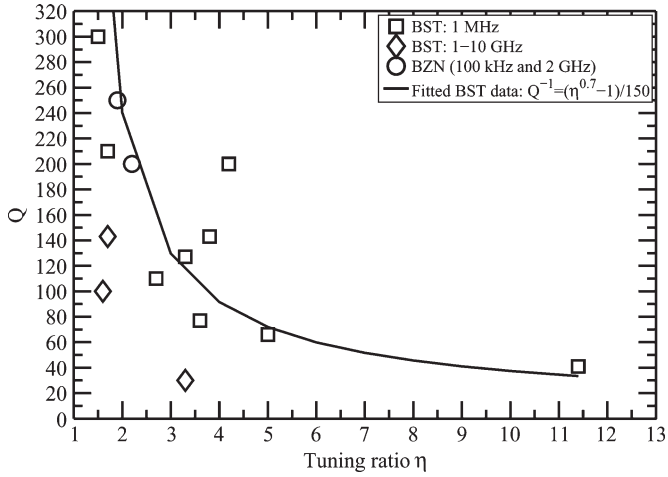

Fig. 4. $Q(\eta)$ results based on a literature survey on the performance of dielectric parallel-plate MIM varactors. The solid line is a fit to the best reported measurement results of ferroelectric varactors (BST, squares) at 1 MHz [17]–[25]. Data of BST for 1–10 GHz are plotted as diamonds [17], [21]. Varactors based on the nonferroelectric dielectric BZN are indicated by circles [26], [27]. The BST data indicate a $Q(\eta)$ trade-off.

Experimental results show a weaker $Q(\eta)$ dependence of than eq. (4) predicts. We attribute this difference to extrinsic losses in polycrystalline material.

The low-frequency $Ba_xSr_{1-x}TiO_3$ data can be fitted by

$$Q^{-1} = (\eta^{0.7} - 1)/150 \tag{5}$$

(see Fig. 4). Data at microwave frequencies in some cases come close to the low-frequency data. This is another indication that the losses are still dominated by extrinsic losses and less by intrinsic losses as described by eq. (4). The $Q(\eta)$ plot shows the limiting (fitted) curve of what could be achieved if you increase the tuning field up to breakdown. The data also suggest that there is still room for improvement by reducing the extrinsic defects.

C. Semiconductor-Switched Capacitors

Semiconductor technologies such as PIN diodes, CMOS switches, and pHEMT switches offer high performance at RF frequencies. PIN diodes dissipate considerable power in the ON state and are therefore left out in this paper. Although they can have a good high-frequency performance.

A transistor-switched capacitor is basically a transistor in series with a nontunable (linear) or a tunable capacitor (see Fig. 5).

Typically, a nontunable capacitor is used due to its higher Q-factor. High-quality MIM capacitors are available that have negligible small losses with respect to the losses of the switch. Such capacitors have dielectrics with a low dielectric constant and low losses, such as SiO_2, Si_3N_4, and Al_2O_3, and are connected with highly conducting electrodes such as Al, Au, and Cu. The transistor is employed to switch a capacitor ON and OFF. In the OFF state, the parasitic capacitance of the switch determines the minimum capacitance value. In the ON state, the transistor resistance determines the Q of the switch–capacitor configuration. We assume that the switch is connected to an

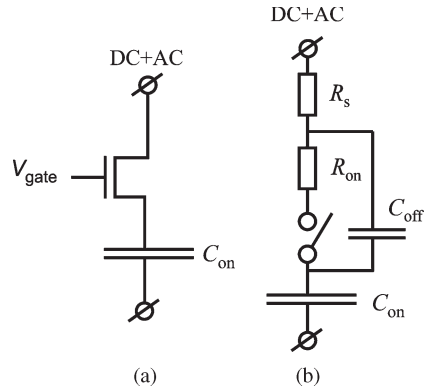

Fig. 5. (a) Schematic of a transistor in series with a capacitor. If sufficient gate bias $V_{\rm gate}$ is applied on the transistor, a channel will be formed between the source and the drain, connecting the capacitor to the circuit. (b) Loss model of the transistor-switched capacitor. If the switch is closed, $R_{\rm ON}$ will dominate the performance. If the switch is open, the OFF-capacitance $C_{\rm OFF}$ will dominate the minimum capacitance. The capacitance C is assumed to be an ideal capacitor, e.g., a low-loss MIM capacitor.

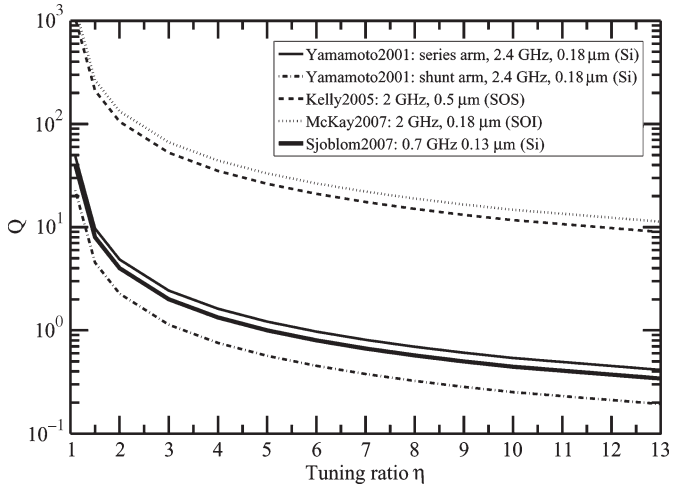

Fig. 6. Performance of CMOS switches in terms of Q and η at 0.7 GHz (0.13 μm Si [28]), 2 GHz (0.18 μm SOI [30] and 0.5 μm SOS [31]), or 2.4 GHz (0.18 μm Si [29]) based on a literature survey. The measurement results from the literature are performed on Si, SOI, or SOS. The product of $R_{\rm ON}C_{\rm OFF}$ of the CMOS switches from literature are filled in eq. (6), which results in the curves above. The Q decreases with increasing η.

ideal capacitor. Varying its value yields the trade-off between the tuning ratio η and the quality factor Q in the ON state. In the model of Fig. 5, the ON state yields a lower Q than the OFF state so we take the lower value in the ON state for comparison. A low ON-resistance $(R_{\rm ON})$ is thus crucial for a high-Q-switched capacitor array.

In this section, we discuss CMOS and pHEMT switches. We assume that $R_{\rm ON} \gg R_s$. The $Q(\eta)$ trade-off for CMOS and pHEMT switches becomes

$$Q^{-1} = \omega R_{\rm ON} C_{\rm OFF}(\eta - 1) \tag{6}$$

which is the same expression as for uniformly doped varicaps. Equation (6) has been fitted to the following literature data.

1) CMOS switches, on 0.13 μm Si at 0.7 GHz [28], on 0.18 μm Si at 2.4 GHz [29], on 0.18 μm silicon-on-insulator (SOI) at 2 GHz [30], and on 0.5 μm silicon-on-sapphire (SOS) [31] in Fig. 6;

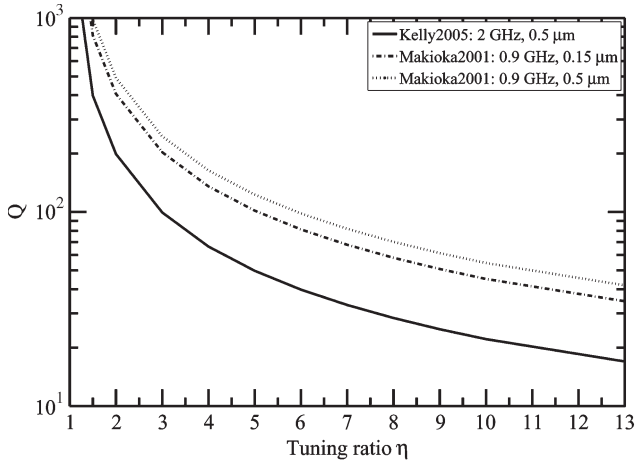

Fig. 7. Performance of pHEMT switches in terms of Q and η at 0.9 (0.15 μm and 0.5 μm [32]) or 2 GHz (0.5 μm [31]) based on eq. (6) and a literature survey. The measurement results from the literature are performed on Si, SOS, and SOI. The product of $R_{\rm ON}C_{\rm OFF}$ of the pHEMT switches are filled in (6), which results in the curves above. The Q decreases with increasing η.

2) pHEMT switches, on 0.5 μm GaAs at 2 GHz [31] and on 0.15 and 0.5 μm GaAs at 0.9 GHz [32] in Fig. 7.

The best figures of merit $R_{\rm ON}C_{\rm OFF}$ are reported for the case of a 0.5-μm CMOS switch on sapphire $R_{\rm ON}C_{\rm OFF,CMOS} =$ 750 fs [31] and a 0.5-μm pHEMT switch $R_{\rm ON}C_{\rm OFF,pHEMT} =$ 360 fs [33].

In CMOS switches N-channel MOSFETS are preferred because of a low $R_{\rm ON}$. The width of the channel needs to be optimized [34]. A large width reduces $R_{\rm ON}$ and increases to a certain extent. If the width becomes too large, then the capacitive coupling to the substrate will reduce the Q.

In pHEMT switches, channel doping decreases the $R_{\rm ON}$ at the cost of an additional parasitic capacitances between the source and drain, reducing the isolation in the OFF state [35].

D. RF-MEMSs

RF-MEMSs [36] contain movable parts and can be configured as miniaturized relays or continuously tunable capacitors. RF-MEMS switches have a relatively large physical size, compared to the other devices discussed earlier, due to the actuator that moves the mechanical parts. The first case is similar to semiconducting switches and will be briefly discussed at the end of this section. In the second case, the geometry of a capacitor is varied. A compact version is a planar electrostatic RF-MEMS capacitive switch, where the RF capacitor is also the electrostatic actuator (see Fig. 8).

The capacitance is tunable by varying the distance d between the top electrode and the dielectric, by a dc bias stimulus superimposed on an ac signal, or by a separate actuator. This principle also holds for vertical 3-D MEMS like comb structures. The combs move in-plane and varies the overlap area A of the electrodes. IDC capacitors in MEMS technology have low parasitic capacitances due to the use of air as a dielectric, and the interdigitated fingers have a very large aspect ratio, so that they become tilted "MIM capacitors" by 90°. Rotational movement like in manual trimming capacitors is less suited

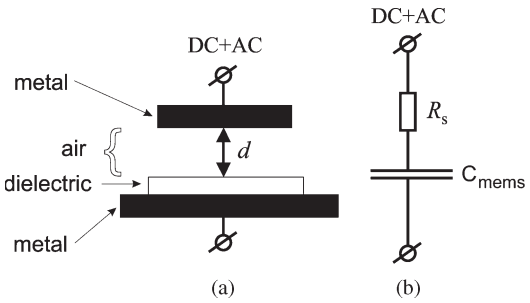

Fig. 8. (a) Schematic cross section of a planar RF-MEMS electrostatic switched capacitor. The dielectric layer prevents a short circuit if the top electrode moves downward. The distance d between the top electrode and the dielectric determines the value of the capacitance and is controlled by the electric field. (b) Loss model is based on physical operation principles. The interconnect and resistive electrode is loss are given by $R_{\rm s}$ and the capacitance of the planar RF-MEMS capacitive switched capacitor by $C_{\rm MEMS}$.

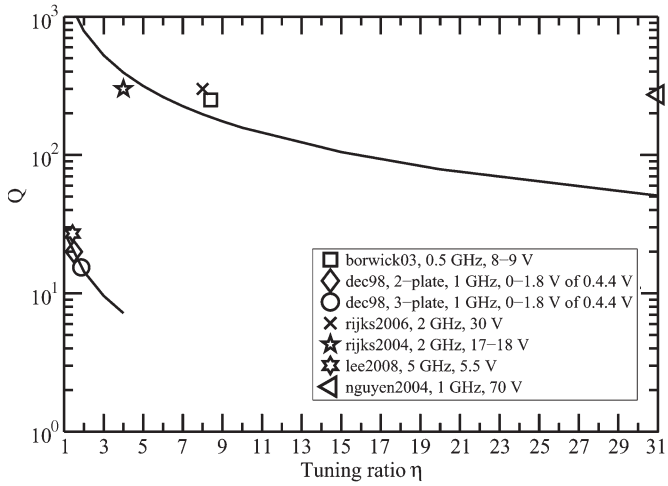

Fig. 9. $Q(\eta)$ curves obtained from eq. (7) and a literature survey on the $Q(\eta)$-performance of planar RF-MEMS electrostatic capacitive switches between 0.5 and 5 GHz [37], [39], [41]–[44]. The actuation voltage and operating frequency differ in some cases from 2 GHz since not all measurements in the literature are performed at this frequency. Measured data points of RF-MEMS devices using the gap tuning principle are shown, except for "nguyen2004" [37]. Two trend lines are indicated for lower and higher actuation voltages. The Q decreases with increasing η.

for integration on the wafer level due to a lack of bearings, but it can be integrated vertically [37]. Yoon and Nguyen [38] designed an RF-MEMS that can move a dielectric horizontally between two parallel plates. The measurements resulted in a Q of 218 at 1 GHz, with a tuning range of 40% $(\eta \approx 2)$. This is not higher than the line that we report in Fig. 9. Therefore, the reasoning that "practical" devices that are useful for applications will have a trade-off upholds. There will be no trade-off—as already stated—if the actuator can be as large as pleased. The "movable dielectric" devices are limited in tuning range due to the air gap. There is no fundamental difference in gap tuning, area tuning, and moveable dielectric tuning since the dielectric layer (air or vacuum) is basically lossless and the electrode and anchor losses dominate the performance of unpackaged planar RF-MEMS capacitively switched devices. In principle, the planar RF-MEMS capacitively switched capacitor has no trade-off between quality factor and tuning ratio. However, it has practical limitations. The equivalent circuit is shown in Fig. 8. The dielectric losses for common insulators in planar RF-MEMS electrostatic capacitive switches, such as SiO_2 and Si_3N_4, are negligible ($\tan\delta < 0.003$ is certainly feasible). The main losses therefore come from the resistive electrodes, whereas in the technologies discussed above, the inherent losses add to or, often, dominate over the electrode losses. The trade-off between a practical actuator and the capacitor design induces a trade-off between Q and η. One of the typical bottlenecks are the electrode connections to the movable electrode (anchors). They need to be well conductive but at the same time they must be flexible to allow movements. Lee *et al.* [39] circumvented this by using an electrically floating top plate and two separate planar bottom plates. Two capacitors are measured in series from the floating top plate to the bottom plates. The signal pad goes via the substrate without passing through the mechanical springs. The capacitance varies between 300 and 430 fF, with $Q \approx 70$ at 2 GHz and $\eta = 1.7$ at 5 GHz. Smaller planar RF-MEMS capacitive switches need narrower or thinner connections when the tuning ratio and the actuation are kept constant. However, they should also have a lower capacitance so that the quality factor is not strongly dependent on the size of the planar capacitive RF-MEMS switch, but rather on the gap that needs to be closed. A larger gap yields a higher anchor resistance at a given actuation voltage. A large gap is equivalent to a large tuning ratio. The electrode surface roughness additionally affects the maximum capacitance when closed $(C_{\max})$ and should be low [40] to yield a high tuning ratio.

Parasitic effects, such as coupling to the substrate, are, of course, also important and are normally strongly reduced by isolating substrates. For a best estimate, those effects are neglected here. Then $R_{\rm s}$ and $C_{\rm MEMS,max}$ are the crucial parameters and the quality factor is expressed by

$$Q^{-1} = \omega R_{\rm s} C_{\rm MEMS,max} = \omega R_{\rm s} C_{\rm MEMS,min} \eta \qquad (7)$$

with the resistance $R_{\rm s}$ of the electrodes. The measurement data from the literature [37], [39], [41]–[44] differ in some cases from 2 GHz, but are in the range of 0.5–5 GHz. A Q of 300 has been measured at 2 GHz, with a tuning ratio of 8 at a maximum actuation voltage of 17 V and a nominal capacitance of 0.47 pF [44], yielding $R_{\rm s}C_{\min} = 33$ fs. The data from the literature in combination with eq. (7) result in a benchmark for planar RF-MEMS capacitive electrostatic switches. The RF-MEMS electrostatic capacitive switch shows a high Q across the tuning range at 2 GHz. The trade-off between the Q and η for these devices are visualized in Fig. 9 for gap-tuned RF-MEMS devices since these devices uphold the highest performance.

The performance close to $Q = 20$ shows that the Q decreases with η. Planar RF-MEMS capacitive switches with a higher $Q(\eta)$ performance close to $Q = 300$ also show the same decrease. For both groups of data points, a trend line has been drawn. Galvanic RF-MEMS make or break an ohmic contact as a relay. Their equivalent circuit is comparable to the simplified model for semiconducting switches in Fig. 5. An ideal fixed capacitor is connected to the galvanic MEMS

switch. The ON-resistance is a sum of the resistance of the anchors and the resistance of the contact. A capacitive RF-MEMS with the same size of a galvanic RF-MEMS can therefore have a lower series resistance. However, on the other side there is the advantage of a lower OFF-capacitance because of the small contact area. The size of the galvanic MEMS is mainly determined by the size of the actuator. A large actuator can induce a high contact force and hence ensure a low ON-resistance. A trade-off between the size of the switch and ON-resistance is therefore expected. This is reflected in Fig. 9. A lower actuation voltage or a smaller size leads to a higher loss.

The present state of RF-MEMS switch reliability for upcoming military and commercial applications is presented in [45]. One of the best reliable galvanic MEMS switches [46], which is still fairly large, achieves a figure of merit of $R_{\rm ON}C_{\rm OFF} \approx$ 30 fs. This is in the same order of magnitude as planar capacitive RF-MEMS and clearly demonstrates the performance potential of planar RF-MEMS capacitive switches. The off-capacitance was calculated from the $S_{21} = 35$ dB at 1 GHz isolation parameter, and the ON-resistance $R_{\rm ON} = 0.5\ \Omega$ includes the connections. Similar ON-resistances have been achieved by other galvanic MEMS technologies [36], [47].

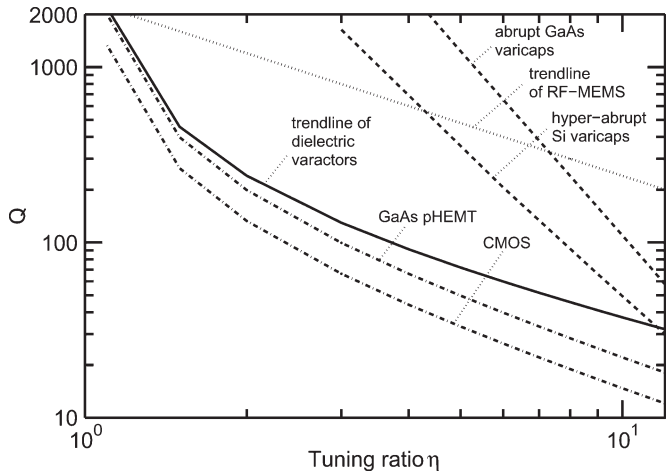

Fig. 10. State-of-the-art intrinsic quality factor Q at 2 GHz without interconnects versus the tuning ratio $\eta = C_{\max}/C_{\min}$ limited to $\eta = 12$. All data are given at 2 GHz unless stated otherwise. The best data found in the literature for GaAs pHEMT (0.5 μm) [31] and CMOS (0.18 μm SOI) switches [30] is shown with dash-dotted lines. The solid line is a fit to the best reported measurements of ferroelectric varactors (BST) at 1 MHz. The trend line also overlaps the data points of nonferroelectric BZN at 100 kHz and 10 GHz. The dashed lines 0 represent the $Q(\eta)$ response of ideal abrupt GaAs varicaps with $N = 10^{15}$–$3 \cdot 10^{17}$ cm^{-3} at $V_{\rm rev,max} = 497$–7 V and the best estimate of a hyperabrupt Si varicaps with $N \sim 10^{18}$ cm^{-3} at $V_{\rm rev,max} = 5$ V [3]. The dotted line is the trend line for higher actuation voltages for planar RF-MEMS electrostatic capacitive switches, assuming that the loss and tuning are proportional to the maximum capacitance [44].

III. Discussion

The state-of-the-art performance in terms of $Q(\eta)$ of each tunable and switchable technology is combined and depicted in Fig. 10. For varactor diodes, the limiting simulations are given. The smallest (continuously) tunable devices are thin-film plate capacitors with tunable dielectrics, e.g., ferroelectrics, exploiting their high dielectric constant.

A transitor–capacitor switchable array is preferred in the high tuning regime and is best realized by pHEMT and CMOS for practical reasons. RF MEMS have a higher tuning ratio, but are less mature and not widely available. The values of CMOS and pHEMT switches are somewhat worse compared to varicaps due to the parasitic capacitances at the channel. RF-MEMS capacitive switches offer the lowest loss, with a high tuning ratio as well as digital operation. A large physical size and a relatively small capacitance value, due to hermetic packaging constraints, results in a limited capacitance density.

The differences in the quality factor Q at tuning ratios below 3 become less important if the capacitors are combined with a coil. A coil typically has a Q-factor below 100 at 1–2 GHz, particularly when integrated or miniaturized. The choice then depends more on other features such as size, cost, and availability.

The described trade-offs can be approximated by:

$$Q^{-1} = (\omega\tau)^{\beta}(\eta^{n+1} - 1)/(n+1) \tag{8}$$

In most cases, β is equal to 1, except for some extrinsic dielectric losses that scale with $\beta < 1$. The exponent n is a measure on how fast the quality factor drops with increasing tuning ratio η. It can be influenced by the device design, but is normally larger than 1. The figure of merit τ is in the range between 10 and 1000 fs. Typically, a higher figure of merit can be reached when the exponent n is increased. However, the gain at low tuning ratios is lost at high tuning ratios.

It is worthwhile to note that a series combination of a lossless fixed capacitor and a lossy tunable capacitor with a large tuning ratio is approximated by $n = 1$ in eq. (8). Circuit designs with external low-loss capacitors, therefore, will not improve the $Q(\eta)$ trade-off significantly. When a high linearity and higher power handling are required, many tuning devices can be connected in series [48], [49], which is only attractive for small devices. Additionally, the series connection increases the breakdown voltage, but the trade-off $Q(\eta)$ remains the same. For example, increasing the dielectric thickness of a ferroelectric MIM varactor will increase the breakdown voltage, but will not change the $Q(\eta)$ trade-off that is fixed by the material properties of the dielectric film. Switches can also be connected in series for higher breakdown voltage, but normally at the cost of additional parasitics. Power handling from, e.g., a 3 V battery can be increased with voltage converters (see, e.g., [50]). However, a low operation voltage will lower the cost and size and will make the device more attractive for certain applications. It should be stated that the above discussion outlines the general trend for the intrinsic performance. Packaging and interconnects can degrade the performance severely and must be optimized for each of the technologies within the given cost constraints. Switched capacitors have advantages when linearity is a priority, whereas continuously tuned devices are typically smaller than arrays of switches.

IV. Conclusion and Outlook

The trade-off between losses and tuning ratios of tunable capacitors at microwave frequencies has been assessed in

terms of basic physics-based models. All technologies show an increased loss for a higher tuning capability and can be approximated by the following equation: $Q^{-1} \sim (\eta^{n+1} - 1)$, with $n = -0.3$–2. Planar microelectromechanical capacitive switches have the highest performance tuning potential with a high Q, but are large. For continuous moderate tuning ranges $\eta < 3$, highly doped GaAs varactor diodes could offer the best performance. Ferroelectric capacitors are an alternative if small physical size and low cost processing are mandatory. In addition to showing the limitations of some tunable technologies, new upcoming technologies are becoming more mature like tunable electroacoustic resonators (e.g., surface acoustic wave and bulk acoustic wave resonators). Tunable acoustic resonators can have high Q factors in the microwave frequency range, however, a large tuning ratio still remains a challenge.

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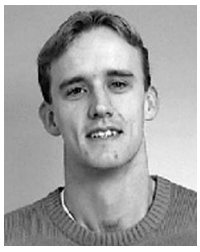

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