

# An Energy and Performance Exploration of Network-on-Chip Architectures

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**Abstract**—In this paper, we explore the designs of a circuit-switched router, a wormhole router, a quality-of-service (QoS) supporting virtual channel router and a speculative virtual channel router and accurately evaluate the energy-performance tradeoffs they offer. Power results from the designs placed and routed in a 90-nm CMOS process show that all the architectures dissipate significant idle state power. The additional energy required to route a packet through the router is then shown to be dominated by the data path. This leads to the key result that, if this trend continues, the use of more elaborate control can be justified and will not be immediately limited by the energy budget. A performance analysis also shows that dynamic resource allocation leads to the lowest network latencies, while static allocation may be used to meet QoS goals. Combining the power and performance figures then allows an energy-latency product to be calculated to judge the efficiency of each of the networks. The speculative virtual channel router was shown to have a very similar efficiency to the wormhole router, while providing a better performance, supporting its use for general purpose designs. Finally, area metrics are also presented to allow a comparison of implementation costs.

**Index Terms**—Circuit-switching networks, evaluation, low-power design, measurement, network-on-chip (NoC), packet-switching networks, performance comparison, simulation.

## I. INTRODUCTION

IN THE forthcoming era of many-core computing networks-on-chips (NoCs) represent the only solution that can provide scalable global on-chip communications [1]. Their regular layout not only deals with the problem of complex wire layout but also allows a natural handling of the communication parallelism inherent in many-core systems. Furthermore, NoCs are a key enabling technology for the provision of many additional services ranging from different quality-of-service (QoS) levels to fault-tolerance. Apart from global communications, the other major challenge facing designers now is

high power dissipation. Power dissipation issues have grown to such importance that they now directly constrain attainable performance. Additionally, technology trends suggest that with further technology scaling communication power will demand an increasing proportion of the already limited system power budgets. For NoCs, it is now therefore important to understand any performance benefits they can deliver in the context of the power costs they demand.

Previous studies into the power consumption of NoCs has focused on the use of high-level power models. Although these can offer rapid power estimates, they do so at the expense of the accuracy of the results. Following on from the work presented by Banerjee *et al.* in [2], the contribution of this study is a more detailed and accurate power analysis of a range of NoC architectures. These results are then extended by measuring the performance properties of the networks. The comparison of the power demands versus the performance returns of the different NoC designs explored then has strong implications for the class of NoC architectures that should be used.

As outlined in Sections III and IV, four different networks, spanning a large range of router architectural families—a Circuit-Switched router, a Wormhole router, a QoS supporting virtual channel (VC) router and a speculative, single cycle virtual channel router—were selected for this study. Complete Hardware Description Language (HDL) models of these networks were then synthesized, placed and routed using a standard application-specific integrated circuit (ASIC) tool flow, with a 90-nm, high-performance CMOS process. Thereafter, extracted parasitics allowed accurate power and energy figures to be obtained for a variety of experiments, outlined in Section VI-A. Section VI-B then characterizes the performance of the networks under a range of synthetic traffic patterns, which are combined with the measured power results to express an energy-delay product metric for the designs in Section VI-C. Finally, the area measurements reported in Section VI-D allow the implementation costs to be judged.

## II. RELATED WORK

Power consumption has become a major design constraint for processing architectures. A good summary of the field and its problems has been provided by Mudge [3]. A brief overview of existing work specific to NoC power characterization is provided here.

Peh *et al.* have developed insightful high-level power models for a set of NoC router components and used these to estimate the power consumption of various wormhole and virtual channel NoC architectures [4], [5]. Although such high-level models may provide valuable power estimates early in the design cycle,

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the limited accuracy of the high-level results and the number of components currently modelled restrict the usefulness of these data.

A similar power measurement methodology is provided by Xi and Zhong [6]. High-level power models were again derived and then embedded into a transaction level modelling (TLM)-based simulation framework. The authors extended the work by examining the impact of technology scaling using the Berkeley Predictive Technology Models. This allowed key predictions to be made for future technologies, but the questionable accuracy of the high-level models still remains a problem.

Banerjee *et al.* attempted to increase the accuracy of power results by first extracting a SPICE level netlist from a synthesized design [7]. This was then used to develop power models for NoC router components which then provided power results under random traffic simulations. However, only a limited range of architectures were used limiting the results that could be obtained.

Mullins built on the accuracy front by fully synthesizing and performing place and route on a specific router design before utilizing the extracted parasitics to analyze power consumption [8]. This paper provided power figures at a high level of accuracy and was thus clearly able to demonstrate the importance of low-level ideas such as clock gating. The current limitation of this work is the single architecture utilized. A comparative study is clearly needed to be able to judge the quality of the design.

Dielissen *et al.* [9] presented a power comparison of the  $\text{\AA}$ ethereal NoC and a bus-based system. For the NoC, various measurements are performed to determine the effect of traffic types, packet lengths, path, and packet interaction. The power is measured for a 0.13- $\mu\text{m}$  CMOS technology, nominal process operating at  $V_{\text{dd}} = 1.2$  V, 25 °C and a data path of 32-bits. At a worst-case estimation for random payload (activity of 0.5) with guaranteed throughput (GT) traffic, the router consumes 68.25 pJ per flit of which 32 pJ is consumed by the clock tree. For best effort (BE) traffic an extra 15.7 pJ/flit is required.

Lee [10] reported a detailed power analysis of a high-performance system-on-chip (SoC) using an NoC for communication between heterogeneous intellectual property blocks such as RISC, SRAM, and field-programmable gate array (FPGA) units. The 25 mm<sup>2</sup> chip, realized in 0.18- $\mu\text{m}$  CMOS technology, consumes 160 mW of which 51 mW is consumed by the NoC. For a 5-port switch with a 32-bit data path the reported packet energy is 229 pJ per packet of which 86% is consumed by the queues. Each packet transports a payload of 64 bits.

### III. SELECTION OF NoC TEST CASES

Any characterization study such as this would ideally evaluate the impact of all input parameters on any output results. However, to enable a tractable study it is necessary to select a single, representative value for many parameters. All the parameter values used in the rest of the paper were therefore selected using this logic.

The large variety of network architectures currently in existence however, clearly implies that the network architecture cannot be represented by a single value. The challenge here was to select a small number of test cases that still represented a

large family of network architectures. The four networks listed as follows were finally selected to represent a spectrum of designs, from those that use fully static scheduling to those that exploit fully dynamic scheduling.

- 1) The circuit-switched network (from now on referred to as the CS network) presented by Wolkotte *et al.* [11] which primarily aims at satisfying QoS needs. It has a simple, statically scheduled data-path and no inherent control. This design represents the set of networks that place a high importance on meeting QoS demands and advocate simplicity and static allocation of resources against highly dynamic techniques.
- 2) A wormhole flow control- and switching-based router (referred to from now on as the WH network) which performs dynamic allocation, but not at the cost of highly complex allocation methods.
- 3) The virtual channel flow control-based router architecture presented by Kavaldjiev [12] (referred to from now on as the GuarVC network), to allow a comparison to a design using increasing amounts of control. The router is designed to offer QoS for streaming applications, while also using source routing and semi-dynamic allocation of resources, thus allowing the impact of both of these techniques to be evaluated.
- 4) The speculative, single cycle, virtual channel design presented by Mullins *et al.* [13] (referred to from now on as the SpecVC network). Each router in this design contains a large amount of allocation logic, which attempts to provide good resource sharing, while minimizing latencies.

## IV. ROUTER DESIGNS

This section provides a brief overview of the network architectures used. For all power measurements, the networks were based on a  $4 \times 4$  mesh topology with 5-input  $\times$  5-output port routers, with 4 ports connecting to the neighboring routers and the fifth one connecting to a local computation tile. All flits provided a 64-bit data payload size, with additional control bits necessary for the WH, GuarVC, and SpecVC designs. The dynamic networks also utilized a static, dimension-ordered,  $XY$  routing scheme.

### A. Circuit Switched Router

The CS router provides a simple data-path, being composed only of a crossbar with registered outputs. Each output port is 64-bits wide, since no control data is necessary. To provide more flexibility, each 64-bit output port is split into four, 16-bit wide, lanes. Given the 5-port design, 20 input and output lanes therefore exist. A  $16 \times 20$  crossbar provides full connectivity between every input and output lane except that no U-turns are allowed. The crossbar allocation is a configurable memory of 20 entries (1 for each output lane), with 5-bits per entry (4 address bits to identify an input lane and 1 valid bit).

The splitting of a 64-bit flit into 16-bit units for transport over the network also means that a serializing and deserializing unit is necessary at the tile interface of the router. The completely static nature of the CS network means that a separate control network is necessary to provide all circuit set-up and tear-down

functions. To model a scalable solution for this, a simple wormhole routed network was provided. All experiments then considered both the circuit-switched and packet-switched routers, to account for the necessary overhead of the packet-switched network. Fig. 1(a) shows the complete structure of the CS router. Further details of this design have been reported by Wolkotte *et al.* [11].

**B. Wormhole Router**

The WH router uses a conventional input-queued architecture with 4-flit-deep buffers at each input. A two-stage pipeline is provided. The use of look-ahead routing allows switch allocation to occur in the first stage with crossbar and link traversal in the second.

Control information is appended to each flit rather than being carried in an additional header flit. The 64-bit data-path therefore combines with a one-hot encoded, 5-bit next-port identifier for look-ahead routing, two bits each for destination  $X$  and  $Y$  addresses and one bit to identify tail flits, to result in a total flit size of 74 bits.

A pipeline register is provided between the input first-in-puts–first-outputs (FIFOs) and the crossbar. For the crossbar traversal stage the flit at the head of the FIFO is loaded into this register, which drives it across the rest of the data path.

A stop-go flow control is also used for buffer management, where a *buffer nearly full* signal is output by each input FIFO to the corresponding upstream router to indicate that flit transmission should be stopped. Fig. 1(b) shows the structure of this router.

**C. QoS Providing Virtual Channel Router**

The GuarVC router implements wormhole routing with virtual channel flow control. A conventional input-queued architecture with 4 VCs per port and 4-flit-deep buffers for each VC were used.

Each flit identifies its VC by using a 2-bit VC identifier. The use of separate head, body, and tail flits means that the flit type is encoded by an additional 2 bits. Combining with the 64-bit data-path results in a total flit size of 68 bits.

Source routing is used to determine the packet’s entire route at the originating node, which is then carried by one or more header flits. Per hop of the route, 6 bits are required, 2 bits for the next port, 2 bits for the VC, and a 2-bit identifier for VC allocation. For a 64-bit data path, routing information for 10 hops are merged into a single header flit.

Input VC queues do not share a single crossbar port per input port and hence the crossbar is asymmetric and has 20 inputs, i.e., it has one input for every input VC queue. This creates a single point of arbitration that is used to enable QoS. To provide for guaranteed throughput traffic, a central controller allocates network VCs to at most a single QoS requiring data stream. The round-robin arbiters used at each output port then give a predictable arbitration result, where each data stream is guaranteed a certain proportion of the network throughput, i.e., throughput based QoS demands can be met.

Best effort flows are dealt with by assigning the same VC to multiple data streams. Conflict-free VC allocation is guaranteed

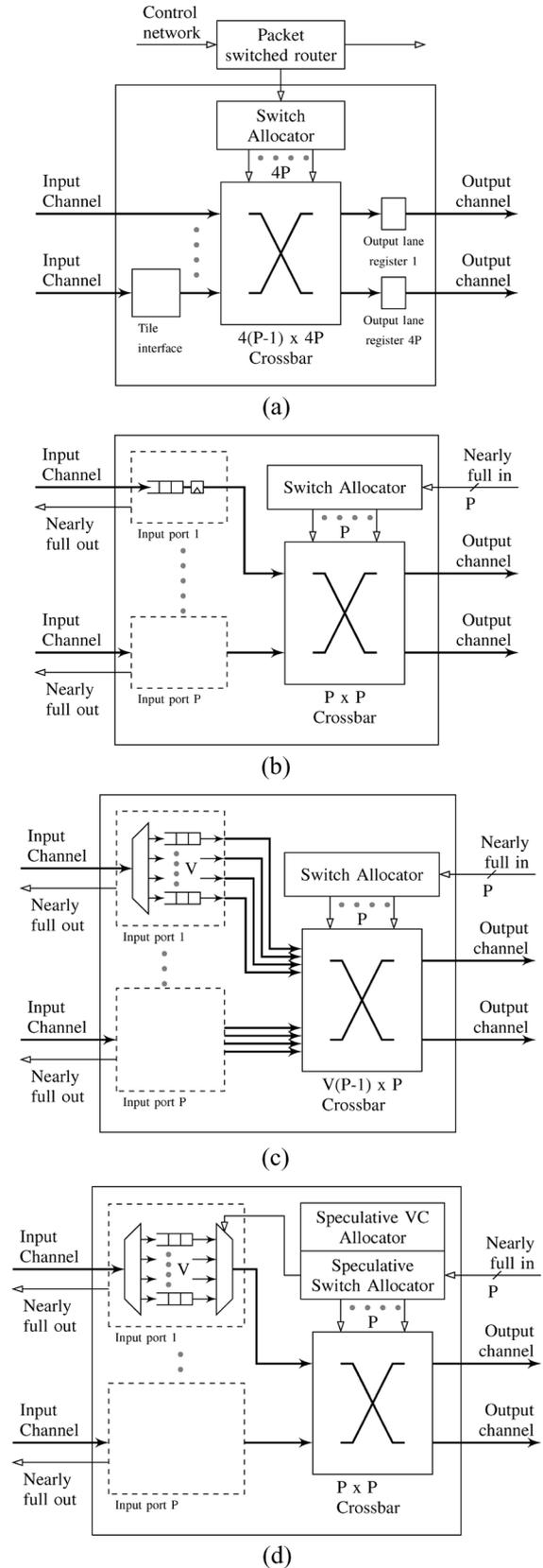


Fig. 1. Router architectures studied. (a) CS router. (b) WH router. (c) GuarVC router. (d) SpecVC router.

by the 2-bit identifier in the header flit, but it does not guarantee a particular bandwidth or latency.

A stop-go flow control method is utilized to prevent buffer overflow. Fig. 1(c) shows the structure of this router, with further details having been provided by Kavalajiev *et al.* [12].

#### D. Speculative Virtual Channel Router

The SpecVC router provides for single cycle flit forwarding by utilizing look-ahead routing and speculative VC and crossbar allocation. A conventional input-queued architecture with 4 VCs per port and 4-flit-deep cyclic buffers for each VC was used.

Each flit identifies its VC by using a one hot encoded 4-bit VC identifier. A 5-bit next-port identifier, 4-bits each for destination  $X$  and  $Y$  address and a bit to identify tail flits combines with the 64-bit data path to result in a total flit size of 82 bits.

Both the VC and switch allocators (based on matrix arbiters) can allocate VCs and crossbar ports speculatively for the next clock cycle if necessary. Since both crossbar and link traversal are performed in a single clock cycle, in the best case, an incoming flit finds preallocated resources and can thus be forwarded to the next hop in a single clock cycle.

A stop-go flow control method is utilized to prevent buffer overflow. Fig. 1(d) shows the structure of this router, with further details having been provided by Mullins *et al.* [13].

### V. POWER MEASUREMENT FRAMEWORK

The first step in the power measurement methodology was to describe the full network designs in an HDL. A CMOS 90-nm, high-performance process with a core voltage of 1.2 V and nominal threshold voltage was selected and a standard ASIC tool flow utilized to synthesize, place, and route one instance of each of the four routers in this technology. Due to the significant benefits of clock gating, shown by Mullins [8], automatic clock gating was enabled during synthesis so that low-level clock-gating cells were automatically inserted whenever appropriate enabling conditions were detected. Parasitic extraction was then performed and the results back annotated into the designs to allow accurate power measurements on the routers.

The inter-router link characterization was performed separately from that of the routers. Links of length 1.5 mm, based on intermediate metal layers (M3–M6), were used. Theoretical values could have been derived with the equations as presented by Banerjee [14], but SPICE simulations were chosen to get the same level of accuracy. The Quickcap field-solver [15] tool from Magma was then used to extract link capacitance values with an 8-wire model. The energy/delay tradeoffs of various link repeater configurations were then analyzed with SPICE simulations. Ultimately, instead of using a delay-optimal repeater configuration, a lower energy configuration with 9.7 FO4<sup>1</sup> delay with an associated 0.36 pJ/transition/mm for the links was selected for this study.

The traffic sources were defined entirely in C and the Verilog Programming Language Interface (PLI) was utilized to link the C traffic source with the HDL network descriptions. This provided a highly flexible framework, where each tile could be

<sup>1</sup>One FO4 delay is the delay of a single inverter driving four identical inverters.

modelled by a separate set of C routines, at any desired level of complexity.

All simulations were performed at 200 MHz at the nominal process, voltage, and temperature corner (PVT).

## VI. RESULTS AND DISCUSSION

### A. Power Measurements

1) *Power at Fixed Throughput:* An initial power characterization of the designs was obtained by streaming data through a single router and measuring the dissipated power. Four fixed traffic streams were defined, one originating at each of the North, South, East, and West ports of the router, with each one transmitting a stream of packets to the opposite router port.

256-bit packets, each carrying a random payload, were selected for these experiments. The use of the 50% switching activity factor of a random payload is motivated by observing it in various applications such as the baseband processing of various wireless standards. The data rate of each stream was set to a moderate 30% of the maximum bandwidth of a single router link, with flits being sent at randomized intervals. Power analysis was performed for 5000 clock cycles for each experiment. For simplicity, the CS net was only configured once at the start of the experiments. This clearly represents a best case scenario for this network. The data rate of 30% for the GuarVC equals the net data rate of only the data payload carrying flits of the packet. A single three hop header is added per packet to route it through the router, which results in a gross data rate of 37.5%.

Fig. 2 shows the total, router, and link power results of these experiments for all of the routers. The leakage power is indicated by the shaded areas of the individual bars. An important result to note is that the router power is more than the link power for all the designs and is significantly so for the SpecVC design. The link power results are otherwise as expected with the more highly loaded GuarVC links, caused by the extra header flit per packet, dissipating the most power and the narrowest width CS flits dissipating the least. From these results, it is clear that the benefits provided by complex NoCs come at a high energy cost, at least at the 90-nm technology node.

The router powers are comparable to several contemporary computation tiles. For example, a speed optimized ARM926EJ-S processor with caches at 200 MHz requires 47 mW and an area of 1.40 mm<sup>2</sup> [16]. In the absence of other scalable solutions to allow global communications, this new era of much higher communication power compared to computation power then importantly points to a reversal in computation to communication usage—whereas in the past, increased communication could be justifiably used to reduce computation, it might now be much more desirable to increase the amount of computation to minimize communication.

All the routers dissipated a significant amount of power even in the 0-stream (i.e., no traffic) condition (from now on referred to as standby power) with a breakdown reported in Table I. Given the lack of any leakage minimization techniques, one component of this is leakage power. As we move to future technologies, leakage can be expected to contribute an even larger amount to this. Second, there is also some clock related dynamic power. This is caused purely by the activity in the clock tree

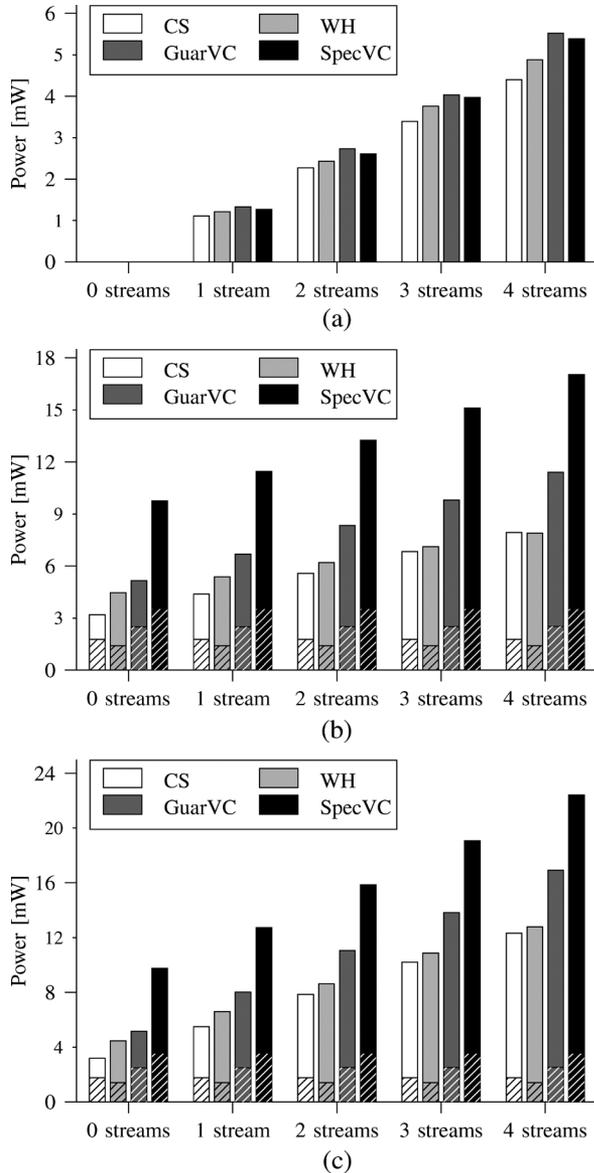


Fig. 2. Link and router power at fixed throughput. (a) Link power. (b) Router power. (c) Total power.

(since it is only gated at a low-level) and on the clock pins of any non-clock gated synchronous elements.

Analysis shows that the major contributors to standby power originate along the data path rather than the control path. For instance, in the all packet switched routers, not only do the input FIFOs consume a large amount of power, but a large proportion of the clock tree (another large standby power consumer) goes towards clocking these FIFOs. The impact of this control to data-path power division is discussed in more detail in Section VI-A2.

The large observed standby power means that in any real system, standby power reduction techniques will be key. To reduce leakage power advanced techniques such as power gating or the use of high- $k$  dielectrics could clearly be applied. Techniques to reduce the dynamic component of the standby power have also been demonstrated, such as the gating of the entire

TABLE I  
STANDBY POWER BREAKDOWN

Component	Standby Power [mW]			Dynamic	Static
	CS	WH	GuarVC		
Top level clock tree	0.64   0.02	1.65   0.04	1.52   0.03	3.61	0.11
Flit buffers + logic	0   0.10	1.27   0.93	1.05   1.86	1.04	2.30
Crossbar	0   1.00	0.09   0.28	0.03   0.36	0	0.01
Crossbar allocator	0.11   0.06	0.05   0.09	0.01   0.21	0.67	0.18
VC allocator	—	—	—	1.05	0.23
Output ports	—	—	—	0.20	0.20
BE router	0.22   0.15	—	—	—	—
Tile interface	0.44   0.33	—	—	—	—
Other	0   0.10	0   0.06	0.06   0.04	0.02	0.12
Total	1.41   1.77	3.06   1.41	2.67   2.50	6.60	3.15

clock-tree demonstrated by Mullins [8]. However, it is important to realize that when packets are being routed, such standby power reduction techniques cannot be applied entirely. For example, the buffers cannot be completely power gated off while flits are actively stored in them. When packets are being routed, they will require additional power, but this will be on top of the fixed standby power. The large value of this standby power relative to the active power can therefore have serious implications for the feasibility of deploying NoCs. It is therefore important to strive towards architectures with inherently low standby power needs.

2) *Packet Energy Under no Congestion*: A more fundamental metric than the power at a given throughput is the energy required to perform a certain amount of communication in each of the four NoCs. As discussed, the activity of routing a packet means that the router dissipates some fixed standby power as well as some additional energy specific to the computation performed for each packet. Considering the standby power to be the overhead power of a particular architecture means that the *increase* in energy demands represents the *dynamic energy cost* of the particular computation performed for each packet. Measuring the increase in router power under the four-stream traffic condition, multiplying by the simulation time and dividing by the number of packets processed then allowed this dynamic energy cost per packet to be calculated. This methodology will only work given effective low-level clock gating and the results obtained showed this to be generally true. With this methodology, some inter-packet dependencies will inevitably exist (for example, if two packets affect the same clock gating enable signal for any register), but these are reduced in Section VI-A3 by utilizing more random traffic.

Fig. 3 shows the dynamic energy cost required to route a 256-bit, random payload packet through each of the four routers, with a breakdown across the major components reported in Table II. The anomalous clock-gating of the WH router input ports meant that the 45.72 pJ value calculated with the previous methodology is not directly representative of the buffer computational energy and it was manually determined to be 66.0 pJ (which is then consistent with the other router buffer energy results). In these experiments, the GuarVC handles solely BE traffic packets which required a three hop header

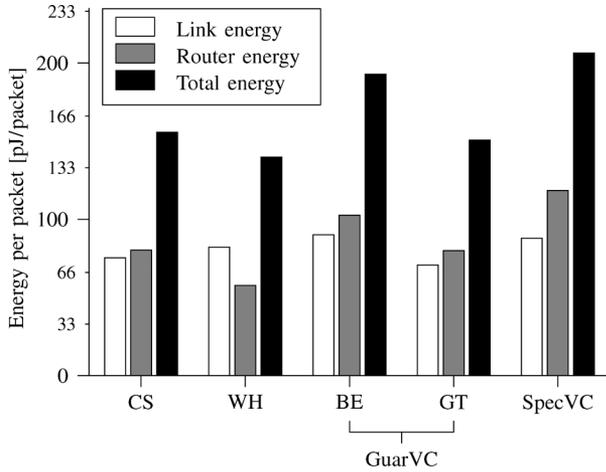


Fig. 3. Packet energy for streaming traffic.

TABLE II  
STREAMING TRAFFIC PACKET ENERGY BREAKDOWN

Component	Packet energy		value [pJ]   relative share [%]	
	CS	WH	GuarVC	SpecVC
Top level clock tree	0	0	0.01   0.0	5.98   5.1
Flit buffers + logic	28.1   47.7	45.72   79.4	64.10   62.5	58.2   49.2
Crossbar	37.9   35.4	6.62   11.5	31.69   30.9	15.5   13.1
Crossbar allocator	4.65   5.9	2.94   5.1	2.84   2.8	7.27   6.1
VC allocator	—	—	—	1.92   1.6
Output ports	—	—	—	8.99   7.6
BE router	0	—	—	—
Tile interface	0	—	—	—
Other	8.77   11.0	2.33   4.0	3.98   3.9	20.5   17.3
Total	79.4   100	57.61   100	102.61   100	118.4   100

flit per packet. The energy per packet reduces by 22 pJ for the router and 20 pJ for the link if the router handles solely GT traffic, which does not require a unique header per packet, as depicted by the right group of GuarVC bars in Fig. 3.

The key result to note here is that the total energy of the different designs are not vastly different, with the data-path components dominating over the control elements in all designs, especially in the CS and WH nets. Specifically, the flit buffers consume a large proportion of the total energy. Moreover, it is interesting to see that the buffer energy is not directly proportional to the amount of buffering in the designs. This is because, with effective clock-gating, the energy needs are only proportional to the computation activity. In the case of the buffers, energy is only required when data is written into or read out of a buffer position. The remainder of the time, clock-gating ensures that very little energy is dissipated. The same explanation also holds true for the rest of the router's computation activity.

Besides using the dynamic energy cost to compare architectures with the same functionality, it can also be used to compare functionalities across different network types. For example, in the particular case of the buffers, the WH router buffers flits twice, taking 66.0 pJ, which is consistent with the single buffering operation performed by the CS router taking 28.1 pJ. As the SpecVC router also buffers flits just once, the extra

energy for the SpecVC buffers therefore comes from the wider buffers and the more complex data-path around the buffers providing added functionality (as each flit needs to fan out to each register of each VC, unlike the other non-VC designs). The GuarVC router also buffers flits just once and has a smaller buffer width, but extra energy is consumed by the extra header flit per packet and added functionality around the buffers similar to the SpecVC design. Similarly, the reason for the high CS energy can clearly be seen to be the higher order crossbar used for that design. The CS crossbar takes significantly more energy than even the more complex input port multiplexer and crossbar structure used by the SpecVC design.

The leakage power variation was seen to be insignificant across all the streaming traffic conditions, i.e., the leakage power is practically independent of routing activity. This means that an equivalent *leakage energy cost* for a packet does not exist. Even if some leakage reduction techniques were used, it would still be more meaningful to consider them as standby power reduction techniques and the leakage power as part of the fixed standby power. However, as already discussed, Table I shows the leakage power to also be dominated by the data-path components.

Importantly, from an energy perspective, the much higher data-path power compared to control-path power justifies the use of complex, dynamic allocation techniques for NoCs. As long as the data path can be kept simple, NoC routers with complex allocation techniques can feasibly be deployed without significantly straining the power budget. What little increase in the power that comes from the more complex control can be tolerated, given the better performance and utilization of communication resources they provide. These arguments would be further backed up when considered in the context of reducing transistor cost, given continued scaling. However, given the non-power optimized designs considered here, it is difficult to accurately judge how the data-path to control-path energy ratios might change. On one hand, several data-path optimizations such as the use of SRAMs as FIFOs can clearly reduce the data-path energy. Conversely the control-path energy might be increased by varying parameters not considered in this study. On the other hand, it is questionable whether roughly the order of magnitude data-path to control-path energy difference observed in this work can be eliminated, especially in the context of even wider data-path widths expected for future technologies. Finally, a very simple (and hence low power) data-path might also not be feasible from other perspectives. For instance, with the GuarVC router, QoS specifications demand a higher order crossbar which dissipates extra energy.

The data reported so far can also be used to estimate the impact of changing some of the design parameters. For example, the impact of using a higher-order topology can be seen to have a large impact on a single router's power needs, as shown by the increasing power needs of the higher order crossbars in the designs presented here. However, the authors primarily foresee that the data presented here could be used to better calibrate existing analytical tools, such as Orion, which can themselves be used to predict the effect of parameter changes. For example, Wang *et al.* [17] demonstrated the use of analytical models of routers and links to explore the topology of the NoC.

3) *Packet Energy Under Congestion*: The packet dynamic energy cost reported in Section VI-A2 does not account for any network congestion. Clearly it is of interest to see how this parameter will affect packet energies. For the WH, GuarVC, and SpecVC routers, this was achieved by instantiating  $4 \times 4$  mesh networks for each design. A traffic source connected to each router then injected random traffic at varying injection rates into the network, destined for random destinations (excluding itself). The inter packet interval is determined by a Bernoulli distribution. Packets, with each carrying a 256-bit (i.e., four flits) random data payload, were again used. An initial 500 clock cycles were used as a *warm-up* time, with the next 5000 clock cycles forming the *sampling time*, any packets transmitted during which were the only ones considered in the analysis. A further 300 clock cycles of *drain time* were used to allow any packets transmitted near the end of the sampling time to reach their destinations. A single router, at coordinates  $x = 2, y = 2$  was considered and the energy of any packets going through it was calculated in the same fashion as in Section VI-A2.

For the CS net, the current lack of dynamic circuit set-up and tear-down support means that this form of congestion energy experiment cannot yet be performed.

Fig. 4 shows the packet energies for various injection rates. For all the routers the energy per packet was seen to vary very little as network traffic increased. As already discussed this calculated value represents the energy required to perform the computation specific to the forwarding of one packet through the router. The above result is then intuitively meaningful as effective clock-gating ensures that the amount of data-path computation (the main energy consumer) does not change with congestion. The data-path functions are independent of the amount of time packets spend in network queues. Indeed, a breakdown of packet energies across all data-path components confirmed that their energy demands do not significantly change. The main reason for the SpecVC and GuarVC router energy increase was seen to be due to an increase in allocation and flow control activity, given the increased resource contention. This is a novel result, showing that although performance (such as packet latency) might be seriously degraded at high congestion, there is no considerable direct impact on packet dynamic energy, given effective clock-gating.

The more important energy impact would come from reducing the time available to effect standby power minimization techniques. For instance, some leakage power reduction techniques, e.g., power-gating, cannot be fully applied while active flits are stored in the routers' buffer. This is another reason why standby power represents a key parameter.

The breakdown of the total power into the practically constant quantities of standby power and a dynamic energy cost per packet can now allow simpler functional simulations (to obtain the packet forwarding timestamps at each router) to give a good estimate of total power needs to be made under a wide variety of traffic patterns.

## B. Performance Measurements

The power metrics reported so far only represent one aspect of the designs. To obtain a more complete characterization it is also important to obtain the performance metrics of the designs.

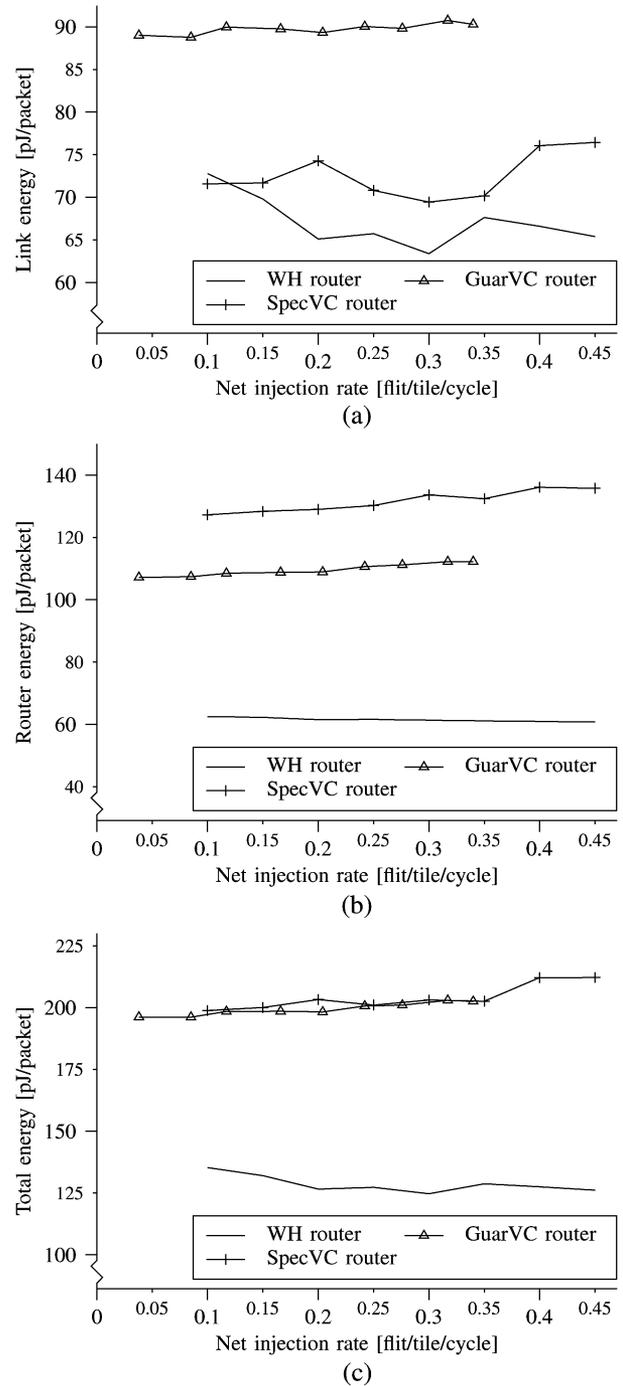


Fig. 4. Packet energy under congestion. (a) Link energy. (b) Router energy. (c) Total energy.

Ideally, such measurements would be obtained using full system level simulations with real applications, but given the absence of these, synthetic traffic generators have currently been used. As with the selection of network test parameters in Section III, the particular performance characterization tests performed attempt to represent a range of expected realistic scenarios.

The first test therefore used uniform random traffic which can be considered to represent any sufficiently complex system. The importance of locality, highlighted by work such as that by Greenfield *et al.* [18], prompted results to be gathered for

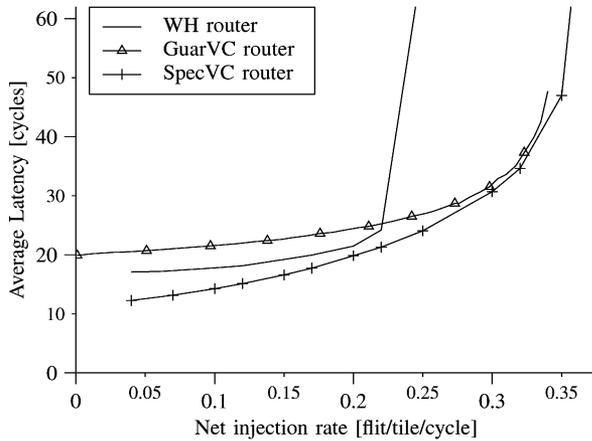


Fig. 5. Packet latency for uniform random traffic.

traffic pattern where the destination of randomly generated communications favored those nodes closer to the source. Finally, the importance of streaming traffic patterns as will likely be observed in radio or scientific applications prompted the use of streaming traffic patterns with QoS demands as well.

All experiments were carried out with an  $8 \times 8$  network, with 4-flit-long packets. An initial 500 packets transmitted per node were used to initialize the network in the *warm-up* period. The subsequent 3000 packets were the ones used during the measurements in the *simulation* period, with an additional *drain* period used at the end to allow all simulation period packets to be received. For the CS net, the current lack of dynamic circuit set-up and tear-down support means that this form of randomized traffic performance measurements is not currently possible.

1) *Uniform Random Traffic*: Fig. 5 shows the measured average packet latency at varying traffic net injection rates<sup>2</sup> into the network under a uniform random traffic pattern. Each source has an equal probability of transmitting to any other source (apart from itself). As expected, the VC networks saturate at a higher injection rate than the WH network and the delay optimized SpecVC network achieves a lower delay than the WH network. The increased delay for the GuarVC router is caused by the relatively simple and static VC allocation scheme used. The VCs for the entire path are allocated at the source, before a packet even enters the network. This is necessary as the GuarVC design is primarily optimized for QoS traffic. However, this causes the packets to be halted in the buffers even if the output port is free. Despite the larger packets (an extra header flit) the saturation points of both GuarVC and SpecVC are almost identical.

2) *Localized Traffic*: It has been shown that localized traffic can form an important part of on chip communication traffic. To model this, a roughly exponentially distributed hop count based traffic generator was used at each node, where 40% of all transmitted packets were sent only one hop away, 25% was sent two hops away, 15% was sent three hops away and the rest uniformly distributed across the rest of the network. Fig. 6 depicts the measured average packet latencies at varying traffic net injection rates into the network for the localized random traffic.

<sup>2</sup>Net injection rates are determined by the injected body and tail flits

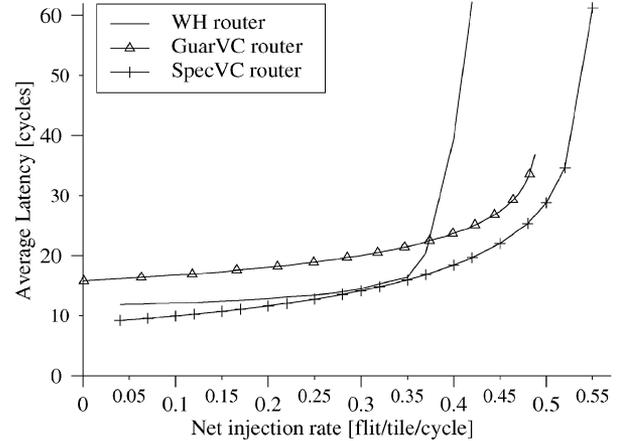


Fig. 6. Packet latency for localized random traffic.

Compared to the uniform random case, all the architectures now show a lower latency and higher saturation point, due to the lower average hop count. Compared to the uniform random distribution the WH and GuarVC router benefit most from localized traffic, as for these architectures the serialization delay dominates over the allocation delay. For the GuarVC design, the static VC allocation has an increased influence on the packet latency.

3) *Streaming Traffic*: The previous two tests assumed randomized traffic scenarios with equal priority for all packets in the network. In radio, multimedia or scientific applications the process graphs consist of a lot of single-in single-out processes that communicate frequently and have QoS demands. Therefore, in this third test, we offered both BE and GT traffic to the GuarVC network. The GT packets from a tile are destined to one specific, other tile in the network. The Manhattan distance between the GT pairs has the same distribution as for the localized traffic scenario, 40% of all pairs are 1 hop apart, 25% two hops, 15% three hops, and the rest of the pairs four or more hops. The assumption here is that the mapping of processes to tiles will be optimized to locality. The BE packets are uniformly distributed as in Section VI-B1. 50% of the tile's injected packets are of type GT and the remaining of type BE.

Since the GuarVC design is the only one supporting QoS needs (it has a clear distinction between BE and GT traffic types), it was the only design tested with such traffic.

Fig. 7 depicts the latency for both BE and GT traffic. For reference, the GuarVC latency of the uniform random test is included. Tests with a different ratio between BE and GT packets resulted in comparable results.

The latency for the GT packets is significantly lower compared to the BE traffic. For the GT packets all resources are pre-allocated in the network, which make the latency the sum of only the serialization delay and hop distance. The GT latency increase is caused by the flit interleaving of multiple packets on the link. At higher net injection rates the BE part of the traffic saturates, but the GT traffic is guaranteed at least 50% of the link's bandwidth and will therefore never saturate. The saturation point of the BE traffic is higher, because fewer of the total injected flits are blocked for relative long periods. For tests with a lower percentage of GT traffic, the saturation point of BE

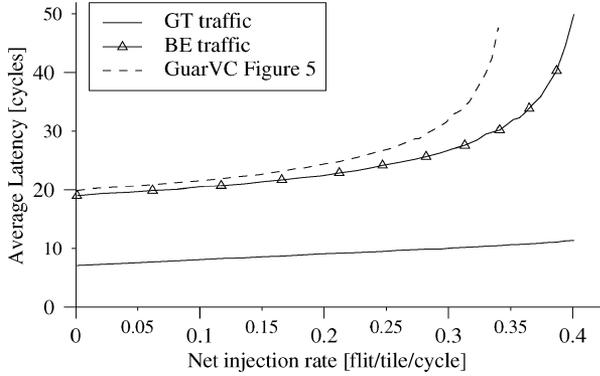


Fig. 7. Packet latency for combined streaming and uniform random traffic.

traffic gradually decreases to the point of the uniform traffic scenario and for a higher percentage it increases.

### C. Energy-Delay Product Measurements

A key property of any design is the energy efficiency it provides. For the networks presented here, their energy efficiency at a single injection rate could be obtained by multiplying the average packet latency from Fig. 5 and the total packet energy from Fig. 4, to present an energy-delay product (EDP). Since, in NoCs literature, the term delay is commonly used to represent only the delay of the head flit, the more accurate term of energy-latency product (ELP) will instead be used. Since a lower value of this figure represents a more energy efficient design, the value of  $(\text{energy} \times \text{latency})^{-1}$  can be used to present a metric which represents increasing values as better designs. Clearly though, different applications will have different latency and throughput requirements. Although the above metric takes into account the latency at each injection rate, it does not account for a network's saturation throughput. In order to do this, it is proposed to sum the individual  $(\text{energy} \times \text{latency})^{-1}$  values between a fixed lower end of the injection rate and the saturation throughput ( $r_{\text{sat}}$ ). In the limit, this simply becomes the integral of the curve, or the area under it. Equation (1) shows how this metric is calculated

$$\text{IELP}_{\text{sum}} = \int_0^{r_{\text{sat}}} \frac{1}{E(r) \cdot L(r)} dr \quad (1)$$

where  $E(r)$  and  $L(r)$  are the packet's energy and latency at the net injection rate  $r$ .

Table III shows this inverse ELP sum ( $\text{IELP}_{\text{sum}}$ ) metric for the three networks and the three applied traffic types described in Section VI-B. The metric excluding the link energy is placed between parentheses. It is important to note that this figure must still be considered in the context of the fixed standby power in the network. Moreover, this metric does not account for any parameters apart from energy and latency. For instance, a metric quantifying QoS demands might score the GuarVC router a lot higher than the other designs. Finally, the energy value used in this metric is only valid for a single hop. The overall  $\text{IELP}_{\text{sum}}$  value for the network can however be obtained by multiplying the reported values here by the average hop count seen by the packets. Since this average hop count is the same for all the

TABLE III  
ELP FOR THE VARIOUS TRAFFIC TYPES

Network	$\text{IELP}_{\text{sum}} [\times 10^7]$ (excl. links)		
	Uniform random	Local random	Streaming
WH	8.9 (19.1)	21.6 (45.5)	—
GuarVC – BE	6.8 (12.4)	12.8 (23.4)	8.5 (15.5)
– GT	—	—	29.7 (55.9)
SpecVC	9.6 (15.0)	19.4 (30.2)	—

networks (given the same traffic pattern and routing strategy), this product is not reported here.

It must be noted that many different traffic patterns can exist in any real system, beyond the three simple patterns used here. However, the presented metric can be used to judge the efficiency of the tested networks under any traffic pattern used.

Looking at the high efficiency of the GuarVC router with GT traffic clearly demonstrates the benefits of specialization. For the non-specialized, general architectures of the WH and SpecVC routers an important question is whether the additional investment in power for the SpecVC design brings at least a proportional increase in the performance. The power-performance ratio provided by the  $\text{IELP}_{\text{sum}}$  figure for the WH and SpecVC routers for the uniform random and local random traffic patterns in Table III can then answer precisely this. The near identical value for both the networks for each traffic pattern implies that the SpecVC design does indeed make a performance return directly proportional to its additional power investment. Clearly, it can be expected that, beyond some point, continued increases in router complexity will not produce proportional performance returns, at which point the efficiency metric will decrease. Similar logic has been extensively applied by Jouppi for microprocessor design to develop the concept of *Microprocessor Efficiency Eras* [19]. In the CMP environment, such observations motivate the use of the most capable microprocessors, which still operate in the highest efficiency region. In the exact same way, the  $\text{IELP}_{\text{sum}}$  metric can motivate the use of the SpecVC like design instead of the WH like design for on-chip communications networks. Clearly, the very small number of synthetic traffic patterns and NoC architectures used in this study do not present enough data points to allow the generalization of this argument to the wider NoCs field, but currently stands as future work.

### D. Area Measurements

The area of each router represents another important parameter and is therefore reported here. The area of the designs was obtained post place and route and is reported in Table IV.

The breakdown of the area for the CS router showed that the higher order crossbar is its largest component, being approximately  $3.5\times$  larger than the WH crossbar. This, along with the serialization logic, the packet switched network and the configuration memory areas of the CS router together outweigh the saving of area from reduced buffering compared to the WH router. The increase in area for the virtual channel routers are caused by the extra input queues for each VC. Furthermore, the GuarVC has a larger asymmetric crossbar and the SpecVC requires more area for its speculative allocation.

TABLE IV  
AREA OF THE DIFFERENT ROUTERS

Component	Area [mm <sup>2</sup> ]   [%]			
	CS	WH	GuarVC	SpecVC
Flit buffers + logic	0.008   7.19	0.045   57.7	0.160   74.7	0.166   67.3
Crossbar	0.058   53.6	0.016   20.1	0.034   16.1	0.015   6.19
Crossbar allocator	0.004   3.34	0.005   6.55	0.018   8.36	0.015   6.24
VC allocator	—	—	—	0.022   8.89
Output ports	—	—	—	0.012   4.66
BE router	0.009   8.76	—	—	—
Tile interface	0.026   24.3	—	—	—
Other	0.003   2.79	0.012   15.7	0.002   0.87	0.016   6.72
Total	0.108   100	0.078   100	0.214   100	0.246   100

## VII. CONCLUSION

This study has presented an accurate power characterization of a range of NoC architectures by considering a static CS network, a WH network, a semi-dynamic virtual channel (GuarVC) network supporting QoS, and a speculative virtual channel (SpecVC) network. All designs were synthesized, placed, and routed in a CMOS 90-nm, high-performance technology. Utilizing the extracted parasitics then allowed accurate power results to be obtained.

A set of streaming traffic conditions was first used to characterize the power dissipation rates of the routers. The router power was seen to be a significant overhead beyond the link power and also appears comparable to contemporary computation units. These results then significantly point to the existence of a new era of computation versus communication costs. In some cases, it may now be prudent to perform more computation to optimize global communications.

All the designs dissipated significant standby power produced mainly by leakage and clock tree power. This standby power can be considered to be the overhead required by a particular architecture and highlights the need to use efficient architectures combined with standby power reduction techniques, to obtain power efficient designs.

The additional power dissipated while routing a packet was used to calculate a dynamic energy cost per packet. The much wider data path compared to the control path meant that it dominated the energy needs, with the buffer energy forming a significant proportion of this figure. This result then importantly shows that the new computation to communication tradeoff extends to within the communications network. They justify the use of complex control in NoC routers.

Calculating the packet dynamic energy cost under congestion for the WH, GuarVC, and SpecVC routers showed no significant variation in this value under different traffic levels. This was again seen to be caused by the data path dominating the energy cost. Since effective clock-gating ensured that the data-path computation did not significantly change with congestion, the energy cost of this did not change either.

For the packet switched routers, performance analysis demonstrated the effects of various tradeoffs in the router designs. Dynamic allocation and virtual channels as implemented in the SpecVC design greatly reduced the packet latency under

random packet injection while the specialized, QoS supporting design of the GuarVC router offered low latency for GT traffic.

The measured energy and latency results are combined into an ELP metric that represents the efficiency of a router architecture for a specific traffic scenario. The specialized design of the GuarVC router allowed it to have a high efficiency value for GT traffic. For the more general WH and SpecVC routers, the efficiency metric importantly showed that the additional power investment made by the SpecVC router resulted in directly proportional performance returns. In the microprocessor domain, the related work of *Microprocessor Efficiency Eras* motivates the use of the highest performance microprocessors that still operate in the highest efficiency regions for CMP systems. Similarly, the router efficiency results favor the use of SpecVC like designs over WH like designs to return the highest performance at no reduction in the power efficiency.

Finally, the area reported for the four routers means that the area impact on the full system of using these NoCs can be easily evaluated.

## REFERENCES

- [1] L. Benini and G. D. Micheli, "Networks on chips: A new SoC paradigm," *Computer*, vol. 35, no. 1, pp. 70–78, 2002.
- [2] A. Banerjee, R. Mullins, and S. Moore, "A power and energy exploration of network-on-chip architectures," in *Proc. 1st Int. Symp. Netw.-on-Chip (NOCS)*, May 2007, pp. 163–172.
- [3] T. N. Mudge, "Power: A first class design constraint for future architecture and automation," in *Proc. HIPC*, 2000, pp. 215–224.
- [4] H. Wang, X. Zhu, L.-S. Peh, and S. Malik, "Orion: A power-performance simulator for interconnection networks," in *Proc. 35th Ann. Int. Symp. Microarch. (MICRO)*, Nov. 2002, pp. 294–305.
- [5] X. Chen and L.-S. Peh, "Leakage power modeling and optimization in interconnection networks," in *Proc. Int. Symp. Low Power Electron. Des. (ISLPED)*, New York, 2003, pp. 90–95.
- [6] J. Xi and P. Zhong, "A transaction-level NoC simulation platform with architecture-level dynamic and leakage energy models," in *Proc. 16th ACM Great Lakes Symp. VLSI (GLSVLSI)*, New York, 2006, pp. 341–344.
- [7] N. Banerjee, P. Vellanki, and K. S. Chatha, "A power and performance model for network-on-chip architectures," in *Proc. Conf. Des., Autom. Test Eur. (DATE)*, Washington, DC, 2004, p. 21250.
- [8] R. Mullins, "Minimising dynamic power consumption in on-chip networks," in *Proc. Int. Symp. Syst.-on-Chip (SoC)*, Tampere, Finland, Nov. 2006, pp. 1–4.
- [9] J. Dielissen, A. Rădulescu, and K. Goossens, "Power measurements and analysis of a network on chip," Philips Research, Eindhoven, The Netherlands, Tech. Note 2005/00282, Apr. 2005.
- [10] K. Lee, S.-J. Lee, and H.-J. Yoo, "Low-power network-on-chip for high-performance SoC design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 2, pp. 148–160, Feb. 2006.
- [11] P. T. Wolkotte, G. J. M. Smit, G. K. Rauwerda, and L. T. Smit, "An energy-efficient reconfigurable circuit-switched network-on-chip," in *Proc. 19th IEEE Int. Parallel Distrib. Process. Symp. (IPDPS)*, Washington, DC, Apr. 2005, p. 155.
- [12] N. Kavalidjiev, "A run-time reconfigurable network-on-chip for streaming DSP applications," Ph.D. dissertation, Dept. EEMCS, Univ. Twente, Enschede, The Netherlands, Jan. 2007.
- [13] R. Mullins, A. West, and S. Moore, "The design and implementation of a low-latency on-chip network," in *Proc. Conf. Asia South Pac. Des. Autom. (ASP-DAC)*, Piscataway, NJ, 2006, pp. 164–169.
- [14] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.
- [15] Magma, San Jose, CA, "Quickcap datasheet," 2007. [Online]. Available: <http://www.magma-da.com>
- [16] ARM, Cambridge, U.K., "ARM926EJ-S overview," 2008. [Online]. Available: <http://www.arm.com>
- [17] H. Wang, L.-S. Peh, and S. Malik, "A technology-aware and energy-oriented topology exploration for on-chip networks," in *Proc. Des., Autom. Test Eur. (DATE)*, Mar. 2005, pp. 1238–1243.

- [18] D. Greenfield, A. Banerjee, J.-G. Lee, and S. Moore, "Implications of Rent's rule for NoC design and its fault-tolerance," in *Proc. NOCS*, 2007, pp. 283–294.
- [19] N. Jouppi, "The future evolution of high-performance microprocessors," in *Proc. 38th Ann. IEEE/ACM Int. Symp. Microarch. (MICRO 38)*, Washington, DC, 2005, p. 155.



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