$V_{(n)}$ and $J_{(n)}$ are functions of position, $0 \leqslant X \leqslant L$. The coefficients $J^{(m)}$ are derivatives of the intrinsic diode characteristic at $V = V_0$ (8).

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# An Area-Variable MOS Varicap and Its Application in Programmable TAP Weighting of CCD Transversal Filters

A. B. BHATTACHARYYA AND HANS WALLINGA

*Abstract*—**A new three-terminal MOS varicap is proposed where the terminal capacitors are made voltage variable not by the modulation of depletion width but by changing the area of inversion under the gate. An MOS capacitor realized on silicon with an impurity gradient along the surface provides the control on the area of inversion because the gate threshold voltage is determined by the doping concentration at the surface.**

**The inhomogeneous doping along the surface is implemented making use of the lateral diffusion from a doped oxide surface. Fabrication details of the capacitor compatible with n-channel silicon gate technology are presented. The $C$-$V$ relationship for the terminal capacitors is simulated by a piecewise model and agreement with measured results is shown.**

**The Area-Variable MOS Varicap (AVMOSV) is used in implementing an electrically programmable CCD filter with variable TAP weighting. Computer simulation shows considerable promise of area-variable capacitors in TAP weight control and transversal filter realization. Preliminary performance characteristics of a programmable CCD filter are presented.**

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A. B. Bhattacharyya is with the Centre for Applied Research in Electronics, Indian Institute of Technology, Hauz Khas, New Delhi, 110 016 India.

H. Wallinga was with the Solid State Electronics Group, Department of Electrical Engineering, The Twente University of Technology, 7500 AE Enschede, PB 217, The Netherlands. He is now on a visiting assignment at General Electric Company, Schenectady, NY 12301.

## I. Introduction

VOLTAGE VARIABLE CAPACITORS or varicaps have found a wide range of applications such as voltage controlled oscillators, tunable integrated circuits, FM deviators [1], and specific tuning elements [2], [3], etc. Generally, such capacitors are two-terminal elements realized with a p-n junction or MOS structure and their capacitance variation with voltage depends on the principle that the depletion width either at the p-n junction or at the semiconductor-insulator interface in the deep depletion mode can be controlled electrically. Since the capacitance is directly proportional to the area and inversely proportional to the depletion width, conventional capacitances with a given area decrease with increasing voltage. There are, however, specific needs where more functional flexibility is required such as in a high-frequency switching application when a three-terminal structure is suitable [4].

On-chip MOS varicaps have been used recently for introducing a compact circuit for programming the TAP weights of a CCD filter electronically [5], [6]. In such implementations, the sense gates of a CCD are loaded by varicaps and a parallel sense capacitor. The part of the CCD image-signal charge through the sense capacitor depends on the ratio of the variable MOS capacitor value and fixed sense capacitor. This part or fraction is controlled or programmed by voltage. The advantage of capacitive weighting is the low power dissipation and smaller chip area compared to the structures where a combination of a floating sense gate and a buffer circuit performs

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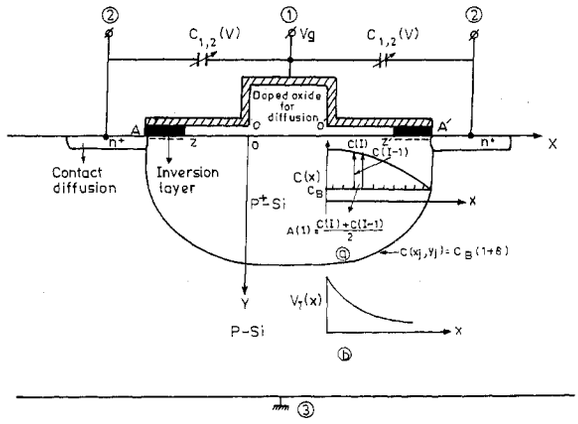


Fig. 1. The proposed area-variable MOS varicap structure on inhomogeneously doped surface. 1) The thick doped oxide serves as diffusion source. 2) Inset (*a*) shows the impurity profile along the surface. 3) Inset (*b*) shows the threshold voltage variation along the surface.

a charge-to-voltage conversion and variable TAP weighting is obtained by means of an MOS transistor acting as an analog multiplier [7], [12] or variable conductance MOST devices [8]. In the varicap-based implementations realized thus far, the sensed charge was only 10 percent of the signal charge in a CCD and, therefore, the insertion loss was high [5].

In this paper, a new three-terminal MOS varicap is proposed where the terminal capacitors are made voltage dependent by effecting variations in the effective area rather than in the depletion layer width. An MOS capacitor on an inhomogeneously doped silicon surface provides the possibility of realizing the voltage controlled area of the inversion layer since the threshold voltage has a dependence on doping. Such an area-variable three-terminal capacitor, in a very compact and elegant manner, integrates the basic functional requirement of programmable capacitive TAP weighting required for CCD transversal filtering. It also offers significant advantages over schemes belonging to this category in terms of the economy of the silicon area, the capability of relative TAP weight variation, and the insensitivity to parasitics inherent in such configurations.

In the following sections, the basic physics of the area-variable MOS varicap, its fabrication, computer simulation for the $C$-$V$ characteristics, and its application to the realization of programmable CCD transversal filtering are presented.

## II. Principle of an Area-Variable MOS Varicap (AVMOSV)

The principle of operation of an AVMOSV is illustrated in Fig. 1, where along the surface of p-type silicon an impurity gradient is realized along $0A$ and $0'A'$. In a practical implementation this is achieved by carrying out diffusion from the doped oxide source between 0 and $0'$ which results in a vertical diffused profile along the $y$-direction and a horizontal impurity gradient along the $x$-direction due to lateral diffusion. Subsequently, an MOS capacitor is fabricated on the inhomogeneous surface $0A$ and $0'A'$.

It is known that the threshold voltage in an MOS structure depends on the doping concentration at the interface; it increases with doping. Thus for the MOS capacitor extending over the region $A$ to $A'$, the gate voltage required for surface inversion at 0 and $0'$ is larger than that required at $A$ and $A'$ since concentration of impurity decreases from 0 to $A$ and $0'$ to $A'$. In other words, if the gate bias is swept over the threshold voltage range covering the doping at $A/A'$ and $0/0'$, the inversion layer will spread from $A$ to 0 and $A'$ to $0'$. Thus the area under inversion is controlled electronically.

For the p-substrate under consideration, the inversion charge is made of electrons. An electrical contact with the inversion layer is established through $n^+$-diffused region.

The above structure can be visualized as a three-terminal capacitor with a single control terminal. The configuration leads to two capacitive components:

1) The oxide capacitor $C_{1,2}$ between the gate terminal ① and the inversion layer accessed through ②. In the illustration shown in Fig. 1, the capacitance $C_{1,2}$ is determined by the inversion length $AZ$ ($A'Z'$) and the gate width $W$, i.e., the area and the oxide thickness. With increasing gate voltage the area of inversion and hence the capacitance $C_{1,2}$ increases.

2) $C_{1,3}$ is the capacitor between the controlling gate terminal ① and the substrate ③. In the given diagram the region under $Z(Z')$ to $0(0')$ is still uninverted because the applied gate voltage is less for inverting this region with higher doping. The uninverted region will contribute a capacitance between gate and substrate which is composed of a series combination of oxide capacitance and depletion capacitance. The contribution of capacitor due to the part $00'$ is negligible due to thick oxide.

In the previously mentioned structure as the area under inversion increases, that in a noninverted condition decreases. Thus with an increase in the gate voltage at ①, $C_{1,2}$ increases and $C_{1,3}$ decreases.

It may be noted that unlike conventional MOS or p-n junction varactors, the voltage dependence on the capacitor is not due to modulation of the depletion layer width but due to the variation in the area determining the capacitance.

## III. Fabrication

An AVMOSV was fabricated using n-channel Si-gate technology. As shown in Fig. 1, the thick doped oxide defines the source for lateral and vertical diffusion. Under the doped oxide $00'$, at the surface ($y = 0$), the surface concentration $C_s$ is the highest. The essential components of the capacitor, defining the masks, are the thick oxide for lateral diffusion $n^+$-contact diffusions, thin gate oxide, and the top poly-Si gate electrode. Fig. 2 gives the process sequence based on CVD techniques used for doping and poly-Si realization. Some of the relevant technological details are outlined in the diagram.

## IV. Computer Simulation and Experimental Results

The doped boron oxide provides the impurity gradient of boron impurities in p-substrate. The contour of the diffused boron impurities $C(x_j, Y_j) = C_B(1 + \delta)$ defines the so-called diffusion depth of boron in p-Si where $C_B$ is the substrate im-

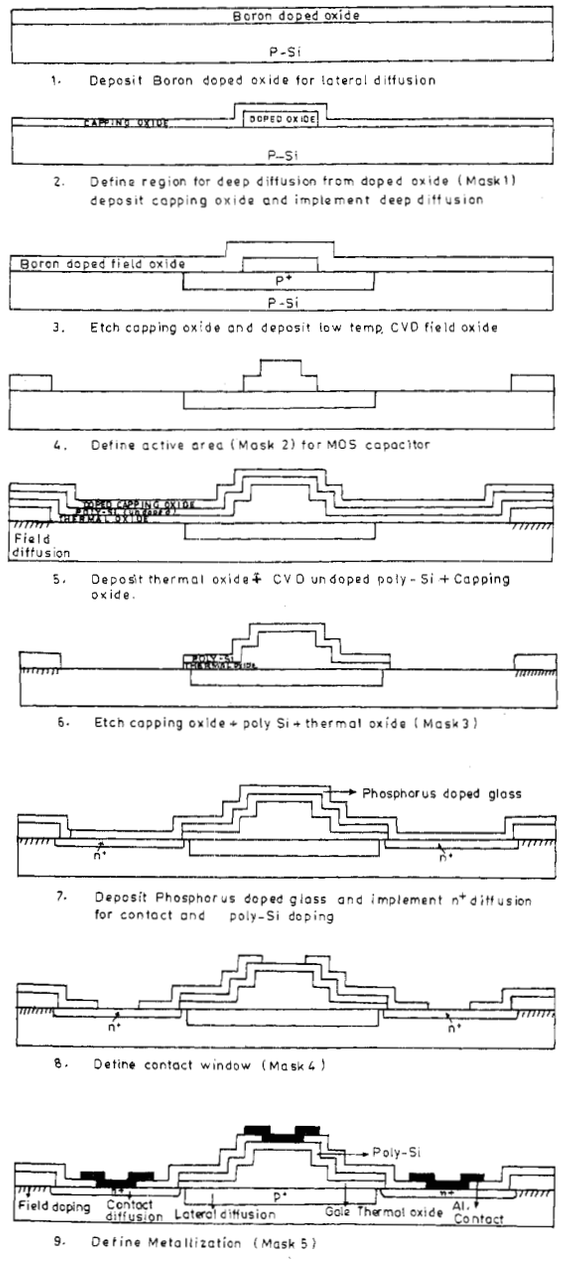


Fig. 2. n-channel Si-gate process for area-variable MOS varicap.

purity concentration and $\delta$ is an arbitrarily small number. The impurity profile $C(x, y)$ is well established from the work of Kennedy and O'Brien [9].

A piecewise model is developed for the theoretical estimation of the $C$-$V$ relationship between terminals ① and ② and ① and ③ as an analytic relation does not seem to be possible with the realistic impurity distributions along the surface. A computer simulation is adopted based on the following relations:

1) From the two-dimensional profile

$$C(x, y) = C_s \left[1 - \operatorname{erf}\left(\frac{x}{2\sqrt{Dt}}\right)\right] \exp(-y^2/4Dt) + C_B$$

the impurity profile along the surface is obtained by putting $y = 0$. Thus

$$C(x, 0) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) + C_B$$

where $D$ is the diffusion coefficient of the impurity at the diffusion temperature, $t$ is the duration of diffusion, and $C_s$ is the surface concentration under the doped oxide.

2) The stretch $0A/0'A'$, over which the doping is inhomogeneous, is subdivided into a number of smaller equal parts, say $N$, and within each part of the impurity is assumed to be a constant given by an average of the boundary values of the section. In other words, $A[I] = (C[1] + C[I-1]/2)$ is the average concentration of the $I$th section as shown in the inset of Fig. 1. The count is assumed to start from $0(0')$. $A[I]$ is the assumed constant in a given section.

3) The threshold voltage corresponding to $A[I]$, in a p-substrate, is given by [10]

$$V_T[I] = \phi_{MS} + 2\phi_F(I) - \frac{Q_{ss}}{C_{OX}} + \frac{Q_B[I]}{C_{OX}} \tag{1}$$

where

$$\phi_F[I] = \frac{kT}{q} \ln \frac{A[I]}{n_i},$$

$n_i$ being the intrinsic carrier concentration

and

$$Q_B[I] = \sqrt{2\epsilon_{Si}\epsilon_0 qA[I]\,|2\phi_f|}. \tag{2}$$

The symbols have their appropriate meanings and signs given in the reference quoted.

4) If the gate voltage $V_g$ corresponds to the threshold $V_T[I]$ of the $I$th section, then the sections from 1 to $I$ are noninverted and those from $I$ to $N$ are inverted. Thus the capacitance $C_{1,2}$ between the terminals ① and ② due to the oxide sandwiched between the gate and the inversion layer is given by

$$C_{1,2}\big|_{V_g = V_T[I]} = C_{OX} \sum_{I}^{N} (\Delta X \cdot W) \tag{3}$$

where $C_{OX}$ is the oxide capacitance per unit area, $\Delta X$ is the length of each section and $W$ is the width of the gate.

As $I$ sweeps from 1 to $N$ a relation between $C_{1,2}$ and $V_g$ is constructed for the range of voltage when capacitance variation is effected.

5) The capacitance $C_{1,3}$ seen between the terminals ① and ③ is that due to the noninverted part and is contributed by the series combination of the oxide and depletion capacitance.

If the gate voltage $V_g = V_T[I]$ causes inversion up to $I$th section, the sections ranging from 1 to $(I-1)$ contribute to $C_{1,3}$. Thus

$$C_{1,3}\big|_{V_g = V_T[I]} = \sum_{(I-1)}^{1} C_T\,|\,V_g = V_T[I] \cdot (\Delta X \cdot W) \tag{4}$$

where

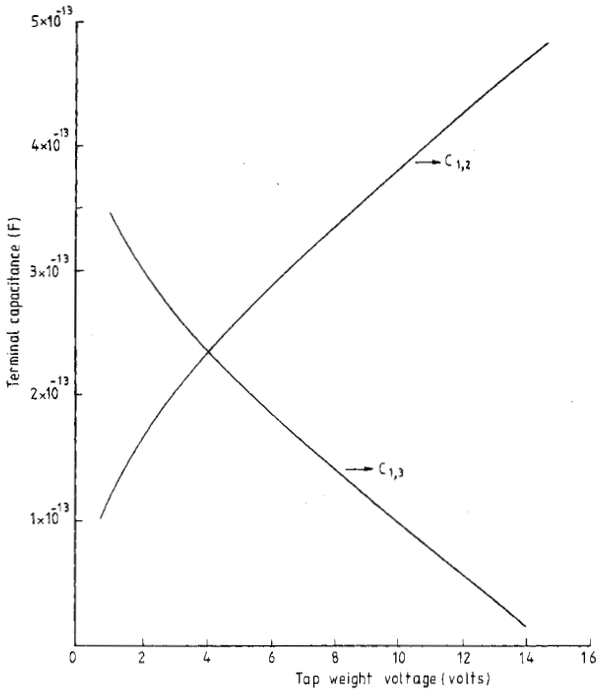


Fig. 3. Simulated $C$-$V$ relation for three-terminal silicon gate (n-type) AVMOSV—$C_{1,2}$ and $C_{1,3}$—based on piecewise model. Parameters used: capacitor width: $W = 175\ \mu m$, capacitor length: $L = 8.0\ \mu m$; surface concentration $C_s$ under doped oxide = $10^{18}/cm^3$, background concentration $C_B = 10^{15}/cm^3$, oxide thickness $t_{ox} = 0.1\ \mu m$, and $\sqrt{Dt} = 1.8\ \mu m$ (diffusion temperature).

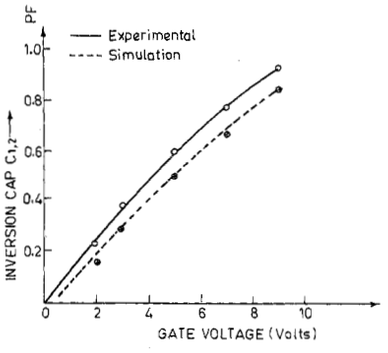


Fig. 4. Measured $C$-$V$ variation $C_{1,2}$ between gate and one of the diffused contacts on the prototype device. Parameter: $C_s = 10^{18}/cm^3$, $C_B = 10^{15}/cm^3$, $W = 500\ \mu m$, $t_{ox} = 0.1\ \mu m$, and $\sqrt{Dt} = 2.2\ \mu m$ (diffusion temperature 1200°C and duration 12.5 h). —— measured variation and ---- simulated variation.

$$C_T\big|_{V_g = V_T[I]} = \frac{C_{OX}}{\sqrt{1 + (2V_T[I]\ C_{OX}^2/qA[I]\ (\epsilon_0\epsilon_{Si}))}} \tag{5}$$

gives the capacitance of each section between gate ① and substrate ③ in the noninverted part [10].

As in the case of $C_{1,2}$, the voltage dependence of $C_{1,3}$ is also simulated as the gate voltage $V_g = V_T[I]$ is ranged for values of $I = 1 \cdots N$. $N$ in the present case is taken to be 40.

The capacitance voltage relation obtained theoretically both for $C_{1,2}$ and $C_{1,3}$ is shown in Fig. 3.

Fig. 4 shows the simulated result for the parameters of the fabricated device and the experimental plot of the capacitor between the gate voltage and one of the diffused contacts.

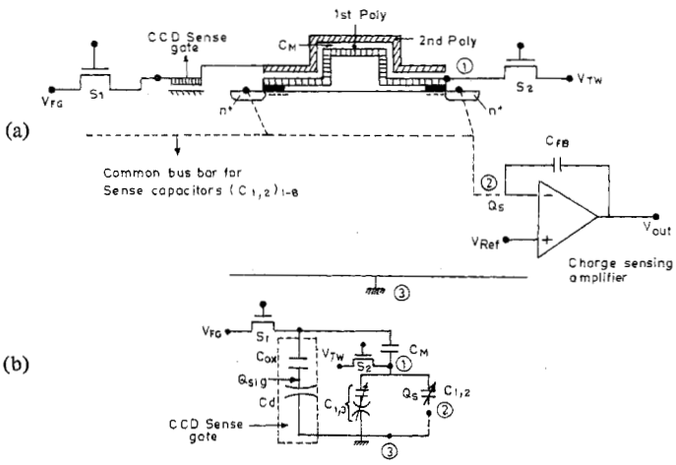


Fig. 5. (a) Schematic of capacitive TAP weighting of the CCD sense gate. (b) Equivalent circuit of the TAP weighting circuit ignoring parasitics.

The measurement was made by a three-terminal GR Bridge (1615-A) and the device was housed in a specially made jig to reduce the parasitics.

The close agreement between the simulation and experiment demonstrates the validity of the concept and the model.

We shall demonstrate the potential of the three-terminal varicap in an important application such as TAP weighting in a programmable CCD filter.

## V. Application of AVMOSV in Programmable TAP Weighting of CCD Transversal Filters

A three-terminal capacitor is ideally suited for realizing the TAP weight control of a programmable CCD filter. The AVMOSV described thus far is shown to be compatible to n-channel Si-gate technology and is thus integrable with the TAP sensing circuit of a CCD filter. The attraction of varicap TAP weighting in a CCD filter lies in the fact that such a TAP weight circuit does not dissipate any power in addition to having the property of analog memory for the reference signal.

The basic principle of capacitive TAP weighting can be explained with the help of Fig. 5. The CCD sense gate is loaded capacitively with a parallel combination of $C_{1,2}$ and $C_{1,3}$. The sense gate of CCD is given a floating potential, for proper operation, through the switch $S_1$. When a signal charge appears at the Si-$SiO_2$ interface of the sense gate, the image charge flows through the load to preserve the charge neutrality. The amount of charge branching through $C_{1,2}$ and $C_{1,3}$ depends on their relative values. For a given signal charge $Q_{sig}$, the charge stored by $C_{1,2}$ is given by

$$[Q]\ C_{1,2} = \frac{C_{1,2}}{C_{1,2} + C_{1,3}}\ Q_{sig} = h \cdot Q_{sig} \tag{6}$$

where

$$h = \frac{C_{1,2}}{C_{1,2} + C_{1,3}}. \tag{7}$$

From (7), it is seen that the value of $h$, a multiplier of the

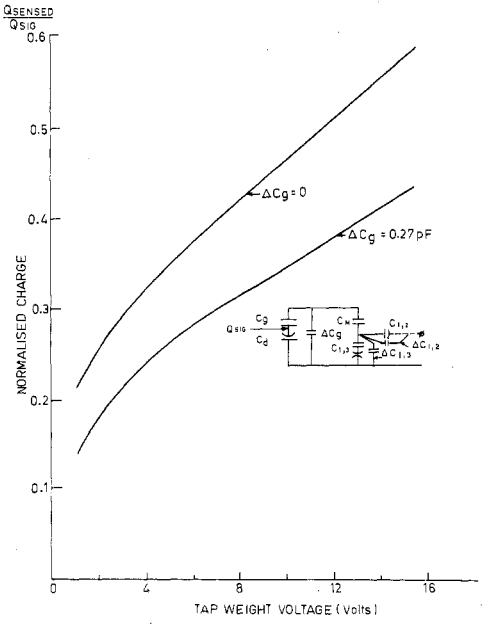


Fig. 6. Charge sensed by $C_{1,2}$ as normalized with respect to the CCD signal charge versus TAP weight voltage. $C_M = 1.2$ pF, $C_g = 0.73$ pF, $C_g = 0.27$ pF, $C_d(\phi_s = 8\text{ V}) = 0.18$ pF, and $C_{1,3} = 1.5$ pF.

signal charge, can be changed or programmed if $C_{1,2}$ or $C_{1,3}$ or both can be controlled electronically.

In an earlier realization of a programmable TAP weighting $C_{1,2}$ was a fixed capacitor and $C_{1,3}$ was a conventional MOS varicap [5]. Since $C_{1,3}$ could only be changed to a limited extent, the structure could modulate the image charge only by 10 percent to implement filter realization. Further, $C_{1,2}$ and $C_{1,3}$ were two separate entities requiring a large silicon estate.

With AVMOSV the two components $C_{1,2}$ and $C_{1,3}$ are inherently integrated into a single compact structure. Further, as $C_{1,2}$ increases, $C_{1,3}$ decreases due to the variation in area whereas, the total area remains constant. Thus $C_{1,2} + C_{1,3}$ is almost constant and the charge modulation capacity governed by $[Q]\,C_{1,2}$ depends on the variation $C_{1,2}$ with voltage.

Before we obtain the expression for the charge sensed by $C_{1,2}$ it will be appropriate to explain the charge-sensing circuitry as shown in Fig. 6. The capacitor $C_M$ realized between two poly-Si layers isolates the floating CCD sense gate from the TAP weight voltage set by switch $S_2$. Two diffusion contacts for the inversion layers are joined and connected to the negative terminal of the charge-sensing amplifier. The capacitors in the present configuration are connected in parallel; if necessary, they could be used as a single element.

It can be shown from the elementary principle of charge sharing between parallel capacitors that the charge $[Q]\,C_{1,2}$ sensed by the charge sensing amplifier is given by [13]

$$\frac{[Q]\,C_{1,2}}{Q_{\text{sig}}} = \frac{(C_{1,2} + C_{1,2})\,C_g C_M}{C_E(C_M + C_{1,2} + \Delta C_{1,2} + C_{1,3} + \Delta C_{1,3}) + C_M(C_{1,2} + \Delta C_{1,2} + C_{1,3} + \Delta C_{1,3})\,(C_d + C_g)} \tag{8}$$

where

$$C_E = \frac{C_d \Delta C_g + C_g \Delta C_g + C_d C_g}{C_d + C_g}. \tag{9}$$

$C_{1,2}$ is the intrinsic sense capacitor between terminals ① and ② of AVMOSC. $C_{1,3}$ is the intrinsic shunt capacitor between terminals ① and ③ of AVMOSC. $\Delta C_{1,2}$, $\Delta C_{1,3}$ are the parasitic capacitances between terminals ①, ② and ①, ③, respectively. $C_M$ is the isolation capacitance between sense gate and TAP weight capacitor. $\Delta C_g$ is the overlap capacitance of the sense gate with neighboring overlapping CCD electrodes. $C_d$ is the depletion layer capacitance under the CCD gate corresponding to the floating gate voltage.

The inset in Fig. 5 shows the capacitances mentioned above. It is evident that $\Delta C_g$, $\Delta C_{1,2}$, and $\Delta C_{1,3}$ reduce the charge modulation capability of the structure and need to be minimized for optimum performance. $\Delta C_{1,2}$ is mainly due to the overlap capacitance between gate electrode and contact diffusion, $\Delta C_{1,3}$ is contributed by the capacitance between the control gate of the AVMOSV and the substrate due to the thick oxide.

Fig. 6 illustrates the variation of $Q_{\text{sensed}}/Q_{\text{sig}}$ as a function of TAP weight voltage. It is noticed that when $\Delta C_g = 0$, the charge modulation could be as large as 60 percent of the signal charge. This happens to be a significant improvement over the performance by structures where $C_{1,2}$ is fixed and $C_{1,3}$ is a conventional varicap.

A prototype 16-bit programmable CCD filter was implemented using n-channel Si-gate technology with double-layer poly-Si gates as implemented for AVMOSV varicap fabrication. In the CCD implementation, however, the inhomogeneous doping realized along the surface from the doped oxide fell short of the desired target of 12 $\mu$m and was only 7 $\mu$m. The filter architecture is schematically presented in Fig. 7, and has the following features:

1) Dual channel 16-bit CCD with eight TAPS in each channel to ensure positive and negative TAP weighting.

2) MOST switches for setting the voltage to the CCD sense gates. Alternate fourth gate in a 4-phase structure connected to the TAP circuit is provided the floating potential through the MOST switch. Odd numbered $\phi_4$ are connected directly to dc supply of appropriate value.

3) MOST switches for TAP weight voltage setting on the AVMOSV control gate terminal.

4) On-chip impedance buffer with MOST followers, feedback capacitors with reset switches in parallel with it.

5) A common bus-bar for the sense capacitors $(C_{1,2})_{1,8}$ connected to the input of the impedance buffer.

Fig. 8 shows the photomicrograph of the programmable filter using AVMOSV TAP weight control. The performance of the filter is mainly characterized by the harmonic distortion, dynamic range, power consumption, and the linearity of the TAP weight control.[1] The TAP weight control linearity is illustrated in Fig. 9, where the filter output voltage has been plotted as a function of the differential TAP weight control voltage, applied commonly to all TAPS. The charge transfer inefficiency of the filter devices was $10^{-4}$ per transfer. In Fig. 10, the TAP weights have been set to a binary 5-bit

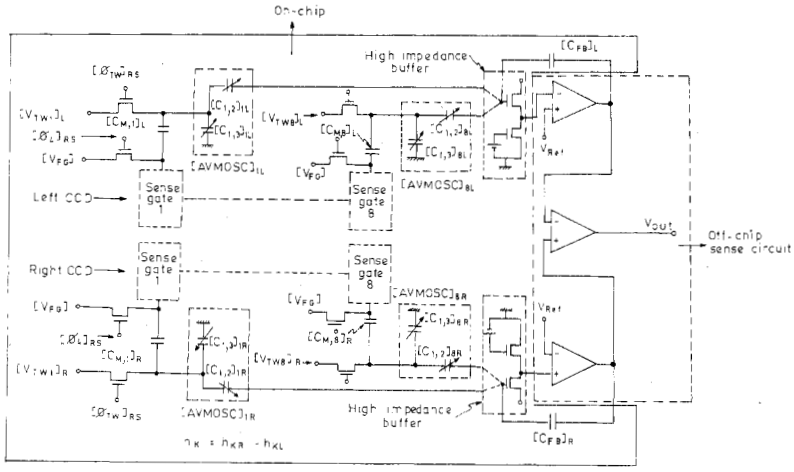


Fig. 7. CCD programmable filter architecture with AVMOSV TAP weighting. R = Right, L = Left.

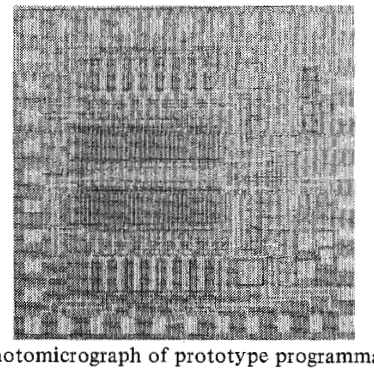

Fig. 8. Photomicrograph of prototype programmable filter.

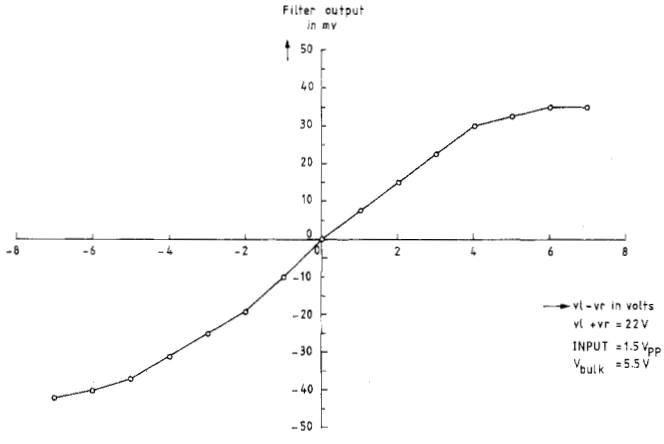


Fig. 9. Filter output voltage as a function of differential TAP weight control voltage for programmable TAP's.

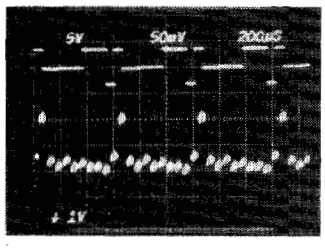


Fig. 10. Matched filter response (lower trace) on a 5-bit Barker code. Impulse response of the filter is (1, −1, 1, 1, 1).

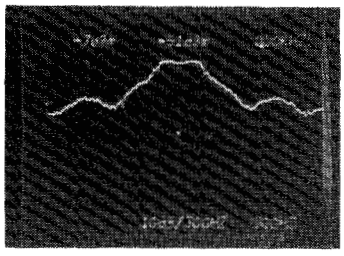

Fig. 11. Frequency response of an integral filter with same TAP weight voltage setting. Sidelobe rejections and nulls are as theoretically expected.

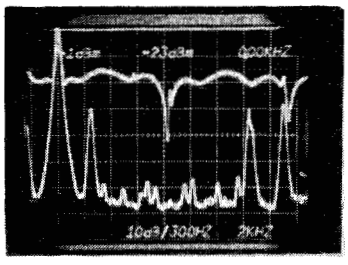

Fig. 12. Response of a seven-element Hilbert transformer. $h_0 = -0.12$, $h_2 = -0.6$, $h_4 = +0.6$, $h_6 = +.12$, $h_1 = h_3 = h_5 = 0$. Lower trace depicts the harmonic distortion.

Barker code: 1, 1, 1, −1, 1, and the impulse response as well as the autocorrelation with an equal input code are shown. As a rough measure of the similarity of the filter coefficients on integral response filter was studied with the same setting for the TAP weight voltage. With a block input signal an expected convolved triangular shaped output resulted with no visible distortion. The frequence response of such a filter with a sample-hold output is of the form $(\sin N\omega/2)/(\omega/2)$, where $N = 8$ for the present case and $\omega$ is the angular frequency. The experimental response with equal TAP voltage setting is shown in Fig. 11 which matches the theoretical expectations excellently, indicating that there is no serious TAP-to-TAP variation. Harmonic distortion measurements have been performed on the filter, programmed as a Hilbert transformer with a 1-percent ripple in the passband as shown in Fig. 12. The second harmonic distortion was below −30 dB for 10-percent fat

zero for a 1.5-V peak-to-peak input and with no substrate bias. Under the same operating conditions the CCD itself had a second harmonic distortion of -35 dB.

## VI. Discussion and Conclusion

A novel three-terminal voltage variable MOS capacitor has been realized which has been used successfully in analog TAP weighting of a CCD transversal filter. In such a varicap based TAP weighting, the power consumption is restricted merely by the normal CCD delay line (if sense amplifiers are excluded) as no dc current paths exist in the charge redistribution floating gates. TAP weighting varicaps and switches thereby offering attraction when low power consumption is the priority. Compared to filter structures of the same family of varicap weighting the present structure provides an advantage of about a 25-percent silicon estate in the TAP weighting circuit as AVMOSV realizes in a single compact structure the function of two separate capacitors used earlier [5]. In addition, AVMOSV TAP weighting can be shown to be less sensitive to parasitics than the structure in [5].

The fidelity of the CCD filter was demonstrated through an integral filter, a Hilbert transformer, and a Barker-coded matched filter. The present design aimed for larger TAP weight variation rather than on low distortion performance. Optimization on the varicap circuit promises room for improvement on the distortion.

Further, the reported performance on a device processed nonoptimally regarding the realization of inhomogeneous doping on the surface and with an optimal processing performance is expected.

The AVMOSV realization also demonstrates the possibility of varying the area of a diode with voltage which may find useful application in electronic programmability of other devices such as in distributed $RC$ structures.

An additional degree of flexibility in the $C$-$V$ relationship may be added by shaping the gate of the MOS capacitor appropriately.

A detailed circuit performance of the above filter is being studied [11].

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