Ultrafast All-Optical Shift Register and Its Perspective Application for Optical Fast Packet Switching

Bo Tian, *Student Member, IEEE,* Wim van Etten, *Senior Member, IEEE,* and Wim Beuwer

***Abstract*—SEED (self-electrooptic effect device) configuration, symmetric- (S) SEED switching characteristics, a single all-optical memory cell, and the packet switch structure are briefly introduced. By applying a planar integrated optical circuit based on SEEDs, the demonstration of an all-optical memory cell, which can be used in optical switching and optical data storing is introduced by using master-slave integrated configuration of SEEDs. The system structure, the switching performance, and the dependence of the switching speed are discussed. Based on these performance analyzes, some improved schemes are presented. By applying a pair of external preset pulses and integration of inductors, the SEED's devices even can provide 50 Gb/s throughput with data power of 1 mW, this is very competitive for optical communication. Based on these analyzes, an all-optical shift register that utilizes SEEDs embedded in the connecting optical waveguides is presented. Considering its advantage of application in optical packet header processing, we present the application of this all-optical shift register in an optical multiprotocol label switching switch.**

***Index Terms*—Optical fiber communication, optical switches, optoelectronic devices, packet switching.**

I. Introduction

HIGH-PERFORMANCE digital application systems that address services such as: asynchronous transfer mode, IP/Tag switching and multiprotocol label switching (MPLS) switching, motivate the development of high-speed all-optical switches. By deploying high-speed all-optical switches, the signal conversions between the optical domain and electrical domain that are normally needed before and after the switch nodes can be avoided. A breakthrough can be created in the so-called "electronic bottleneck" (slow electronic processing, such as switching, in an inherently fast optical transmission system). Optical fast packet switching is believed to be the potential candidate for the future optical transport network (OTN). This paper will aim at the analysis and implementation of an all-optical shift register, which can ideally be the heart of an all-optical packet switch.

The self electrooptic effect device (SEED) is one of the few existing optical components allowing for high-speed all-optical signal processing. SEEDs have been demonstrated with switching times up to 33 ps [1] and switching energies as low as 5.9 fJ/μm^2 [2], even less at 4.1 fJ/μm^2 for extremely shallow quantum-well SEED (E-SEED) and 3.0 fJ/μm^2 for an impedance-matched asymmetric Fabry–Pérot ESQW S-SEED (AE-SEED) [3], which is very promising for all-optical processing.

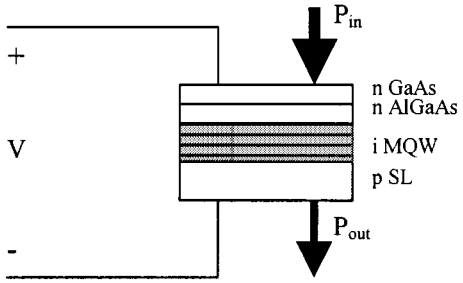

Fig. 1. Schematic diagram of the SEED configuration.

Several structures of optical switch prototypes based on S-SEEDs have been reported [4]–[8]. Compared with these reported optical interconnection systems, the integrated scheme we present here can replace the necessary mirror arrays, zoom lenses etc., and therefore, it is easier to realize, more compact, and more stable.

II. Self Electro-Optic Effect Devices

SEED's operation is based on the effect that is called the quantum confined stark effect (QCSE). This relies on changes in the optical absorption that can be induced by changes in an electric field perpendicular to the thin semiconductor layers in QW material. In QCSE, electric fields applied perpendicular to the QW layers can shift the optical absorption edge to lower photon energies with the exciton absorption peaks remaining clearly resolved. This electroabsorptive effect can be applied for high-speed optical modulators, optical switching and optical signal processing devices.

The schematic and physical layout of the device are shown in Fig. 1. The material was grown by molecular beam epitaxy on a Si-doped n-type GaAs substrate. The p region was grown as a fine-period GaAs–AlGaAs superlattice (SL) to improve the quality of the material.

The interesting electroabsorption has recently been studied at long ($\lambda \sim 1.5$ μm) and short ($\lambda \sim 0.95$ μm) wavelengths. It is very important for lightwave communication to develop materials able to show this interesting effect at long wavelengths that falls in the region of minimum fiber losses. In [9], an InP-based pin layerstack, with a single InGaAsP–InGaAs QW, suitable for

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The authors are with the Telecommunication Engineering Group, University of Twente, 7500AE Enschede, The Netherlands.

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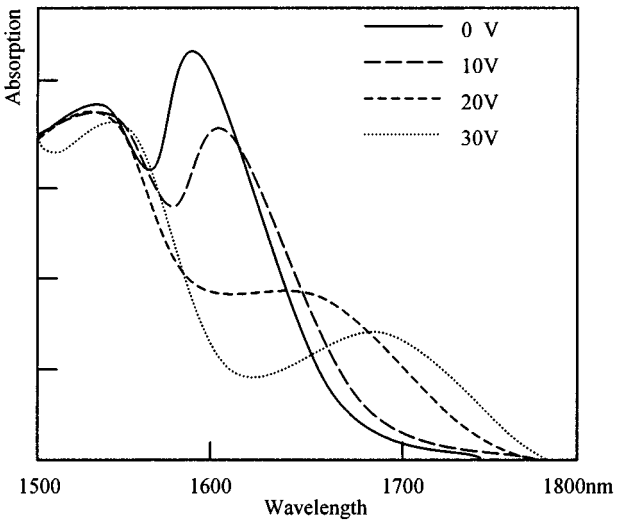

Fig. 2. Curves of the SEED absorption versus input beam wavelength with the perpendicular electrical field as parameter.

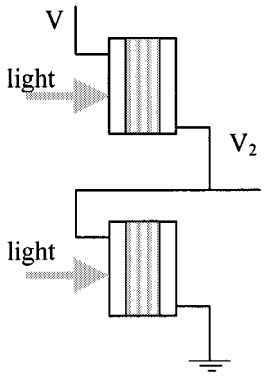

Fig. 3. Two SEEDs in cascade. The S-SEED.

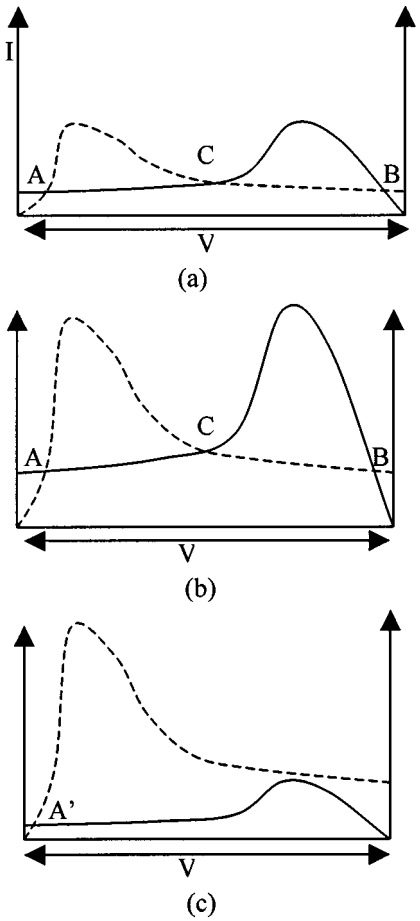

Fig. 4. I–V characteristics with different illumination situation. (a) Both of the SEEDs are equally weakly illuminated. (b) Both of the SEEDs are equally strongly illuminated. (c) One of the SEEDs is weakly illuminated, the other one is strongly illuminated.

planar integration of SEEDs working at wavelength 1520 nm, is introduced. The absorption curves of a SEED for different perpendicular electrical fields are shown in Fig. 2. From this figure, we can see increasing reverse bias shifts the absorption peak to higher wavelengths. The absorption height of the absorption resonance decreases with the increasing bias because of the reduced overlap between the electron and the hole wave functions, and the linewidth becomes wider [10].

III. S-SEEDS Switching Characteristics

SEEDs were successfully demonstrated as bistable optical devices. When using SEEDs as bistable elements in a memory cell, the devices are placed in series with an electrical load and a voltage source. The load can be a resistor or a diode, but also another SEED in such a way that each of the two SEEDs is the load for the other one, see Fig. 3. The latter configuration is called symmetric SEEDs (S-SEEDs).

S-SEEDs work as differential devices; each input and output is composed of two beams, as shown in Fig. 3. A single reverse biased SEED exhibits current–voltage (I–V) characteristics depicted in Fig. 4(a) as the dashed curve. For the S-SEEDs, where two reverse biased SEEDs are connected in series, with the equally weak optical input injecting into each SEED, composite I–V characteristic curves are shown in Fig. 4(a). When the optical powers are increased with an equal amount, the resulting curves are shown in Fig. 4(b). In these two cases, a voltage bistability exists for the S-SEEDs, indicated by the two points of intersection A and B. The third intersection point C is unstable [11]. When a pair of unequal optical beams is applied to the SEED diodes, different amounts of photocurrent are generated for the two SEEDs; this result is shown in Fig. 4(c). Only one point A is left as the final operating state. This means that the final state of the S-SEEDs is only determined by the ratio of the input power intensities impinging on both SEEDs. Another property of S-SEEDs important for our purpose is that the status of the S-SEEDs can be read and (re)set in the electrical domain as well. Reading the state can be done by measuring V_2 in Fig. 3 by applying a high impedance device. Setting the S-SEEDs electrically to a certain state is accomplished by pulling up or down the V_2 terminal.

IV. A Memory Cell Using SEEDs

Fig. 5 shows a design for an optical memory cell using SEEDs. Such a cell comprises four SEEDs, which are two by two parallel and two by two in series. The signals “Ref”

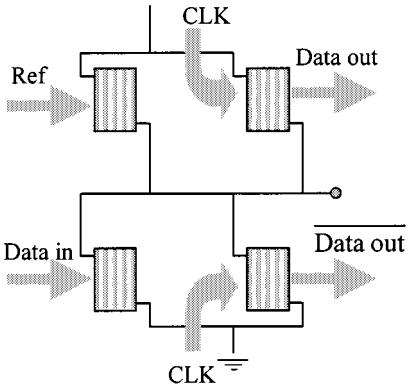

Fig. 5. A single SEED memory cell.

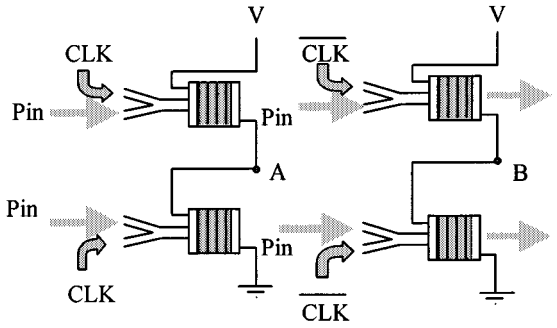

Fig. 6. A combined all-optical shift register.

and "Data in," "CLK," "Data out" and "$\overline{\text{Data out}}$" are optical signals. Two SEEDs (S-SEEDs) in series operate like a balance; the state of the S-SEEDs is determined by the level of the optical "Data in" signal compared to the "Ref" signal. The input signals will set the state of SEED memory cell, and subsequently the stronger optical clock signals can read out the state with a certain gain, so that the output signal is strong enough to drive next optical memory cell.

V. System Bit Rate

The system bit rate is limited by the time it takes for the photocurrent to charge the capacitance of the first S-SEEDs in one memory cell. This photocurrent is proportional to the optical power incident on the device windows. The system bit rate can be found by first determining the absolute powers from the output of the preceding memory cell, which are incident for the first stage devices, and then calculating the switching time of the first stage S-SEEDs in a memory cell from these inputs.

The system bit rate can be given by using the calculation in [12], [13]

$$B = \frac{1}{2kCV_0}\left\{\left[\frac{1}{P_{\text{clk}}}+\frac{1}{P_{\overline{\text{clk}}}}\right]\cdot\left[\frac{1}{T_{\text{opt}}T_{\text{on}}(1-T_{\text{on}})-T_{\text{opt}}T_{\text{off}}(1-T_{\text{off}})}+\frac{1}{T_{\text{opt}}T_{\text{on}}(1-T_{\text{off}})-T_{\text{opt}}T_{\text{off}}(1-T_{\text{on}})}+\frac{2}{(T_{\text{on}}-T_{\text{off}})}\right]\right\}^{-1}. \quad (1)$$

Here, $k = hv/q$, hv is the photon energy, q is the charge of an electron; C is the capacitance of a single SEED. T_{on} is the high transmission coefficient T_{off} is the low transmission coefficient. $P_{\overline{\text{clk}}}$ and P_{clk} are the clock power injected onto the SEED cell windows, T_{opt} is the passive waveguide connection efficiency between adjacent memory cells.

Let us consider the following practical values: $C = 12.5$ fF, $V_0 = 2$ V, $T_{\text{on}} = 41\%$, $T_{\text{off}} = 17\%$, $P_{\overline{\text{clk}}} = P_{\text{clk}} = 1$ mW and $T_{\text{opt}} = 55\%$. The system throughput can then amount to 460 Mb/s. However, the system throughput can go up to 790 Mb/s with transmission coefficients of 60% and 10%.

VI. A Combined Scheme

Based on the system performance analysis of the optical memory cell based on SEEDs, here we present an improved scheme of the all-optical shift register shown in Fig. 6.

We combine the two stages S-SEEDs as a single S-SEEDs in a memory cell; the optical input signal and optical clock signal are coupled by an effective waveguide coupler. So there are two SEEDs in a memory cell instead of four. By this way, half the amount of SEEDs can be saved; the capacity that is needed to be charged by the photocurrent will be reduced to half the amount; the capacity introduced by the electrical connection will be decreased.

This all-optical shift register operates in a time sequential manner. The lower power input signal that originates from the previous stage sets the switch state; then the higher power clock signals are applied to read the state and transfer it to the next stage. This operation brings the time sequential gain. However, operation in this way also means a tricky design of the device so that the input signals of the preceding S-SEEDs will not strong enough to change the current S-SEEDs, although it will reduce the noise tolerance.

The switching time of a stage is determined by the input signals set the switching states, the time that clock signal read out the states can be neglected. The system bit rate of the combined all-optical shift register is given as

$$B = \frac{1}{kCV_0}\left\{\left[\frac{1}{P_{\text{clk}}T_{\text{cpl}}}+\frac{1}{P_{\overline{\text{clk}}}T_{\text{cpl}}}\right]\cdot\left[\frac{1}{T_{\text{opt}}T_{\text{on}}(1-T_{\text{on}})-T_{\text{opt}}T_{\text{off}}(1-T_{\text{off}})}+\frac{1}{T_{\text{opt}}T_{\text{on}}(1-T_{\text{off}})-T_{\text{opt}}T_{\text{off}}(1-T_{\text{on}})}\right]\right\}^{-1}. \quad (2)$$

Here T_{cpl} is the coupling efficiency of the waveguide coupler applied before the SEED's window. When applied with a 3-dB waveguide coupler, $T_{\text{cpl}} = 50\%$; however, if the data signals and the clock signal's wavelength/polarization are properly separated, a wavelength-dependent/polarization-lossless coupler can be fabricated so that T_{cpl} can be one.

With $C = 12.5$ fF, $V_0 = 2$ V, $T_{\text{cpl}} = 50\%$, $T_{\text{on}} = 41\%$, $T_{\text{off}} = 17\%$, $P_{\overline{\text{clk}}} = P_{\text{clk}} = 1$ mW and $T_{\text{opt}} = 55\%$, the system through put can be 610 Mb/s, however, if a wavelength/polarization-dependent lossless coupler is applied, the system throughput can be 1.2 Gb/s. With the higher contrast

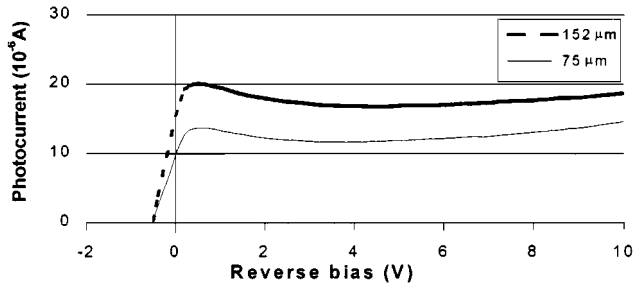

Fig. 7. Photo I–V characteristic for different SEED's waveguide lengths.

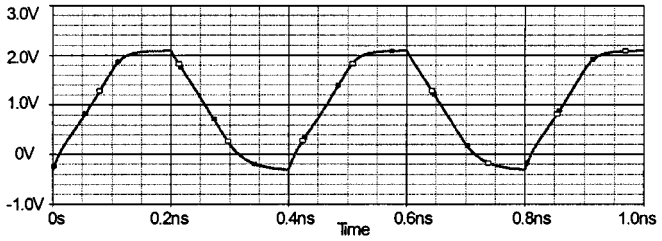

Fig. 8. Switching voltage of S-SEEDs,.The input pulse of peak value of 1 mW. The wavelength is 1520 nm.

transmission coefficients 60% and 10% [13], the system throughput is 1 Gb/s, and 2 Gb/s is possible by applying a wavelength/polarization dependent lossless coupler.

VII. Device Improvement

A SEED's photo I–V characteristic for different waveguide lengths are shown in Fig. 7. The input laser power is -6 dBm at 1520 nm; considering coupling losses of the waveguide, the estimation of the input power into the device of -12 dBm is reasonable. A region of negative differential resistance was observed in waveguides as long as 326 μm or shorter. The size of the device should be optimized; if the size is too large, the device capacitance becomes larger, as a consequence, the switching speed is lower. On the other hand, if the device is too small, the absorption of photons will be more inefficient.

There are several ways to improve the switching speed of the S-SEEDs:

1) By adding more QW layers, reducing the length of the device, the device capacitance will be decreased, however, the photo current can stay at the same level.

   With the device 75 μm long, the switching simulation was performed by applying an input data pulse of peak value of 1 mW, initial value of 0.1 mW, the referencing input power is keeping at 0.55 mW constantly; the wavelength is 1520 nm; the switching of S-SEEDs is shown in Fig. 8. The switching time can be as short as 0.125 ns, which means the S-SEED's can operate at a speed of 8 Gb/s
2) By integrating with external components as shown in Fig. 9, a pair of inductors compensate the S-SEED's capacitance. From Fig. 10, we can see by using an integrated inductor, the device switching speed can be up to 10 Gb/s.
3) By using a pair of preset pulses before the data is injected into the device.

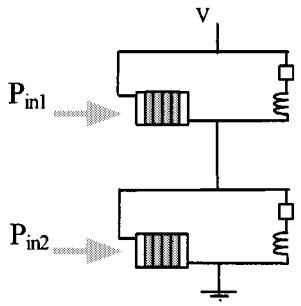

Fig. 9. Improvement of SEED by using external integrated components.

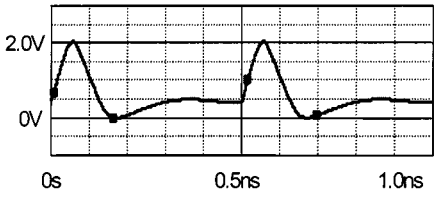

Fig. 10. Switching voltage of S-SEEDs with external resistor (12 kΩ) and inductor (1 μH).

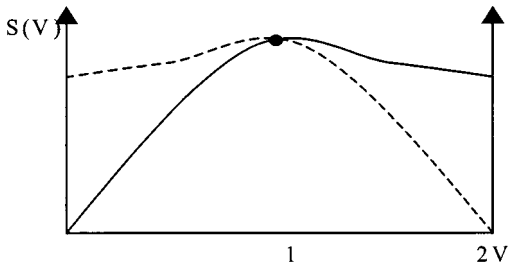

Fig. 11. I–V switching characters of S-SEEDs at longer wavelength.

This operation uses a state-preset pulse operating at a wavelength several nanometers longer than the SEEDs working wavelength. When the working wavelength is increased, the current peak will shift to higher voltage [2]. At the longer wavelength, the I–V curves tilt inward as shown in Fig. 11 resulting in a single point of intersection. If the state-preset pulses are equally applied to the SEED's windows, the S-SEEDs will be set at the unstable state until the state-preset pulses are removed. After that any difference between data pluses P_{in1} and P_{in2} will unambiguously determine the state of the S-SEEDs. This operation reinitializes the device before the inputs set the state of S-SEEDs, while allowing the clock and input signal to operate at the desired wavelength. The order of operation is 1) the state-preset pulse initializes the S-SEEDs at the unstable point; 2) the optical input data, P_{in1} and P_{in2}, determine the state of the S-SEEDs; and 3) the clock pulses read out the S-SEED's states. The switching timing is shown in Fig. 12. The rise time can be shortened to 15 ps as follows from Fig. 13, which means the speed of 33 Gbit/s is achievable. The triangle waves in Fig. 13 are introduced by the set-preset pulses, however these waves have no negative influence in noise tolerance and can be easily gotten rid of by using a diode. 3) If we combine the two methods in 2) and 3), a better improvement can be seen in Fig. 14. The rise time can be even shortened to 10 ps and the switching speed can be up to 50 Gb/s.

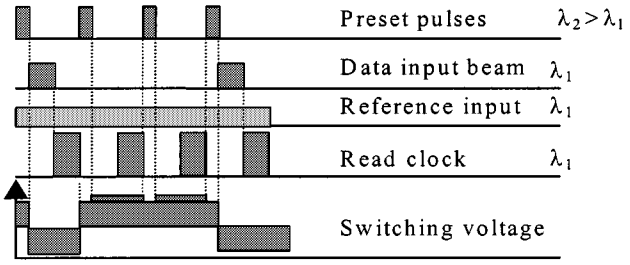

Fig. 12. Switching timing of S-SEEDs with set-preset beams.

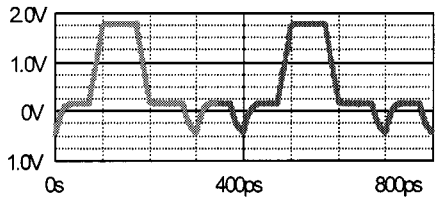

Fig. 13. Switching voltage of S-SEEDs with external 800-μW preset pulses.

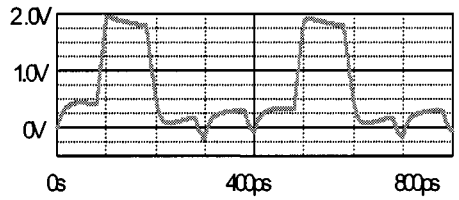

Fig. 14. Switching voltage of S-SEEDs with external resistor (12 kΩ), inductor (1 μH), and external 600-μW preset pulses.

VIII. Header Replacement in Packet Switch

In packet switching networks, from the traditional X.25, Frame Relay, ATM to MPLS switching network, information is transported in packets of a constant or flexible size. The packet size, which determines the overhead efficiency and delay, varies in different protocols. In a packet, a number of the first bits are used to store header information for routing purposes, the remaining bits form the payload for user data. The payload is transported transparently through the network; the header has to be decoded in most switch nodes. Moreover, it will have to be replaced frequently when passing a node.

In a packet switching header processor, when a complete packet has been received the header bits can be read electrically by a controller. This controller decodes the header information and determines the optical switching action from the contents of the header. Moreover, the controller establishes the new header information, encodes it and replaces the old header by the new one. After that, the new packet cell can be retransmitted.

IX. All-Optical Shift Register Based on S-SEEDs

SEEDs may influence the design of an all-optical shift register, mainly through their operational characteristics (i.e., switching energy and physical requirements). In our proposal, we intend to use a planar chip. The SEEDs are integrated into the planar chip and are connected by integrated waveguides. The data signals are coupled into the planar chip by applying a coupling system. All of the optical functions and connections are produced on chip, until the output signals come out from the chip. By using this scheme, we do not have to put most of our effort into the complex mechanical system which is used to connect the SEEDs in [4]–[6]. This will certainly bring simple, compact, and stable circuit solutions.

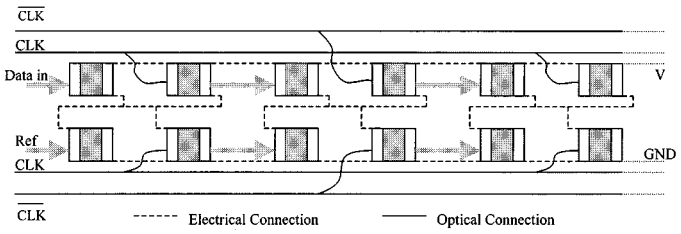

Fig. 15. All-optical shift register implementation.

The operation of S-SEEDs in general is governed by the input signal contrast. The input signal contrast is $\rho_{\rm in} = P_{\rm data\,in}/P_{\rm ref}$; for a binary one to be correctly transferred from one device to the next, $\rho_{\rm in}$ must be greater than $\sim$1.4 for a 10 V applied bias [4]. Signal contrast is affected by the S-SEEDs transmission contrast, the efficiency of the waveguide connections between the adjacent SEEDs, the transmission uniformity of the optical path, and the presence of scattered light in the system. Signal transmission efficiency is primarily determined by the optical component transmissions, but also by the overall waveguide/device coupling efficiency, as well as by any vignetting of the signal beams by the optical system.

Our proposed all-optical shift register is shown in Fig. 15. A number of S-SEEDs are cascaded in master-slave configuration. In order to get the maximum coupling efficiency, the SEEDs are embedded in the connecting waveguides. For the first cell, the initial input signal power ratio will determine the state, for the other cells the input signals can be the output signals from the preceding cell. When writing the content of a cell, the clock of that cell has to be at a low level, whereas the clock of the preceding cell should have a high level in order to provide sufficient optical power for the writing process. During the writing cycle, the clock of the cell to be written is low, so that no optical signal is supplied to the next cell. During this period, it is not allowed for the cell to provide information to the next cell. Reading the cell is accomplished by making the clock high. At the same time, the clock of the preceding cell has to be low, so that the input is not changed during the reading cycle. It is concluded that the clock signals of the adjacent cells are in antiphase and two memory cells are required for a single step in the shift register.

X. The Application of the Optical Shift Register

Multiprotocol label switching (MPLS) is a versatile solution to address the problems faced by present-day networks speed, scalability, quality-of-service (QoS) management, and traffic engineering. MPLS has emerged as an elegant solution to meet the bandwidth management and service requirements for next-generation Internet Protocol (IP)-based backbone networks. In Fig. 16, an all-optical MPLS switch based on a SEED's shift register is presented. An all-optical shift register constructed by using an S-SEED's array is used to shift the IP packets. Optical connections (i.e., passive optical waveguides) are integrated between two neighboring memory cells. The

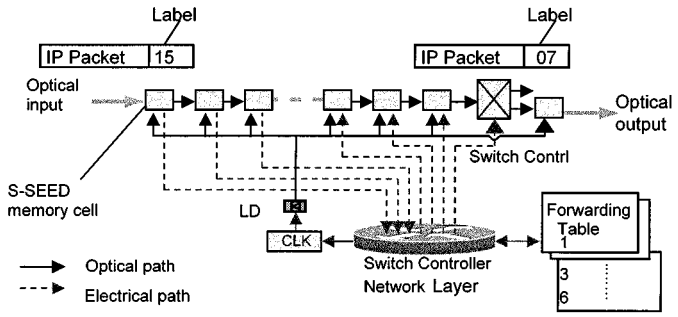

Fig. 16. The implementation of all-optical MPLS switch based on SEEDs.

clock signals of CLK and $\overline{\text{CLK}}$ can be generated by current modulating two laser diodes. After the two clock signals are coupled into the chip, they can be split by integrated beam splitters into CLK and $\overline{\text{CLK}}$ signals, which are connected to the odd memory cells and even memory cells respectively. "Data in" and "Ref" signals can be coupled into the first S-SEED's optical window by a coupling system; the input signals and optical clock signals are coupled to the SEED windows by an effective waveguide coupler. A switch controller provides the clock synchronization, interface, label swapping, and network layer routing function by reading for label switching routers (LSRs) and label edge routers (LERs) and writing the all-optical shift register for LERs.

XI. System Features and Issues

Optical power losses with the resulting decrease in system speed are perhaps the major system limitations. There are several possible ways to increase the system speed.

- Decrease the loss in the SEED's. The high state transmission of the S-SEEDs can be improved by employing extremely shallow quantum-wells (ESQW) and asymmetric Fabry–Pérot (AFP) in the p-i-n diode structure [14].
- Use higher power lasers. Currently the maximum power available in a commercial laser that has a single transverse mode is approximately 100 mW. S-SEED's switching speed is limited by the absolute input power; higher clock power certainly can result into higher output, which will influence next S-SEED's switching speed.
- Decrease the switching energies of the S-SEEDs. The switching energies of the devices can be reduced by applying either smaller device size or a reduction of the change in the applied electric field across the device when the device changes state. Smaller device size is unattractive owing to the worse absorption efficiency. One way to reduce the applied electrical field change is to develop new materials that require less change in the applied electric field.
- Apply effective waveguides for coupling input power into the SEEDs. From(2), we can see that the system speed is proportional to the input power. When the data input signal and clock signals work at the same wavelength, the minimum theoretical coupling loss 3 dB will reduce the switching speed by a factor of two compared with using a lossless coupler. However when the system is properly designed so that the input data signals and clock signals are properly separated in wavelength or polarization, a wavelength/polarization-dependent lossless coupler can be fabricated, this will result in a speed twice as fast as that of using a 3-dB coupler.

Considering the unique characteristics of optical transmission system, the scheme we presented here has certain advantages.

- Critical delay and level margins. In this optical register, a pair of "clean" optical clock signals are impinged in every optical memory cell. In this way, the optical input data signal is reshaped and regenerated in every optical memory cell. This guarantees that the critical delay and level margins are not inherited to the next memory cell.
- Signal format. From Fig. 4 we can see, once S-SEEDs are switched to a stable state, it will stay in that state even after removing the optical inputs or impinging another pair of optical signals with equal amount of power. This means that the optical input signal modulation format (RZ or NRZ) has no influence on the switching times if the optical pulse duration is longer than S-SEED's switching time.

XII. Conclusion

In this paper, SEED's device characteristics, the operation principle, and system architecture of the all-optical shift register by integration of SEEDs are discussed. The system performance, system bit rate dependence on transmission coefficients, and absorption coefficients are discussed as well. Based on these analyzes, a combined scheme is shown, with faster system throughput but less noise tolerance. We also proposed three methods to improve the switching speed of an all-optical shift register based on SEEDs, with combination of two improvements, the estimated speed of 50-Gb/s throughput is very competitive for ultrafast optical communication systems. By embedding the SEEDs into the connecting waveguides to get the maximum coupling efficiency, an optical header processing technology based on the optical SEED's shift register for an optical MPLS switch is demonstrated. For other kind of applications (i.e., optical modulator, wavelength converter or optical data storage), the same working principle is applicable. What we need to do is to produce different suitable SEED's chips.

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Bo Tian (S'02) was born in Henan, China in 1972. He received the B.E. and M.E. degrees in electrical engineering from Xi'an Jiaotong University, in 1994 and 1997, respectively.

After that, he joined Shanghai Zhongxing Telecom Institute where he worked on optical fiber access network. Since 1998, he has been working in Telecommunication Engineering group of University of Twente, The Netherlands, as a research assistant in optical communication. His current interests include optoelectronic devices, optical communications, digital signal processing and wireless communications.

Wim van Etten (M'80–SM'91) was born in Zevenbergen, The Netherlands, in 1942. He received the M.Sc. and Ph.D. degrees in electrical engineering from Eindhoven University of Technology, Eindhoven, The Netherlands, in 1969 and 1976, respectively.

From 1969 to 1970, he was employed by Philips Electronics, developing circuits for oscilloscopes. In 1970, he was appointed an assistant professor at Eindhoven University of Technology, Faculty of Electrical Engineering. From 1970 to 1976, he was engaged in research on the transmission of digital signals via coaxial and multiwire cables. Since 1976, he has been involved with research and education on optical fiber communications. In 1985, he was appointed as an associate professor at the Eindhoven University of Technology. In 1994, he has been appointed as a full professor of Telecommunications at the University of Twente, Enschede, The Netherlands. His current interests comprise optical communications, mobile communications, detection, and simulation of communication systems. He is author or co-author of over 60 papers in international journals, conferences, and symposia. He served as a member of organizing committees, programme committees and proceedings editor of various conferences and symposia. Moreover, he is first author of the text book "Fundamentals of Optical Fiber Communications," Prentice Hall, 1991.

Dr. van Etten is a member of the NERG (Dutch Institute of Electronic and Radio Engineers). Presently, he is president of the NERG, vice-chairman of the executive committee of the IEEE Benelux joint Chapter on Communications and Vehicular Technology, and member of the Organizing Committee of the URSI General Assembly, Maastricht 2002.

Wim Beuwer was born at Oldenzaal, The Netherlands, in 1943. He studied at the Technical University of Delft, Ir. titled in 1972

Until 1988, he worked at the microwave group of the University of Twente in the area of S-parameter and noise figure measurements. He then joined the Telecommunication Engineering group at the University of Twente. He has been working as assistant professor in the area of optical communications.