VIPMOS—A Novel Buried Injector Structure for EPROM Applications

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***Abstract*—A buried injector is proposed as a source of electrons for substrate hot electron injection. To enhance the compatibility with VLSI processing, the buried injector is formed by the local overlap of the n-well and p-well of a retrograde twin-well CMOS process. The injector is activated by means of punchthrough. This mechanism allows the realization of a selective injector without increasing the latchup susceptibility. The p-well profile controls the punchthrough voltage. The high injection probability and efficient electron supply mechanism lead to oxide current densities up to 1.0 A · cm^{-2}. Programming times of 10 μs have been measured on nonoptimized cells. The realization of a structure for 5-V-only digital and analog applications is viable. A model of the structure for implementation in a circuit simulator, such as SPICE, is presented.**

I. Introduction

An increasing demand exists for high-performance EPROM's and E^2PROM's in digital applications. In the near future, magnetic media may be replaced by E^2PROM's [1]. However, also in analog and analog–digital applications adjustable components are required. EPROM's can be used in analog CMOS circuits. In this way, it is possible to cancel offsets in differential amplifiers [2]. E^2PROM's may also find application in adaptive filters or in neural networks [3], [4]. In this paper we will describe a new structure for an EPROM device, which is realized by high-energy ion implantation and may be used in various EPROM applications. The paper focuses on the working principle of the realized structure and its modeling. Furthermore, programming characteristics of nonoptimized memory cells are given, in order to demonstrate its high speed potential. In a following paper, the performance of optimized cells and method of cell selection in a memory matrix will be discussed based on the evaluation of a 16K flash-E^2PROM [5].

Conventional EPROM's widely use the method of Channel Hot Electron (CHE) injection for programming. Electrons that become hot in the pinchoff region have a small probability of being injected into the gate oxide and flowing to the floating gate. The electrons should gain sufficient kinetic energy in the electrical field parallel to the Si-SiO_2 interface and then they have to be redirected towards the Si-SiO_2 interface [6]. The influence of the drain and gate voltage on the number of hot carriers and the height of the Si-SiO_2 potential barrier lead to conflicting demands [7], [8]. Therefore, high drain and gate voltages are often used as a compromise in practical programming. As a result, drain-side CHE injection EPROM's have a low injection probability. They generally do not allow 5-V-only operation, although for some drain-side CHE injection EPROM's with submicrometer channel length the programming drain voltage can be reduced to 5 V [9]. The source-side CHE injection technique can be used, in order to overcome these disadvantages [7]. However, as in the case of a drain-side CHE injection EPROM, the injection of hot electrons is limited to a very small region. As the charge injection is the driving mechanism for oxide breakdown [10], the lifetime and the number of programming cycles of such device for E^2PROM applications are restricted.

An alternative method to the CHE injection is the Substrate Hot Electron (SHE) injection, which is shown in Fig. 1. The source of electrons is the substrate. The SHE injection has several advantages. Electrons that are accelerated in the depletion layer underneath the gate and become hot are directed towards the Si-SiO_2 interface. The injection probability can be increased by raising the gate voltage, which lowers the Si-SiO_2 potential barrier [11]–[13]. In contrast to the conventional CHE injection, this can be done without decreasing the number of hot electrons. The SHE injection technique can be applied in a 5-V-only EPROM, because the only higher voltage needed on chip is connected to the gate terminal of high impedance and can be generated on chip by charge pumping techniques [14]. The injection of electrons can take place over nearly the whole active gate area. In the case of equal injection current the SHE injection offers a lower oxide current density than the CHE injection. Because the oxide is stressed less locally, a higher reliability of the SHE injection EPROM may be expected compared to the CHE injection EPROM. In addition, both normal CMOS and EPROM devices can use the same advanced source and drain structures in order to suppress unwanted short-channel effects [15].

The major problem associated with the conventional SHE injection is the method for generation of electrons in the substrate. Photogeneration and avalanche multiplication have been used. Verwey *et al.* [16] employed a forward-biased n-type substrate with a p-type epilayer. Eitan *et al.* [17] used a forward-biased p-n junction, which was situated closely to the EPROM device. Such a forward-biased p-n junction has low injection efficiency, because only a small part of the injected carriers (10^{-3} to 10^{-2} [18]) enters the depletion layer under the gate. The majority of these carriers either recombines in the substrate or are directly collected by the source and drain without any probability of surmounting the Si-SiO_2 potential barrier. Although the last technique has been implemented in a memory array [19], none of the above-mentioned techniques seems to be a viable way for integration in CMOS circuits because of the danger of latchup.

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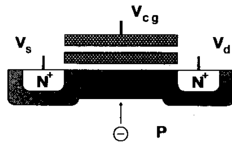


Fig. 1. A conventional substrate hot electron injection EPROM structure. The acceleration of electrons occurs in the depletion layer (hatched) perpendicularly to the monosilicon surface.

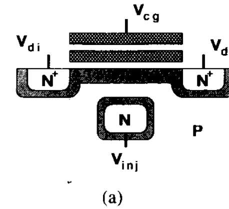
In spite of the promising programming method for EPROM's, the SHE injection was not attractive, because it lacked an efficient source of electrons. This problem has been overcome in the so-called VIPMOS structure [19]. The acronym VIPMOS stands for Vertical Injection Punchthrough-based MOS. This structure results in a local buried injector as the source of electrons. The basic device principle is explained in Section II. Section III deals with the device fabrication. Simulations emphasize some of the advantages of this device. Furthermore, a model for implementation in a circuit simulator is presented in Section IV. Experimental results are given in Section V and Section VI summarizes the conclusions.

II. Basic Principle

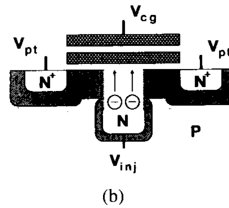
Fig. 2 visualizes the VIPMOS structure. The VIPMOS structure has an additional n-type doped area underneath the gate. This n-type area is the buried injector and acts as the source of electrons. Apart from the injector, the structure can be similar to the conventional SHE injection EPROM, as shown in Fig. 1.

In the programming mode, the injector is grounded. A high voltage V_{cg} is applied to the control gate. Fig. 2(a) shows the VIPMOS EPROM in the case of connecting both the source and drain to a voltage V_{di}. The substrate area between the MOS stack and injector is not completely depleted. Increasing the voltages on the source and drain will extend the depletion layer underneath the gate into the direction of the injector. At a certain voltage V_{dep}, the depletion layer will touch the depletion layer at the injector side. Further increase of the voltage leads to punchthrough (Fig. 2(b)). The punchthrough voltage V_{pt} is defined as the voltage on the source and drain, when the injector current increases and starts to deviate from the junction saturation current. In the punchthrough mode the injector emits electrons into the depletion layer under the floating gate. These electrons will be accelerated in the electrical field. Some of them will become hot and gain sufficient energy to surmount the Si-SiO_2 potential barrier. The injection mechanism is very efficient, because all electrons emitted by the injector are accelerated in the direction towards the Si-SiO_2 interface and have a chance of being collected by the floating gate. This will be illustrated in the next section. Utilization of the punchthrough mechanism for application in bipolar ROM's has already been reported by Lohstroh *et al.* [20]. Mouthaan *et al.* [21] used the punchthrough mechanism in a dynamic RAM cell. In the device, presented in this paper, it is combined with the generation of hot electrons for nonvolatile memories. Actually, the local buried injector, that is activated by means of punchthrough, combines the previously described advantages of the SHE injection with an efficient source of electrons.

Fig. 3 shows the energy band diagram of the VIPMOS structure under programming and read condition. The device can be characterized by two potential barriers ϕ_b and ϕ_f. ϕ_f is the po-



(a)



(b)

Fig. 2. The VIPMOS structure with the local buried injector. At V_s and V_d equal V_{di} the punchthrough condition is not satisfied (a). Both depletion layers just touch for the case that V_s and V_d equal V_{dep}. At a voltage V_{pt}, punchthrough occurs and the injector emits electrons into the depletion layer underneath the gate (b).

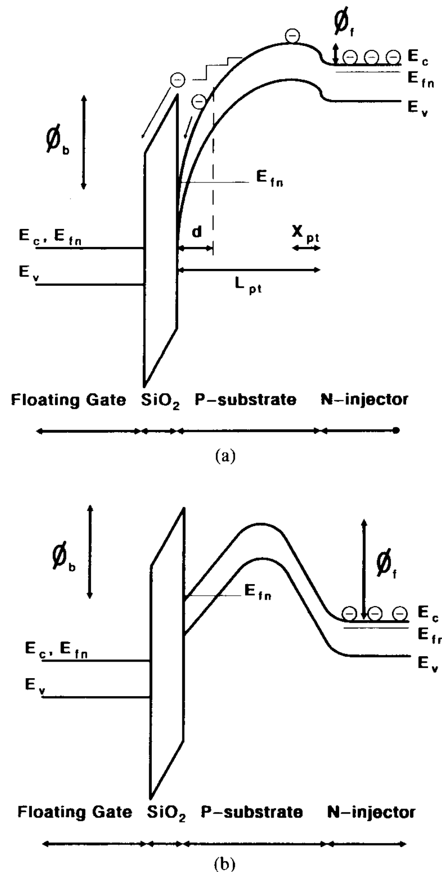


Fig. 3. The energy band diagram of the VIPMOS structure under programming (a) and read (b) condition. The device is characterized by two potential barriers ϕ_f and ϕ_b. ϕ_f is the barrier between the injector and the substrate area above the injector, whereas ϕ_b is the Si-SiO_2 barrier.

tential barrier between the injector and the substrate area above the injector, whereas ϕ_b is the Si–SiO$_2$ potential barrier. In the programming mode, ϕ_f is decreased when the source and drain voltage exceed V_{dep}. Electrons will diffuse over the lowered barrier (Fig. 3(a)) and are accelerated towards the Si–SiO$_2$ interface. Some of them may surmount the Si–SiO$_2$ barrier, the majority will be drained by either the source or drain. Fig. 3(b) shows the energy band diagram in the read mode. The injector potential is raised (e.g., it is connected to the drain voltage). Thus the barrier ϕ_f is increased, thereby preventing the emission of electrons from the injector.

In the punchthrough mode, the injector current can be written as

$$I_{inj} = I_0 \exp\left(\frac{q\Delta\phi}{kT}\right) \tag{1}$$

with

$$\Delta\phi = \phi_{j0} - \phi_f. \tag{2}$$

ϕ_f is the height of the potential barrier as indicated in Fig. 3(a) and ϕ_{j0} is the built-in potential of the junction between the injector and the substrate area above the injector. The dependence of $\Delta\phi$ on the channel potential ϕ_{ch} can be written as [22], [23]

$$\Delta\phi = \frac{\phi_{ch} - \phi_{dep}}{n} \tag{3}$$

where ϕ_{dep} is the channel potential, when the depletion layer under the gate just touches the depletion layer at the injector side. The nonideality factor n denotes the fraction of the increasing channel potential that is available to forward bias the junction between the injector and the substrate area above the injector. Our devices show typical nonideality factors of 3 to 4. Using (1) and (3), the punchthrough current may be written as

$$I_{inj} = I_0 \exp\left(\frac{q(\phi_{ch} - \phi_{dep})}{nkT}\right). \tag{4}$$

In fact, the nonideality factor n is not a constant, but it gradually increases with increasing $(\phi_{ch} - \phi_{dep})$. Assuming a highly doped injector and a homogeneously doped substrate area above the injector, a more precise expression for $\Delta\phi$ is given by [22], [23]

$$\Delta\phi = \frac{x_{pt}}{L_{pt}}(\phi_{ch} - \phi_{dep})\left(1 + \frac{x_{pt}}{L_{pt}}\frac{\phi_{ch} - \phi_{dep}}{4\phi_{j0}}\right) \tag{5}$$

with x_{pt} is the distance from the potential minimum, when $\phi_{ch} = \phi_{dep}$, to the injector and L_{pt} the distance from the Si–SiO$_2$ interface to the injector, as indicated in Fig. 3(a).

At high currents, I_{inj} will become space-charge-limited and it can no longer be described by an exponential behavior as in (4). For the derivation of the injector current it is assumed that the injector is grounded. For the case it is not grounded or it has a considerable resistance, ϕ_{ch} has to be replaced by the potential difference across the punchthrough structure.

Hot electron injection is often modeled by the Lucky Electron Model (LEM) [11]–[13]. This model was originated by Shockley [24] and later refined by Verwey *et al.* [11], [12] and Ning *et al.* [13]. Following this model, the probability for an electron of being injected over the potential barrier ϕ_b is given by

$$P_{inj} = A \exp\left(-\frac{d}{\lambda}\right) \tag{6}$$

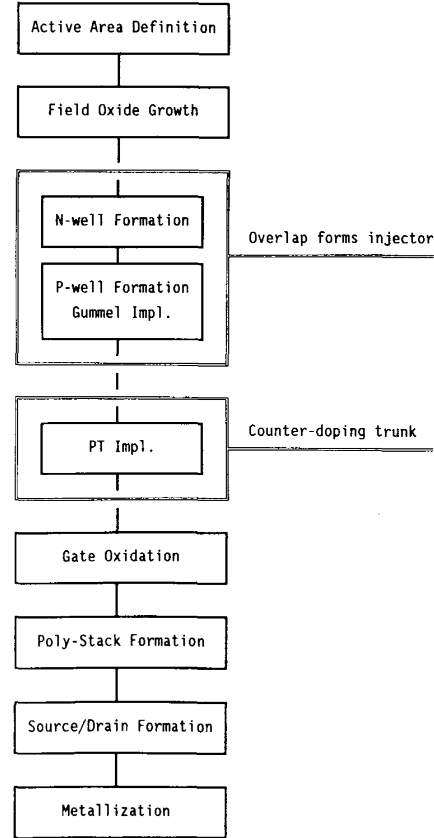


Fig. 4. Process flow forming the VIPMOS structure.

where A is a fitting constant. d is the minimum distance which an electron has to travel without suffering any collisions, in order to acquire an energy equal to the Si–SiO$_2$ barrier ϕ_b, as indicated in Fig. 3(a). λ is the scattering mean free path of an electron. Using the solution of the Poisson equation, the following expression for d can be derived, assuming a substrate area above the injector that is homogeneously doped to a concentration of N_a

$$d = \sqrt{\frac{2q\epsilon_{si}\phi_{ch}}{N_a}}\left(1 - \sqrt{1 - \frac{\phi_b}{\phi_{ch}}}\right), \qquad \phi_{ch} \leq \phi_{dep} \tag{7}$$

where q is the electronic charge and ϵ_{si} is permittivity of silicon. The height of the barrier ϕ_b is affected by the electrical field in the gate oxide. Ning derived an expression for ϕ_b, which incorporates the image force barrier lowering term and a "tunneling barrier lowering" term [13]

$$\phi_b = 3.2 - \beta E_{ox}^{1/2} - \alpha E_{ox}^{2/3} \tag{8}$$

with E_{ox} is the electrical field in the gate oxide. α and β are constants. E_{ox} is calculated by

$$E_{ox} = \frac{V_{flg} - V_{fb} - \phi_{ch}}{T_{ox}} \tag{9}$$

with V_{flg} is the floating gate voltage, V_{fb} the flatband voltage, and T_{ox} the gate-oxide thickness.

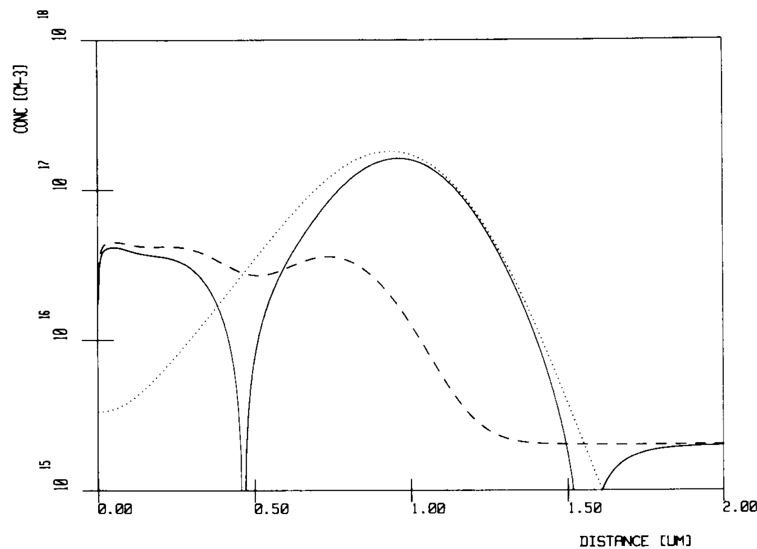


Fig. 5. The 1-D-doping profile of the buried injector as simulated with SUPREM III. The solid line represents the net doping concentration, the dotted line the phosphorus concentration, and the dashed line the boron concentration.

Using the above-mentioned equations, the current flowing to the floating gate can be calculated as

$$I_{flg} = P_{inj} \times I_{inj} \tag{10}$$

thereby combining the LEM with the punchthrough model.

III. Process Description and Simulation

The process simplicity makes the application of VIPMOS structures attractive for custom CMOS applications. The buried injector structure can easily be realized by high-energy ion implantation. In this way, the Gummel number of the substrate area above the injector can be well-controlled. This is important, because the punchthrough voltage is sensitive to the Gummel number. To create a local injector, the conventional buried layer does not seem to be favorable. The possible spread in the thickness and doping concentration of the epitaxial layer result in a nonreproducible Gummel number of the region above the injector.

Essentially, the buried injector is formed just by an overlap of the retrograde n-well and p-well of our high-energy ion-implanted CMOS process [25]. The process flow is given in Fig. 4. The Gummel number of the substrate area above the injector is given by

$$Q = \int_0^{L_{pt} - x_{pt}} \left(N_a(x) - N_d(x)\right) dx. \tag{11}$$

$N_a(x)$ and $N_d(x)$ are determined by the p-well and n-well profile, respectively. The wells are implanted immediately after the field oxidation. The retrograde n-well, in which the normal PMOS devices are formed, is made by a single implantation step of 1-MeV phosphorus ions and a dose of 1×10^{13} cm^{-2}. The retrograde p-well is formed by a boron implantation with an energy of 350 keV and a dose of 1.5×10^{12} cm^{-2}. The retrograde p-well implantation determines the threshold voltage of the parasitic field-oxide NMOS. This implantation is fully covered by the overlapping n-well implantation at the injector side. An additional boron implantation with an energy of 110 keV and a dose of 1.5×10^{12} cm^{-2} is done through the same mask. This implantation, further referred to as Gummel implantation, is necessary to suppress the front flank of the retrograde n-well profile. The Gummel implantation ensures a reproducible Gummel number of the substrate area above the injector. The p-well loses its retrograde character due to the Gummel implantation. The threshold voltage of the normal NMOS devices is determined by two boron implantations. The first boron implantation with an energy of 40 keV and a dose of 2×10^{11} cm^{-2} is performed during the p-well formation. The second boron implantation, that also covers the threshold voltage adjustment of the normal PMOS devices, is a blanket implantation with an energy of 10 keV to a dose of 5×10^{11} cm^{-2} through the gate oxide with a thickness of 25 nm. Obviously, these boron implantations also affect the Gummel number of the substrate area above the injector. The doping profile of the bur-

TABLE I
Different Gummel and Threshold Adjustment Implantations that Have Been Used to Vary the p-Well Profile, in Order to Investigate its Influence on the Punchthrough Voltage, Injection Probability, and Nonideality Factor n

Device	Dose (cm^{-2})/Energy (keV)	
	Gummel Implantation	Threshold Adjustment
A	$1.5 \times 10^{12}/210$ $1.5 \times 10^{12}/70$	—
B	$1.0 \times 10^{12}/210$ $1.5 \times 10^{12}/70$	—
C	$2.0 \times 10^{12}/150$	$5.0 \times 10^{11}/10$ $2.0 \times 10^{11}/40$
D	$1.5 \times 10^{12}/110$	$5.0 \times 10^{11}/10$ $2.0 \times 10^{11}/40$

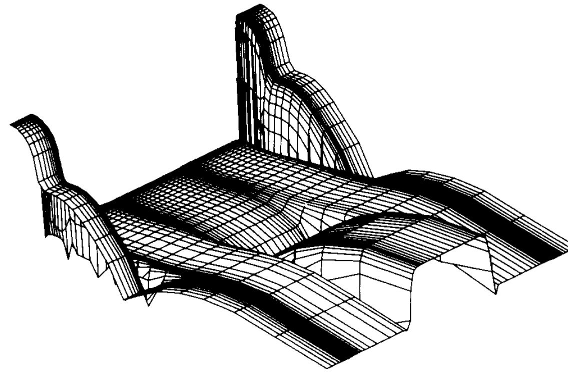


Fig. 6. 2-D-doping profile of the VIPMOS structure, which is used for the device simulations.

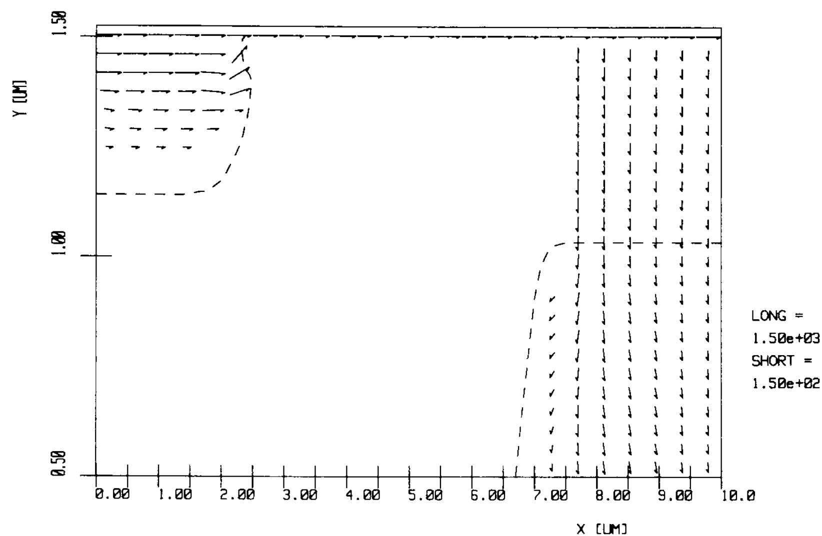


Fig. 7. A vector plot of the electron current density in programming mode. The dashed lines denote the junctions. The spacing between the injector and source is 5 μm. The injector is grounded V_s = 5 V and V_{fg} = 10 V. The injection of electrons from the injector only occurs in the direction of the floating gate.

ied injector, as simulated with SUPREM III [26], is shown in Fig. 5. The junction depth, resulting from the p-well and n-well overlap (device D in Table I), is about 0.5 μm.

In principle, the buried injector can be realized without any extra masking step. However, in the case of the formation of high-energy ion-implanted buried layers an n-type trunk from the buried layer up to the surface arises at the mask edge [27]. The trunk implies an electrical connection between the buried layer and the inversion layer, preventing the VIPMOS structure from operation. In order to tackle this problem, an additional PT-masked (Preventing Trunk) implantation, 150-keV boron ions up to a dose of 5×10^{12} cm^{-2}, is carried out at the edges of the injector. Unfortunately, the PT mask increases the device dimensions at this moment.

The Gummel implantation will scarcely affect the threshold voltage of the normal NMOS devices, because it is a deeper implantation. On the other hand it will considerably increase the bulk factor, especially when higher doses are used in order to obtain a high punchthrough voltage. Also the PT implantation will have a profound effect on the bulk factor.

It is interesting to investigate the influence of the Gummel number of the substrate area above the injector on the injection probability. Generally, a high Gummel number results in a high punchthrough voltage and high injection probability, whereas a lower Gummel number will give a lower punchthrough voltage and lower injection probability [28]. In addition to the Gummel number of the region above the injector, the resulting shape of the profile of the p-well influences the injection probability. A high boron peak near the Si-SiO_2 surface locally enhances the electrical field and leads to a higher injection probability. The shape of the p-well profile also influences the nonideality factor n. A deeper Gummel implantation will shift the position of the potential barrier ϕ_f into the direction of the injector, thereby increasing the nonideality factor n. In order to investigate these aspects, the Gummel implantation and the threshold adjustment implantations were varied. This resulted in four devices A to D

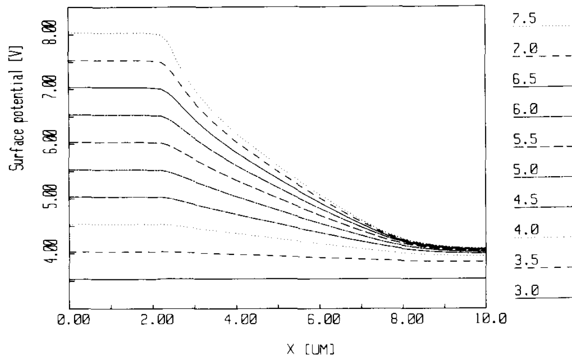


Fig. 8. The potential along the $Si-SiO_2$ interface at different source voltages. The source junction is situated at $x = 2$ μm and the injector junction at $x = 7$ μm. At a certain voltage, the channel potential is no longer constant along the whole injector area.

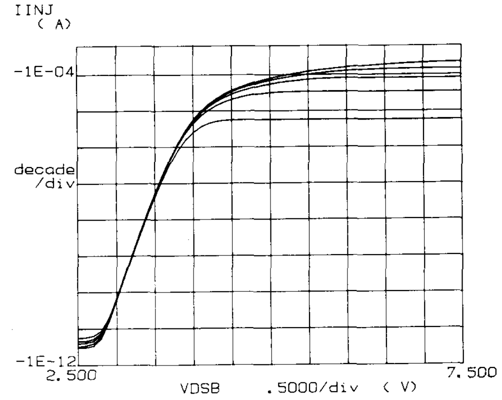


Fig. 9. Typical curves of a VIPMOS device. V_{flg} varies from 7.5 to 11.5 V in steps of 1 V. At low V_{dsb} the current is independent of V_{flg}. At higher V_{dsb} the MOS action dominates the device.

as listed in Table I. The retrograde p-well and n-well implantations were identical for all devices. Section V will deal with the measurements resulting from these devices.

Fig. 6 shows the 2-D doping profile of the VIPMOS structure. This profile is used for device simulation with TRENDY, a 2-D device simulator [29]. In the programming mode the device behavior is symmetrical. Therefore, only one half of the structure is simulated in order to save computation time. A vector plot of the electron current density under programming condition is shown in Fig. 7. The electron current density from injector towards the channel easily exceeds 200 $A \cdot cm^{-2}$ in the programming mode. The electron current density is not constant along the whole injector area. The local injector current density as well as the local injection probability is determined by the channel potential above the injector area. This channel potential itself depends on the amount of charge, which can be derived from the channel by the source and drain. This effect is emphasized in Fig. 8. It displays the channel potential along the surface from source to injector at different source voltages. Notice that at a certain source voltage, the channel potential apparently has no longer a constant value along the whole channel. This restricts the applicability of the LEM, which will be explained in the following section.

As can be seen from Fig. 7, the injection of electrons occurs in vertical direction. Moreover, the injection does not occur in lateral direction, where it might trigger other structures. Holes, generated by impact ionization in the depletion layer under the floating gate, contribute to the substrate current. This substrate current may cause a parasitic bipolar action [30]. The influence of the substrate current is suppressed by the use of a heavily doped p-type substrate [25]. Therefore, the VIPMOS structure seems to be suitable for application in VLSI circuits without the danger of latchup.

IV. VIPMOS Model

Fig. 9 shows a typical plot of the measured injector current as a function of the drain/source to bulk voltage (V_{dsb}) at different "floating" gate voltages (V_{flg}). At drain/source voltages only slightly higher than the punchthrough voltage, the current has a logarithmic behavior and can be well described by (1) and (5). The injector current is independent of V_{flg}. The potential in the channel above the injector region is constant and fixed to a value of about

$$\phi_{ch} = V_{dsb} + 2|\phi_p| \tag{12}$$

with ϕ_p is the substrate Fermi potential. In this case the injector current can be modeled with the help of the previous equations. For the "floating" gate current the LEM can be used. At higher V_{dsb}, the current is dominated by the MOS action. The drain/source to bulk voltage, at which this applies, is further referred to as V_{tr}. For V_{dsb} greater than V_{tr}, the potential in the channel will gradually increase from the middle of the injector to the source and drain. This implies that the injection will not be homogeneous, and moreover the injection probability varies over the injector area. Electrons that are injected closer to either the source or drain have a greater probability of surmounting the $Si-SiO_2$ potential barrier. Thus the injection probability will not only be dependent on V_{flg}, but also on V_{dsb}. This phenomenon is more pronounced for devices with a low Gummel number of the substrate area above the injector. A more precise expression for the "floating" gate current is

$$I_{flg} = \int_{x=a}^{x=b} P_{inj}(x) I_{inj}(x)\, dx \tag{13}$$

where a and b are the boundaries of the injection area. This effect makes a use of the LEM for SPICE modeling inconvenient, because a precise knowledge of the channel potential is required. Therefore, an empirical relation for the injection probability is introduced

$$P_{inj} = P_0 + P_k I_{inj}(V_{flg} - V_{P0}). \tag{14}$$

In (14), P_0 is the injection probability at an arbitrary "floating" gate voltage V_{P0} and $P_k(A^{-1} V^{-1})$ is a fitting constant.

In Fig. 10 the model for the VIPMOS structure is given. This model has been implemented in SPICE. The punchthrough current source is modeled with the help of (1) and (5). We have used the SPICE level3 MOS model [31] for the MOS behavior. The floating gate current is included in the model, using (10) and (14). R_{inj} is the resistance of the injector. It should necessarily be incorporated in the model, because the injector sheet resistance is 1000 Ω/□. The parameters for the model are obtained from the parameter extraction program PROMEA [32] and will be discussed in the next section.

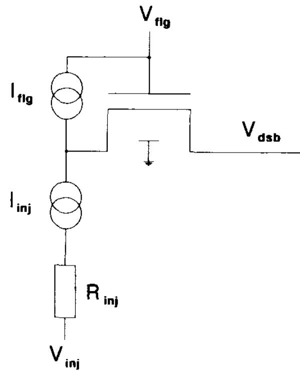


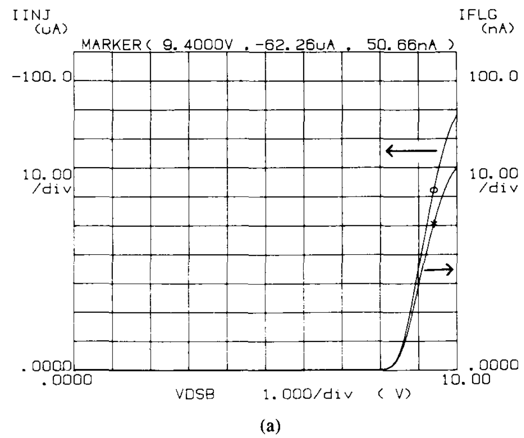
Fig. 10. Model for the VIPMOS structure that has been implemented in SPICE.

V. Measurements and Discussion

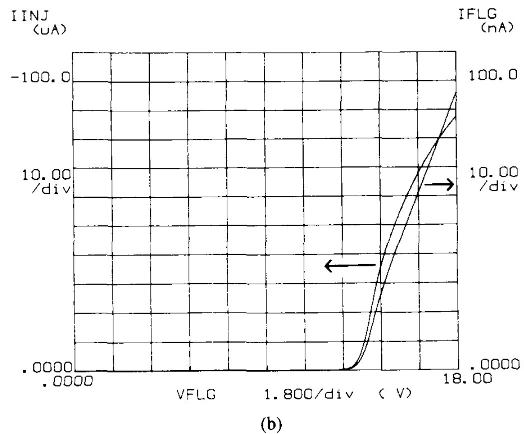
We have fabricated several VIPMOS structures with different punchthrough voltages by varying the doping profile of the p-well. Fig. 11(a) shows the measured injector and "floating" gate current of device A as a function of the drain/source to bulk voltage V_{dsb}. The "floating" gate voltage V_{flg} is 15 V. The punchthrough voltage of this device is 6.85 V and V_{tr} is 8.0 V. The injection probability at the point indicated by the marker is nearly 1×10^{-3}. The injector area of this device equals 12.5 μm^2. It can be calculated that the electron current density in the gate oxide exceeds 0.4 $A \cdot cm^{-2}$. At higher values of V_{dsb} and V_{flg} oxide current densities of 1 $A \cdot cm^{-2}$ are measured. These high values are acquired as a result of a high injection probability accompanied by an efficient electron injection mechanism. In Fig. 11(b) the injector current and "floating" gate current of the same device are plotted as a function of V_{flg}. V_{dsb} is 9 V. It is clearly demonstrated that below a certain value of V_{flg} the injector does not emit electrons, because the punchthrough condition cannot be satisfied at low V_{flg}. Consequently, the injection automatically stops in such an EPROM, when a sufficient amount of charge carriers is accumulated on the floating gate.

The high oxide electron current densities may result in estimated programming times in the microsecond range for optimized structures. These expectations are based upon measurement results shown in Fig. 12. This figure displays the programming characteristics of devices A and D. Device A has a high injection probability and device D can be programmed with a low drain voltage of 5 V. These devices are not optimized. The total floating gate capacitance C_{tot} is approximately 0.8 pF, the coupling ratio has a value of 0.6, and the injector area is 12.5 μm^2. Notwithstanding its considerable C_{tot}, device A reveals a threshold voltage shift of about 3 V within 10 μs. Optimized devices with the same injector area can have a C_{tot} less than 0.1 pF. This will result in programming times which are approximately one order of magnitude shorter than the times shown in Fig. 12. The relatively high control gate voltages can be reduced by increasing the coupling ratio and decreasing the threshold voltage shift. Currently, no optimized cell structures are available. However, a 5-V-only 16K flash E^2PROM with optimized VIPMOS structures is under development [5].

For analog applications, such as neural networks [4], a VIPMOS structure with a lower punchthrough voltage is desirable for supply voltage considerations. Thus a tradeoff should be made between the injection probability and the supply voltage. Fig. 13 shows the characteristics of device D. The punchthrough voltage V_{pt} of device D is 2.75 V and V_{tr} is 3.8 V. The squares in the figure represent the data that have been stored



(a)



(b)

Fig. 11. The measured injector (left axis) and "floating" gate current (right axis) of a device A as a function of the drain/source to bulk voltage (V_{dsb}) with the "floating" gate voltage (V_{flg}) is 15 V (a) and as a function of V_{flg} with V_{dsb} is 9 V (b).

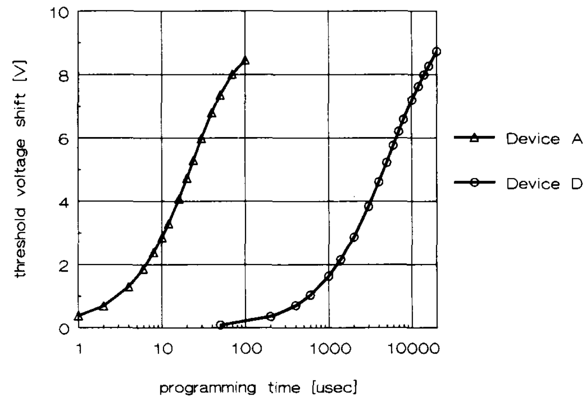
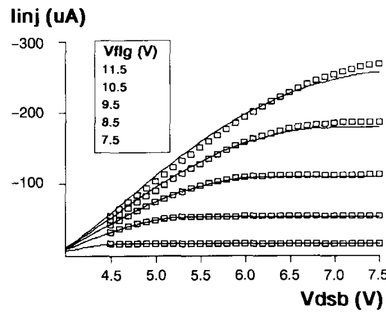
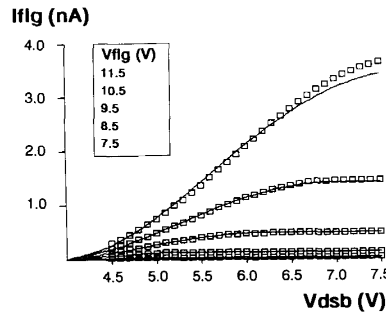


Fig. 12. Measured programming times of the nonoptimized devices A and D. Programming conditions for device A are: V_{dsb} = 10 V and V_{cg} = 25 V. For device D the conditions are: V_{dsb} = 5 V and V_{cg} = 20 V.



(a)



(b)

Fig. 13. Measured (squares) and fitted (solid lines) injector (a) and "floating" gate current (b) of device D, using the model for SPICE. The RMS error is 2.9%.

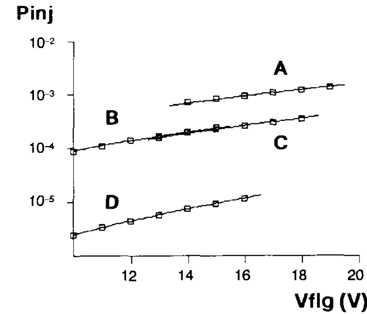


Fig. 14. The measured (squares) and fitted (solid lines) injection probability for the devices A-D using the Lucky Electron Model. The rms error is 1.6%.

TABLE II
THE SPICE MODEL PARAMETERS GIVING THE BEST FIT WITH THE MEASURED INJECTOR AND "FLOATING" GATE CURRENT OF DEVICE D

Parameter	Unit	Value
ϕ	V	0.64
V_{t0}	V	0.56
K_p	$A \cdot V^{-2}$	3.11×10^{-5}
γ	$V^{0.5}$	1.54
θ	V^{-1}	9.63×10^{-2}
V_{max}	$m \cdot s^{-1}$	6.34×10^{4}
W_{mos}	m	10×10^{-6}
L_{mos}	m	5×10^{-6}
I_0	A	1.91×10^{-11}
x_{pt}	m	1.74×10^{-7}
L_{pt}	m	0.50×10^{-6}
V_{pt}	V	2.73
ϕ_{j0}	V	0.58
R_{inj}	Ω	1.44×10^{3}
P_0	·	2.01×10^{-6}
P_k	$A^{-1} \cdot V^{-1}$	1.09×10^{-2}
V_{P0}	V	7.5

after measurement, whereas the solid lines denote the theoretical curves according to the model that has been explained in Section IV. The parameters used in this model have been extracted by the parameter extraction program PROMEA [32] and are listed in Table II. The rms error of the fit is 2.9%. As can be seen from Fig. 13(a), the injector current can quite well be described by the model, which is composed of the punch-through, and SPICE level3 MOS model. The injection probability, being modeled by a linear relationship between the gate voltage and injector current, gives a good prediction for the floating gate current (Fig. 13(b)). The extracted parameters (Table II) do have realistic physical values. The relatively high value, found for the bulk factor gamma, originates from the implantation which should prevent the trunk from the buried injector to the inversion channel [27]. Also the injector resistance R_{inj} of 1.4 kΩ is in good agreement with the value that was expected from the layout configuration.

It is not the intention of this paper to check or approve the physical correctness of the LEM. However, it is interesting to examine, whether the experimental results concerning the reported LEM parameters [6], [13] are applicable to our devices. Hence, the injection probability is measured as a function of V_{flg}. The injection probability P_{inj} is obtained from the division of the measured "floating" gate current by the injector current V_{dsb} is kept at V_{tr}. In the V_{dsb} range, V_{pt} to V_{tr}, the injector current hardly changes with V_{flg} as demonstrated in Fig. 9. So a constant potential along the whole inversion channel can be expected. The results are illustrated in Fig. 14. The squares are the measured data and the solid lines are the theoretical curves according to the LEM. Equation (7) is used to calculate the distance d (this equation is valid for $\phi_{ch} \leq \phi_{dep}$). The minor change in the position as well as the height of the potential barrier ϕ_f for $V_{dsb} = V_{tr}$ only introduces a small error. A value of 9.2 nm was used for λ [6], [13]. The image force barrier lowering constant β was taken as 2.59×10^{-4} $(V \cdot cm)^{1/2}$. The measured data have been fitted with the LEM by means of the doping concentration N_a and the empirical LEM parameters A and α. The theoretical curves correspond very well to the measured data. The rms error is 1.6%.

The assumption of a homogeneously doped substrate above the injector does not disturb the validity of the LEM. In our devices the doping profile in the area above the injector is rather constant and does not have a pronounced shape. Our derivation concerning the injection probability may not be appropriate for devices with a high surface concentration declining to the injector, because an increase of the electrical field in the vicinity of the $Si\text{-}SiO_2$ interface will greatly enhance the injection probability.

The parameters of the theoretical injection model, which give the best fit in measured injection probability, are tabulated in Table III. The value of A is 2.9 and it corresponds very well to the value which has been reported by Ning *et al.* [13]. The

TABLE III
THE MEASURED PUNCHTHROUGH VOLTAGE V_{pt} AND THE NONIDEALITY FACTOR n OF DEVICES A–D
(The fitted doping concentration N_a as well as the parameters of the Lucky Electron Model are included.)

Device	V_{pt} (V)	V_{tr} (V)	n	N_a (cm^{-3})		
A	6.85	8.0	3.6	5.27×10^{16}	λ (nm)	9.2
B	4.75	5.8	3.2	4.69×10^{16}	α ($V^{1/3} \cdot cm^{2/3}$)	7.52×10^{-6}
C	5.35	6.5	3.6	5.33×10^{16}	β ($(V \cdot cm)^{1/2}$)	2.59×10^{-4}
D	2.75	3.8	3.0	4.36×10^{16}	A	2.9

"tunneling barrier lowering" constant α of our devices, 7.5×10^{-6} $V^{1/3} \cdot cm^{2/3}$, is slightly less than the 1×10^{-5}, determined by Ning *et al.* [13]. However, the value is in contrast with the 4×10^{-5}, obtained by Tam *et al.* [6]. From these results it can be stated that the LEM can be used in our devices to predict the injection probability in the case of a constant surface potential.

It can be seen from Fig. 14 and Table III that the doping profile in the injector area strongly influences the punchthrough voltage and injection probability. Therefore, a reproducible VIPMOS structure can only be realized by well-controlled processing, such as ion implantation.

The highest injection probabilities are acquired by device A. This directly results from the high punchthrough voltage. On the other hand, the injection probabilities as obtained from device B and C are nearly the same, although the punchthrough voltages differ 0.6 V. This can be explained as follows: the nonideality factor n of device C is greater than that of device B; thus the position of the potential barrier ϕ_f is shifted towards the Si–SiO_2 interface surface in the latter case, thereby compensating the effect of the lower value of the punchthrough voltage.

The dependence of the injection probability on the electrical field in the gate oxide is more pronounced for the devices with a low punchthrough voltage. It is evident that the use of image force barrier lowering and "tunneling barrier lowering" are of great importance for 5-V-only circuits applying VIPMOS devices, in order to increase the injection probability.

VI. CONCLUSIONS

A novel high-energy ion-implanted VIPMOS structure has been presented. The structure includes a local buried injector, which is used to supply the electrons for the SHE injection. The fabrication of the VIPMOS structure involves a local overlap of the wells of a retrograde twin-well CMOS process and one extra implantation to obtain an accurate Gummel number of the substrate area above the injector. One extra mask is necessary to cover the trunk, that shows up from the buried injector to the Si–SiO_2 interface due to mask edge effects. For this reason, the VIPMOS EPROM cell consumes more area than an EPROM cell using CHE injection. The injector is activated by means of punchthrough. This makes the structure suitable for VLSI applications without the danger of latchup. The punchthrough voltage can be set by the doping profile of the p-well. The local buried injector offers new possibilities for programming EPROM's using SHE injection.

A high Gummel number of the area above the injector results in a high punchthrough voltage and a high injection probability (about 1×10^{-3}). In consequence of the high injection probability and effective injection mechanism, high oxide current densities of 1 A $\cdot$ cm^{-2} and programming times of 10 μs have been measured. On the other hand, the punchthrough voltage can be adjusted to a low value of about 3 V, which enables the application of the VIPMOS structure in EPROM's for analog circuitry or 5-V-only digital memories. For this purpose, a model was proposed which has been implemented in SPICE. This model can very well predict the injector and floating gate current.

The parameters of the LEM, obtained from a parameter extraction, are in good agreement with the parameters as reported by Ning *et al.* [13]. Only the dependence of the Si–SiO_2 potential barrier on the "tunneling lowering" term is slightly less.

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